PMC technology

By Greg Novak

Introduction

Designers typically use native form factor cards to expand I/O on CompactPCI- and VME-based systems. However, implementing a simple function on a CompactPCI or VME card can at times cause overhead to be excessive. Simple I/O functions require a lower cost and smaller form factor standard. Recognizing the need for a mezzanine standard to solve this problem, IEEE released P1386 and P1386.1 in the summer of 2001. PICMG and VITA have enhanced these standards to meet telecommunications and higher throughput requirements. Although the modules target CompactPCI and VME, manufacturers can use them on any form factor with the required mechanical, electrical, and signaling functions. This article will introduce the PCI Mezzanine Card (PMC) and the extensions added by PICMG and VITA.

Description

The PMC standard combines two IEEE standards, IEEE P1386 Standard Mechanics for a Common Mezzanine Card (CMC) family and IEEE P1386.1 Standard Physical and Environmental Layers for PMC. The P1386 standard defines the form factor, connector, and electrical interconnects. P1386.1 maps PCI bus signals onto P1386 cards. The CMC specification defines two module sizes: single (74mm by 149mm) and double (149mm by 149mm). The bezel on a CMC protrudes through the carrying card to allow access to I/O. Four connectors labeled P1, P2, P3, and P4 interconnect to the CMC. Figure 1 shows a singlewide CMC.

As mentioned, the CMC provides the mechanical and interconnect standard for a mezzanine module. The PMC specification maps PCI signals onto CMC-defined interconnects. The 32-bit PCI bus requires two 64-pin connectors, P1 and P2. The 64-bit PCI bus requires three 64-pin connectors P1, P2, and P3. The remaining 64-pin connector, P4, routes I/O signals to a Rear Transition Module (RTM). The PCI specification allows 3.3V or 5V signaling and requires manufacturers to key the PMC module to denote the required voltage (I/O). OEMs can key the PMC for 3.3V, 5V, or universal operation. Users of PMC modules need to make sure that the voltage (I/O) the carrier delivers is compatible with the PMC voltage (I/O). Users commonly remove the voltage (I/O) key from the PMC module because it is *in the way*, when in reality the PMC module and carrier card do not support compatible voltages.

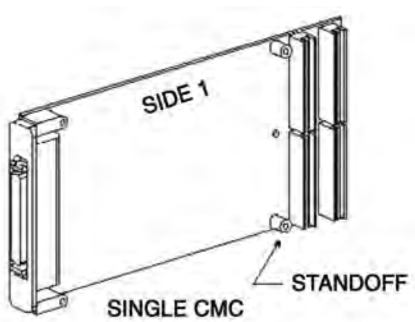

Figure 1

The VITA Standards Organization initiated one of the first enhancements made to the PMC specification. The PMC specification relied on the carrier for the PCI bus monarch. Defined as the main PCI bus processor, the monarch performs the bus enumeration and handles interrupts. The PMC specification expected that the monarch resided on the carrier card and made no provisions for the PMC module to be a monarch. To correct this, the VITA 32 specification defined the signals necessary to allow a PMC module to be a monarch. This specification opened the door for a new family of PMC modules, Processor PMCs (PrPMCs). In addition to specifying signals to support monarch mode, VITA 32 also addressed some of the thermal and component height restrictions that limited designers' abilities to place processors on PMC modules.

The original PMC specification supported 33-MHz and 66-MHz PCI operation. In 2002 the VITA Standards Organization recognized the need to add PCI-X operation support. The VITA 39 specification added the PCIXCAP signal to the PMC P1 connector. This signal allows the PMC to support 66-, 100-, and 133-MHz PCI-X transactions. The VITA 39 specification also included simulation work necessary to define the maximum supportable number of PCI loads at various operating frequencies. Determining the maximum number of supportable PCI loads is important because most PMC carrier cards have other local PCI devices. Sharing the PCI bus between card devices and the PMC can lead to unforeseen operational challenges. If the local PCI segment is running at PCI-X 133-MHz, and a 33-MHz PMC is installed on the segment, then the segment will run at 33-MHz. Care should be taken to identify the impact to any other device that shares the PCI bus segment when using PMC carriers that support PCI-X speeds. In Figure 2, a PMC and PCI-X bridge share a PCI-X 100-MHz bus. When the PMC is not installed, this bus will run at the PCI-X 100-MHz speed. If a 33-MHz PCI PMC is installed, then the segment will run at the 33-MHz PCI speed, slowing bridge throughput.

PCI interface has served the CompactPCI and VME markets well, but lacks the ability to handle the packet-based data transport interfaces network processors require. In August 2001, PICMG released the PICMG 2.15 PCI Telecom Mezzanine Card (PTMC) specification. This specification supports four popular industry standard telecom bus interfaces (H.110, UTOPIA Level 2, POS-PHY, and RMII) and the existing 32- and 64-bit PCI bus. PICMG released an ECR to PICMG 2.15 at the end of 2002. This ECR expanded the number of configurations supported from four to seven by adding Ethernet capabilities to TDM and UTOPIA configurations. PICMG 2.15 flexibility comes at a price, namely ease of use. The PICMG 2.15 subcommittee had to live within the pins available in the PMC specification. Limited pin count required that users document specific configurations and pin usages. This limitation also redefined the pins traditionally used for the upper 32 bits of the 64-bit PCI interface to support the new I/O capabilities, limiting PTMCs to 32-bit PCI interfaces. It is important to verify that the PTMC and its carrier card support the same configuration. Table 1 defines at a high level some of the PTMC configurations available.

Their configuration types determine the capabilities of a PTMC and carrier card.

As an example, a PT5MC (referring to the PTMC) and PT5CC (referring to the carrier card) support configuration 5 (2 Ethernet and 32-bit PCI interfaces). The various configuration types affect the number of PMC I/O lines available to support rear I/O. Consider interface and rear I/O requirements when selecting the type of PTMC.

Conclusion

PCI Mezzanine Card IEEE 1386.1 specifies a mezzanine module standard used to add I/O functionally independent of form factor. This specification initially used the PCI bus as the protocol between the mezzanine and its carrier. The VITA Standards Organization later extended the protocol to include PCI-X and support PrPMCs. PICMG further extended the protocol to include packet-based transports such as UTOPIA and POS-PHY. However, the flexibility these enhancements offer affects compatibility. Users of PMC modules need to make sure that the transport used, voltage (I/O), rear I/O interconnects, and monarch support are compatible with the carrier card. Even with these challenges, the PMC module provides a cost-effective way to add I/O capability to a variety of form factors.

Released Specifications

- IEEE 1386.1 – PMC
- VITA 39 – PCI-X PMC
- VITA 32 – PrPMC
- PICMG 2.15 PCI Telecom Mezzanine/ Carrier Card

For further information, visit these Web sites at www.ieee.org, www.picmg.org, and www.vita.com.

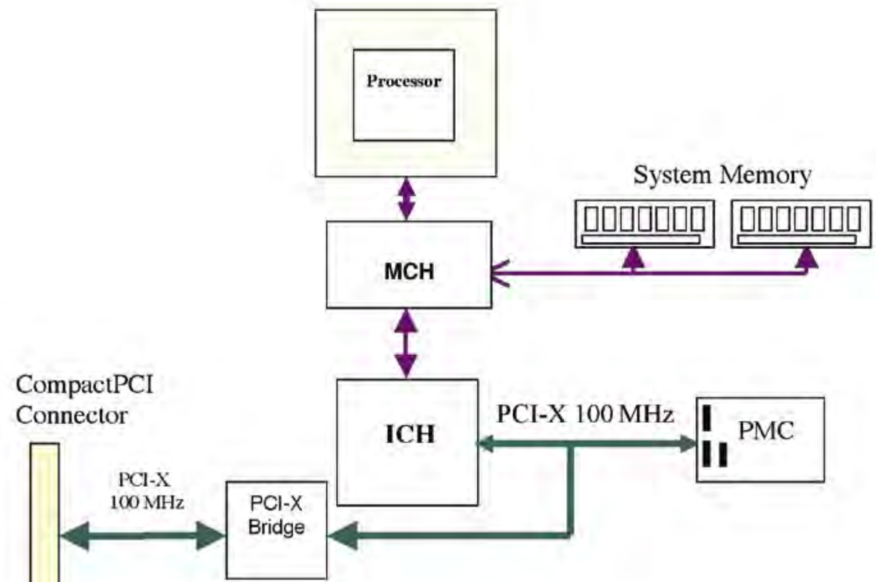

Figure 2

Interface	Configuration						
	1	2	3	4	5	6	7
Serial Tx/Rx	X	X	X	X	X	X	
RMII		X	X				
RMII PHY Management I/F		X	X				
10/100/1000 Ethernet					2	2	
UTOPIA I/II (8-bit)	X		X	X		X	
UTOPIA II (8/16-bit)				X		X	
POS-PHY				X			
Local CT (20-bit)		X	X				
Extended Local CT (32-bit)					X		
User I/O Pins	64	66	6	0	40	4	64
32-bit PCI	X	X	X	X	X	X	X
64-bit PCI							X
JTAG	X	X	X	X	X	X	X
SMB	X	X	X	X	X	X	X

Table 1