DESIGN

# Tools for a highly agile design environment

*By Maged Attia*

*The demand for short IC design cycle times has accelerated with the increasing time-to-market requirements placed on manufacturers of circuit cards for application in the industrial, communications, and embedded systems markets.*

*This need squarely impacts the choice of Electronic Design Automation (EDA) tools for the IC manufacturer wishing to bring advanced products to these card manufacturers in a timely manner. It is compounded by the need for mixed-signal design capability, a straightforward hierarchical design suite that links Integrated Circuit (IC) layout, Design Rule Checking (DRC), and circuit verification, as well as the requirement that such tools be compatible with and run well on Windows (W2K or WXP) or Linux PC platforms.*

*This article will review the above needs and describe how an effective, yet efficient and simple, design environment can be implemented with off-the-shelf tools that are appropriate for both small, fast-moving startup companies and larger enterprises that seek to enhance the efficiency of their design efforts.*

## Tools requirement checklist

One tool fits all doesn't apply when designing complex ICs. To design CompactPCI systems, or mixed-signal circuits in general, the designer needs to find the right tool for the job. Unreliable tools won't meet all requirements and too much tool can be a burden on the design process. The following list details important tool requirements that should be considered when designing mixed-signal commercial chips.

**Powerful layout editing controls**

When designing highly sensitive analog modules, manual layout editing cannot be avoided. The following features in the design tool make this process efficient and less time consuming:

- All-angle and curved shapes capabilities
- Multiple object editing
- Edit-in-place directly to any object in the hierarchy
- Edge, corner, arc, and stretch editing
- Virtual layer palette
- Object slice, rotation, and flipping

**Integrated place and route capability**

When designing highly dense digital modules, an integrated place and route tool is required that performs standard cell place and route, padframe generation, and pad routing. To minimize total area, a built-in routing optimizer automatically reduces the number of vias and net length. The place and route tools should include the following features:

- Multiple routing layers
- Cell clustering option
- Specification of critical nets
- Global signal routing for clock and reset nets
- Back annotation with net capacitances

**Accurate, foundry compatible DRC**

Foundry design rule checking is the most critical step in the chip design cycle. In mixed-signal design, the DRC is critical because multiple foundry rule sets must be checked. The features below ensure accurate and fast DRC:

- Foundry compatibility to reduce chances of manual error
- All-angle hierarchical DRC checking capability
- Off-grid, self intersection, vertex count, and all-angle edge checks
- Full chip and local region check
- Seamless integration with the layout environment
- Hierarchical and powerful errors navigator
- Cell exclusion capability

**Device and parasitic extraction**

The verification process doesn't stop at the DRC. Even though the design might pass the DRC, its response can be unpredictable if the parasitics are not considered. To better predict the design performance and to reduce the number of prototypes, the design tools should be able to extract not only the devices in the layout but also the different types of parasitics in the devices and in the connections between them. Full ship support is required.

**Layout vs. Schematic (LVS) comparison**

The last step in the verification process is to compare the layout and the schematic. The comparison report that the tool generates is as important as the comparison itself. The tool should be able to compare the layout and the schematic accurately as well as provide a detailed report that helps debug any mismatches.

## Hot-swap controller IC

Summit Microelectronics, Inc. developed one of the first hot-swap controller ICs. The SMH4044 is a fully integrated hot-swap controller that provides complete power control for add-in cards, ranging in use from basic hot-swap systems to high-availability systems. It detects proper insertion of the card and senses valid supply voltage levels at the backplane.

Utilizing external low on-resistance N-channel MOSFETs (Metal-Oxide Semiconductor Field-Effect Transistors), card power is ramped by two high-side driver outputs that are slew-rate limited at 250V/sec. The SMH4044 (see the functional block diagram in Figure 1) continuously monitors the host supplies, the add-in card supplies and the add-in card current. If the SMH4044 detects that the current is higher than the programmed value, it will shut down the MOSFETs and issue a fault status back to the host. The onboard Electrically Erasable Programmable Read-Only Memory

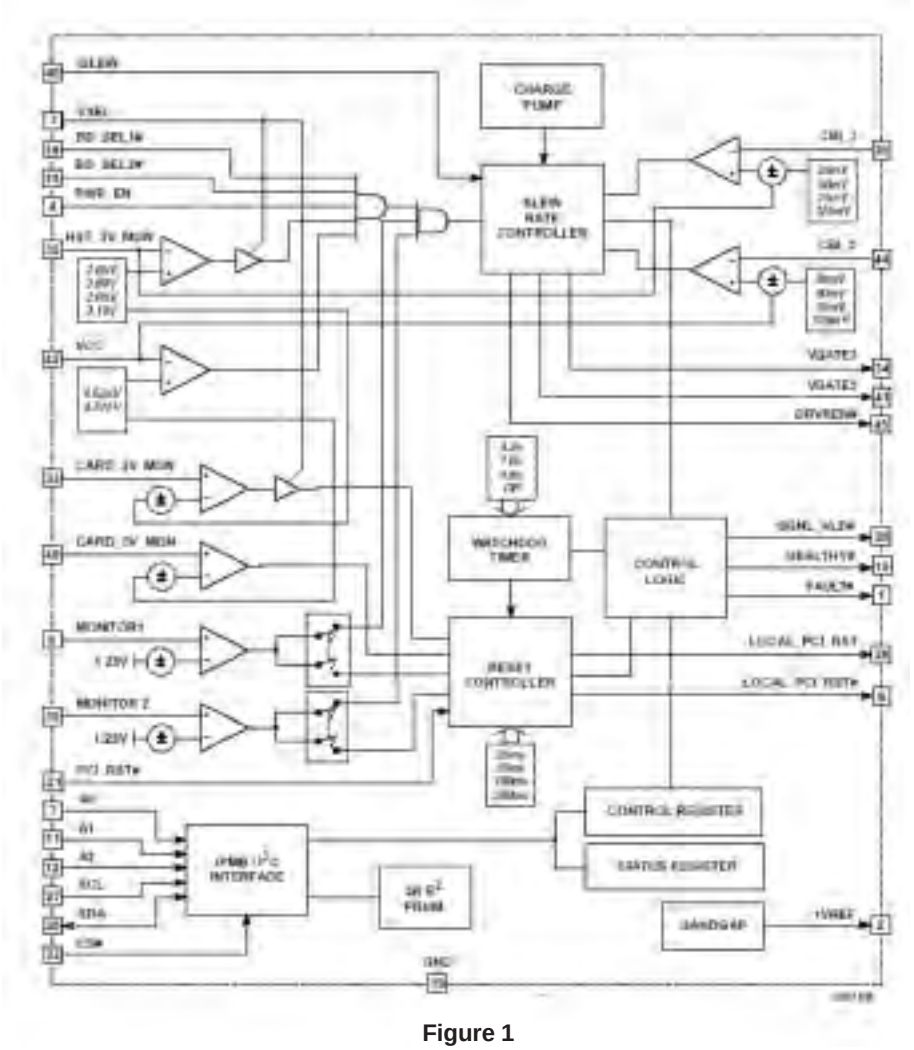


**Figure 1**

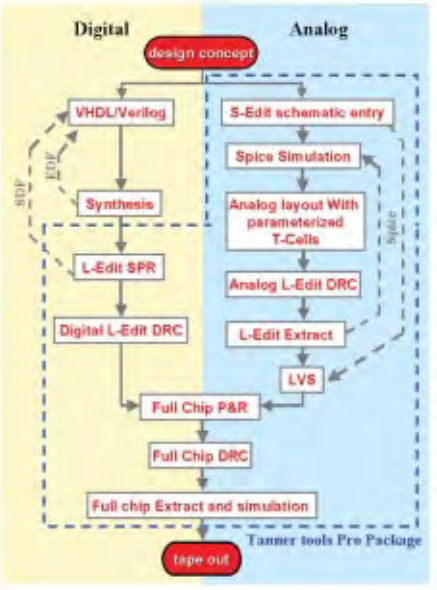


**Figure 2**

(E2PROM) can be used as configuration memory for the card or as general purpose memory.

The proprietary Data Download mode provides a more direct interface to the E2PROM, simplifying access by the add-in card's controller or Application-Specific Integrated Circuit (ASIC). Designing such a highly integrated mixed-signal IC requires hierarchical design tools that are not only very accurate and powerful, but also compatible with the foundry, in order to reduce the number of prototypes and shorten the time to market.

## Complete design suite solution

Tanner EDA was able to meet Summit Microelectronics' needs for the SMH4044 with its Tanner Tools Pro package. The package provides a seamless design flow to integrate the analog blocks with the digital blocks in a mixed-signal chip (see Figure 2).

The Tanner Tools Pro package enhances the accuracy of the manual analog block layout creation by implementing parameterized cells (T-Cells). T-Cells provide the ability to create parameterized cells based on user-written C-language code. With T-Cells, a designer can create versatile source cells that consist of user-defined input parameters and layout-generating code, as well as optional fixed geometry. Once created, T-Cells can be instanced using a simple dialog to enter parameters that are used to run the layout generation code. They can also be used to place an instance into the design.

The package also includes a device layout generator (DevGen), which is utilized for devices such as MOSFETs, resistors, inductors, and capacitors. The DevGen features a user-friendly interface and powerful device variation capabilities, which allows mixed-signal design engineers to streamline processes when they create off-the-shelf device layouts.

The SMH4044 design was done using the Tanner Tools Package in L-Edit (as shown in Figure 3). The SMH4044 was implemented in 0.8u 2p/2m Chartered Semiconductor process and quickly found its share in the CompactPCI market.

## Conclusion

Tanner EDA has delivered an enhanced design tool package, Tanner Tools Pro, which features all the necessary modules and meets the requirements for mixed-signal design. Summit Microelectronics successfully used this design package to create the hot-swap controller IC, SMH4044. Tanner Tools Pro is an advanced Windows-based design flow tool, available at a fraction of the price of other solutions.

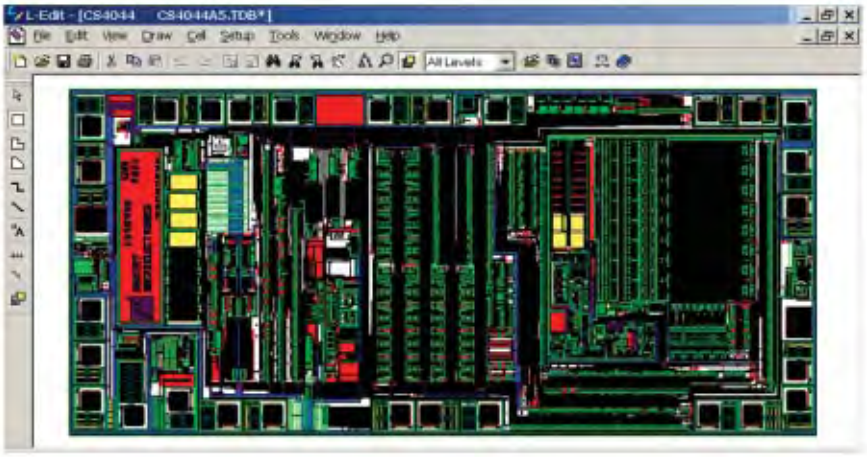


**Figure 3**

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