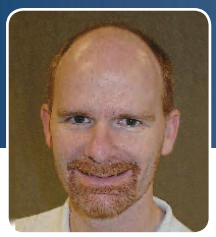

IP vendor offers voice over packet application platforms

The trend toward integrated software capabilities and programming interfaces for hardware platforms has found its way into System-on-Chip (SoC) design. For example, CEVA, an intellectual property company licensing DSP technology to a number of companies in a variety of markets, has recently introduced a Voice over Packet (VoP) application environment called CEVA-VoP. Interestingly enough, the core to this application platform is not a board-level design. Instead, the core of the application environment leverages CEVA DSP core intellectual property to create SoC designs targeted for items from IP phones and dual mode cellular over Wi-Fi products, to larger products such as home gateways and Voice over Internet Protocol (VoIP) broadband equipment. I recently had the opportunity to talk with Moshe Sheier, spokesperson for CEVA-VoP. We talked about how software trends are influencing SoC providers such as CEVA and new software and application innovations from CEVA to address these demands.

VoP platform overview

CEVA is a licensor of DSP cores with more than 115 million chips shipped with CEVA cores in 2005. Their DSP cores are widely used in cellular, DVD, disk drives, and consumer electronics.

In addition to a large portfolio of DSP cores and related subsystems for SoC products, CEVA has added platforms in multimedia, audio, GPS, and storage solutions.

One of those platforms is the CEVA-VoP platform. The product is a fully integrated, single DSP-based VoP system ready for integration into SoC designs. There are four main components to the platform:

- SoC and software interface framework
- Hardware
- Software
- Toolset

The hardware platform itself is available in two different configurations: *voice processor* configuration and *voice + networking processor* configuration. The voice processor configuration supports up to eight channels of G.729AB voice, telephony, or packetized data with tasks that interface with a host processor. This configuration is targeted for applications that will use a network processor function as the incoming/outgoing network interface and a host processor to provide signaling and management functionality. The *voice + networking processor* configuration provides a solution that can offload or even eliminate the need for host and network processing functions, which can dramatically reduce the cost of gateway and VoIP phone applications at the cost of fewer payload processing channels provided by the voice processor configuration.

The software solutions with the platform include:

- ITU-compliant G.7xx suite of voice encoder/decoder algorithms and echo cancellation (G.168-2000) for the DSP core
- UDP/IP stack network protocols
- Real-time Transport Protocol (RTP) packetization
- Operating kernel used as the framework for the software
- Session Initiation Protocol (SIP) signaling stack

These components work together to provide network interface, signaling, and content processing functions for the platform.

VoP: A closer look

Figure 1 shows the CEVA-VoP platform architecture. The blocks in light blue are the voice plus networking components. The blocks in the dark blue are the voice processing components, and the green blocks represent the external interfaces.

The two external interfaces are the network interface itself, which is an Ethernet MAC connected to a LAN either directly or through a Layer 2 switch. The other interface is the Subscriber Line Interface Circuit (SLIC), which carries the Time Division Multiplexed (TDM) channels between the application platform and the ultimate input/output destination(s) of the payload carried within the channels.

The VoIP circuit and software is designed to handle up to eight channels of G.729AB voice codec channels simultaneously at a power of approximately 20 mW. More specifically, each channel consumes 0.1 mA/MHz per channel.

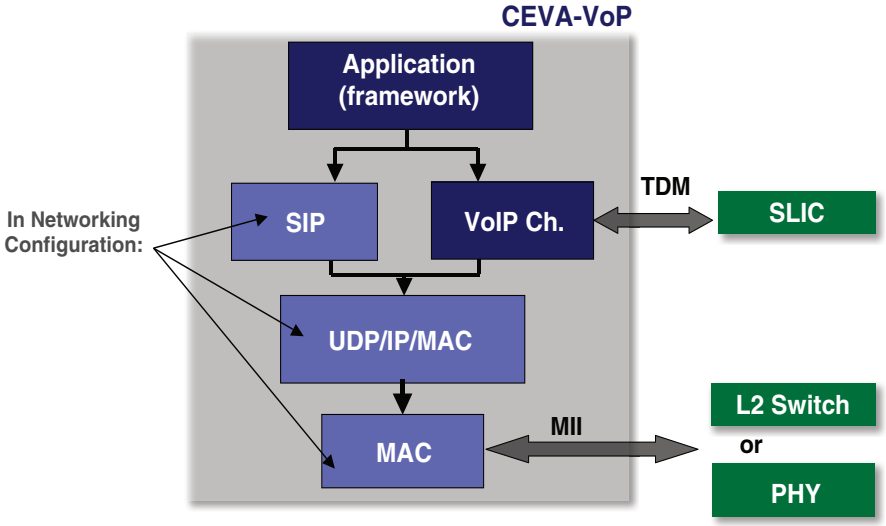

Figure 1

With each channel operating at 25 MHz multiplied by eight channels, that totals 20 mW. Within the voice-only engine configuration, the system can be set up to provide eight G.729AB voice channels with telephony and RTP processing. Another common configuration includes six G.729AB channels with two T.38 fax channels in addition to the telephony and RTP processing.

The voice plus networking engine provides the same configuration, but adds UDP/IP and SIP signaling to the configuration. The additional network and signaling processing will limit the number of channels that can be supported. Exactly how many channels are supported depends upon the application's call setup-per-second characteristics as well as the amount of UDP/IP traffic coming into the system.

The application software framework provides a set of application programming interfaces to configure the voice processing in addition to getting basic statistics and signaling control interfaces to the environment. The framework is written in C/C++ and can be ported to the host processor's operating system environment.

SIP signaling and UDP/IP packet processing functions can also be performed within the environment if a front-end network processor and/or a host processor is not needed for the application. This increases the processing and bandwidth utilization on the DSP, so fewer channels are supported, but at the same time, the SoC subsystem becomes quite a combination networking, signaling, and voice processing machine.

The uniqueness of SoC

One of the things I found fascinating while talking to Moshe about the CEVA-VoP platform is the range of software and tools support needed to provide a SoC application environment for today's customers. The software ranges from C/C++ programming interfaces, signaling, and networking software to DSP assembly codec and payload processing and verilog for the DSP and component subsystems themselves. Therefore it's no small undertaking to provide a fully validated and integrated SoC solution.

Starting with the silicon intellectual property, the CEVA-VoP hardware intellectual property package contains the following elements:

- Fully verified synthesizable verilog code
- RTL to GDSII complete and robust design flow with scripts for mainstream EDA tools
- Verification and simulation environments for verification of the IP integration in the target SoC
- RTL on FPGA for system prototyping prior to silicon fabrication

The IP integrator combines the top level CEVA-VoP verilog block into the SoC design, while using the AHB/APB bus interfaces to connect to the host CPU and system memory, and on the other side the TDM ports to the subscriber line interface (SLIC/SLAC) modules and into the RJ-11 telephony ports. The integrator uses supplied test suites to validate the IP integration following completion. Once validated, the physical implementation (synthesis and place and route) is initiated to form the complete GDSII view for fabrication.

VoP development environment

Figure 2 shows all the different kinds of languages and environments that go into the single Integrated Development Environment (IDE). The myriad of tools and capabilities under one integrated environment allows complete software development from verilog integration, DSP algorithms, and C/C++ interface library interfaces for the platform.

> "The voice + *networking processor* configuration provides a solution that can offload or even eliminate the need for host and network processing functions..."

The set of DSP algorithms includes:

- Voice encoding and decoding for G.711 64 kbps A-law/m-law Pulse Code Modulation (PCM)
- G.726 40/32/24/16 kbps ADPCM
- G.729A/AB 8 kbps CS-ACELP
- G.723.1/A 6.4/5.3 kbps MP-MLQ/ ACELP

An adaptive low delay jitter buffer helps minimize data loss and delay through the platform. There is also a unique three-way conferencing capability in the algorithm that allows mixing of two audio sources on one side into one combined signal on the other side.

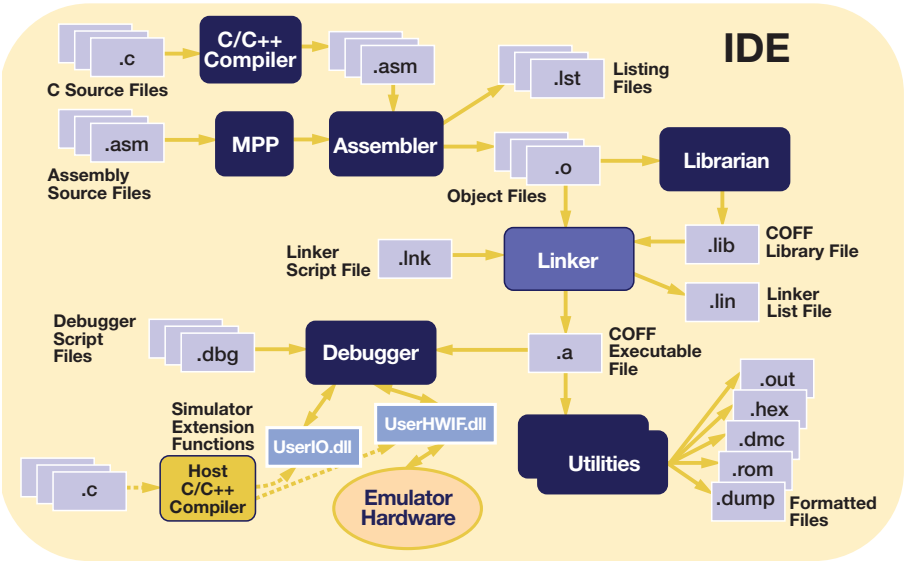

Figure 2

Telephony features include:

- Tone generation and detection
- Fax/modem detection
- Automatic volume level control
- Caller ID
- Call waiting
- Error mitigation/bad frame interpolation
- Host and TDM interfaces drivers

The CEVA software development tools consist of an IDE, a C/C++ Compiler, macro preprocessor, assembler, linker, debugger, and several utilities. They aim to provide an efficient, user-friendly environment for application development. The development tools run on Windows, Linux, and Solaris platforms. The macro preprocessor, assembler, Linker, and C/C++ Compiler are part of the code generation tools, as they build executable code from either C source code or assembly source code.

Once the code has been developed, the IDE includes a graphical debugger as well as simulation. The GUI debugger supports generation and execution for command line and TCL scripts. The debugger can interface to popular verilog simulators as well as emulator interfaces through USB or JTAG ports.

The entire IDE, simulators, and profilers for the DSP software are implemented in C/C++. Low-level DSP assembly with C/C++ level APIs are also provided for external software interface. Moshe mentioned that development tools and an integrated environment are key to the development and customer selection process, so CEVA has developed all its tools internally. The benefit of this approach is that the tools can be tuned for their intellectual property and target applications.

Once the code is developed and debugged using the debugging and simulation environments, an application profiler is also provided to determine performance metrics for the application.

Control and management plane considerations

Typically, the CEVA VoP platform might be integrated with SIP signaling and network management software such as Simple Network Management Protocol (SNMP) to provide an SNMP-managed device. These components would typically run on a separate control and management plane processor and use APIs to communicate to the VoP platform components as well as gather statistics. These functional APIs include things such as call initiation and termination, opening packet streams, specifying DMA channels and memory locations for each voice circuit, and control activities relating to the SIP call control protocol.

We also talked a bit about the Communications Assistance for Law Enforcement Act (CALEA). This involves VoIP systems' ability to support lawful surveillance for law enforcement and homeland security. Similar to the control and management plane functions, these activities would also be controlled from a separate host processor and control the routing of the voice channels through the APIs provided.

Conclusion

SoC designs require a wide variety of software from verilog to assembly, to C/C++ and Java in order to achieve the integration level today's multimedia applications demand. The CEVA-VoP platform is a good example of the next generation of integrated hardware and software intellectual property solutions supplied for the creation of these kinds of applications. Targeted at home gateway (two to eight channels) as well as VoIP phones (voice and cellular over Wi-Fi), it also provides a good example of the flexibility that must be incorporated into a successful SoC platform.

For more information, contact Curt at cschwaderer@opensystems-publishing.com.