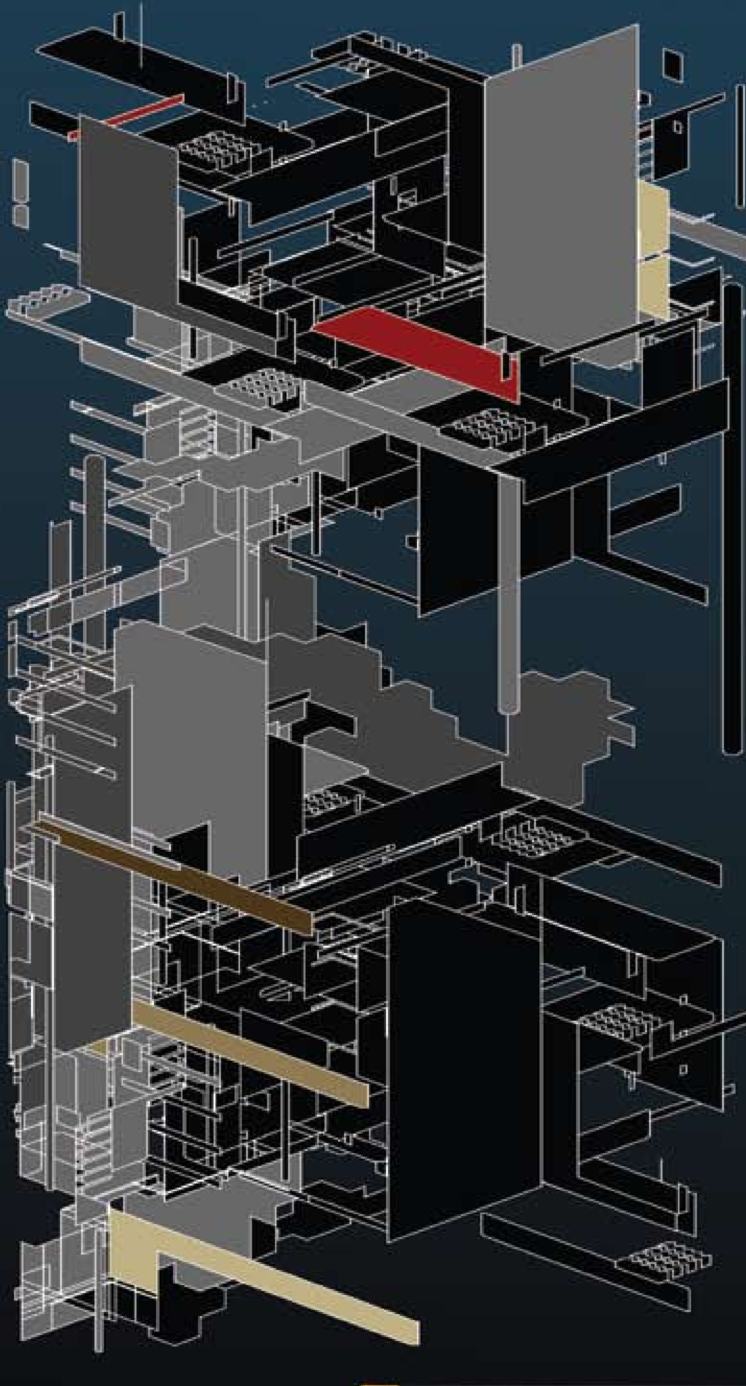
Embedded COMPUTING DESIGN

www.embedded-computing.com

MARCH 2009 VOLUME 7 NUMBER 2



Integrated platforms:
Adding value layer by layer

2009 Components Resource Guide

SPECIAL

INCLUDED WITH THIS ISSUE:

MOXA

Ready-to-Run Embedded Software Platform

www.opensystemsmedia.com

With a wealth of onboard I/O plus expansion options, the EPX-855 supports Linux, Windows® XP embedded, and other x86 real-time operating systems.

- Intel® 1GHz CPU (fanless) or optional 1.8GHz Pentium® M
- Intel® Extreme Graphics 2 technology supports CRT and LVDS flat panels simultaneously with dual independent display and resolutions up to 2048 x 1536
- 802.11 a/b/g wireless support
- Custom splash screen on start up
- Two Ethernet ports; one Gigabit and one 10/100Mbps
- CompactFlash (CF) card supported
- Four serial COM ports, four USB 2.0 ports, 24 bi-directional TTL digital I/O lines, and two UDMA IDE ports
- Bi-directional LPT port, keyboard controller, FDC, and AC97 audio
- PC/104 and PC/104-*Plus* Bus expansion
- EPIC sized 4.5" x 6.5" and RoHS compliant
- +5V only operation
- -40°C to +70°C operational temperature range
- Responsive and knowledgeable technical support
- Long-term product availability
- Quick Start Kits offered for easy software development

Contact us for additional information or OEM pricing. Our helpful and knowledgeable factory application engineers look forward to working with you.

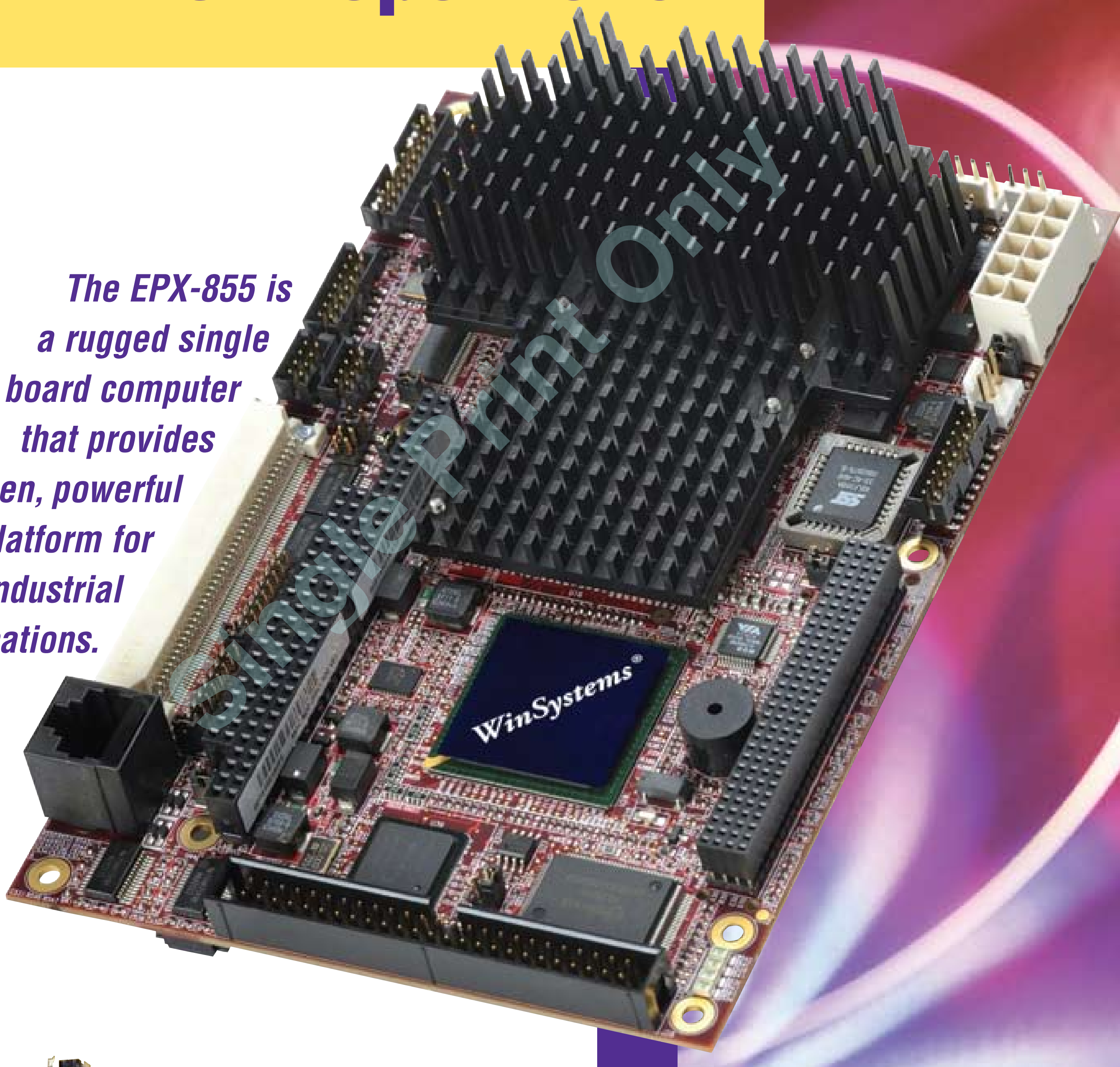
Call 817-274-7553 or
Visit www.winsystems.com/EPX-855
Ask about our 30-day product evaluation

WinSystems®
An Employee-Owned Company

715 Stadium Drive • Arlington, Texas 76011
Phone 817-274-7553 • FAX 817-548-1358
E-mail: info@winsystems.com

A 1GHz Fanless Industrial SBC of *EPIC* Proportions

The EPX-855 is a rugged single board computer that provides an open, powerful platform for industrial applications.



Windows® and Linux Quick Start Kits available.

Embedded COMPUTING DESIGN

Volume 7 • Number 2 www.embedded-computing.com

Columns

8 Editor's Foreword
Is now the time to invest in tools?
By Jerry Gipper

10 Technology Passport
Look Ma, no driver
By Hermann Strass

12 Consortia Connection
Smart standards for wireless technologies

14 Ingenuity @ work
Simplified HMI development

Departments

52 Editor's Choice Products
By Jerry Gipper

Resource Guide

Design aids 34
Interfaces 35
Microcontrollers and processors 36
Power management 39
Programmable logic 40
Software 47

Cover/Web Resources/Events

On the cover

Platform-Oriented Architectures (POAs) can be packaged in layers, making systems integration easier. Check out the Special Feature starting on page 16 for more information on how POAs can help resolve design challenges.

E-casts

Register at: www.embedded-computing.com/ecast

What makes a Real-Time OS indispensable?
March 12, 11 a.m. EDT

Embedded multicore system development fundamentals
March 12, 2 p.m. EDT

E-letter

www.embedded-computing.com/eletter

PCIe Gen 2: Not just more bandwidth
By Touseef Bhatti, PLX Technology

Web Resources

Subscribe to the magazine or E-letter at:
www.opensystemsmedia.com/subscriptions

Read industry news at:
www.embedded-computing.com/news

Submit news releases, new products, white papers, and videos at:
submit.opensystemsmedia.com

Events

Multicore Expo
March 16-19 • Santa Clara, CA
www.multicore-expo.com

Embedded Systems Conference Silicon Valley
March 30-April 3 • San Jose, CA
http://esc-sv09.techinsightsevents.com

Features

Special Feature
16 What's in your platform?
By Jerry Gipper

Chip and board debugging
22 Protocol analyzers simplify USB debugging
By Etai Bruhis, Total Phase

Core IP licensing
26 Software Bill of Materials improves Intellectual Property management
By Mahshad Koohgoli, PhD, and Sorin Cohn-Sfetcu, PhD, Protecode

Programmable logic
28 The high price of low-cost FPGA development boards
By Rob Evans, Altium Limited

Software
32 Trends are good for press, not necessarily for sockets
By Jean J. Labrosse, Micrium

Embedded COMPUTING DESIGN

OpenSystems media.

VME and Critical Systems · Embedded COMPUTING DESIGN · DSP-FPGA.com · INDUSTRIAL EMBEDDED SYSTEMS · Military EMBEDDED SYSTEMS · PC/104 and small form factors

Embedded and Test & Analysis Group

Jerry Gipper, Editorial Director
jgipper@opensystemsmedia.com

Don Dingee, Contributing Editor

Jennifer Hesse, Senior Associate Editor
jhesse@opensystemsmedia.com

Hermann Strass, European Representative
hstrass@opensystemsmedia.com

David Diomede, Art Director

Steph Sweet, Creative Director

Konrad Witte, Senior Web Developer

Joann Toth, Senior Designer

Monique DeVoe, Copy Editor

Phyllis Thompson
Circulation/Office Manager
subscriptions@opensystemsmedia.com

Sales Group

Dennis Doyle, Senior Account Manager
ddoyle@opensystemsmedia.com

Tom Varcie, Senior Account Manager
tvarcie@opensystemsmedia.com

Doug Cordier, Account Manager
dcordier@opensystemsmedia.com

Andrea Stabile
Advertising/Marketing Coordinator
astabile@opensystemsmedia.com

Christine Long, Digital Content Manager
clong@opensystemsmedia.com

International Sales
Dan Aronovic, Account Manager – Israel
daronovic@opensystemsmedia.com

Sam Fan, Account Manager – Asia
sfan@opensystemsmedia.com

Regional Sales Managers
Ernest Godsey, Central and Mountain States
egodsey@opensystemsmedia.com

Barbara Quinlan, Midwest/Southwest
bquinlan@opensystemsmedia.com

Denis Seger, Southern California
dseger@opensystemsmedia.com

Sydele Starr, Northern California
sstarr@opensystemsmedia.com

Ron Taylor, East Coast/Mid Atlantic
rtaylor@opensystemsmedia.com

Reprints and PDFs

Nan Lamade
800-259-0470
license@opensystemsmedia.com

Editorial/Business Office

16626 E. Avenue of the Fountains, Ste. 203
Fountain Hills, AZ 85268
Tel: 480-967-5581 ■ Fax: 480-837-6466
Website: www.opensystemsmedia.com

Publishers: John Black, Michael Hopper, Wayne Kristoff

Vice President Editorial: Rosemary Kristoff

Vice President Marketing & Sales:
Patrick Hopper
phopper@opensystemsmedia.com

Business Manager: Karen Layman

ISSN: Print 1542-6408, Online 1542-6459

Embedded Computing Design is published 8 times a year by OpenSystems Media LLC, 16626 E. Avenue of the Fountains, Ste. 203, Fountain Hills, AZ 85268.

Subscriptions are free to persons interested in the design or promotion of embedded computing systems. For others inside the US and Canada, subscriptions are $56/year. For 1st class delivery outside the US and Canada, subscriptions are $80/year (advance payment in US funds required).

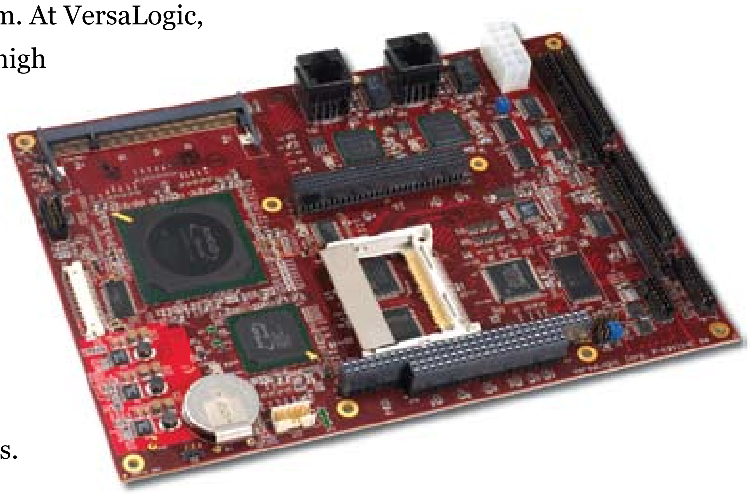
Canada: Publication agreement number 40048627
Return address: WDS, Station A, PO Box 54, Windsor, ON N9A 615

POSTMASTER: Send address changes to ***Embedded Computing Design***, 16626 E. Avenue of the Fountains, Ste. 203, Fountain Hills, AZ 85268

You design products that enhance the quality of life.

Our products help you do it.

One of the most important decisions a medical OEM makes is their choice of an embedded computer. It's at the heart of any system. At VersaLogic, we design our embedded computer products to ensure high reliability and long-term availability. That's why our single board computers can be found in a long list of medical products. And because we understand that medical customers have special requirements, every board we make is run through exhaustive quality tests, ensuring that we deliver only the best. Whether you need one of our standard products or a version customized to your needs, our skilled technical staff will work with you to meet your exact specifications.



Contact us to find out how for more than 30 years we've been perfecting the fine art of extraordinary support and on-time delivery: One customer at a time.

1.800.824.3163
1.541.485.8575
www.VersaLogic.com/ECD

VersaLogic Corporation

Editor's Foreword

Jerry Gipper

Is now the time to invest in tools?

Determining when you should invest in development tools is often a hard decision to make, especially during an economic recession. Yet it is still a decision that needs to be made.

During boom times, the push to get more done is commonly addressed by throwing more human resources at a design task, with managers asking for more engineers to keep projects on schedule. Investments in development tools and new processes take a backseat. These investments meet resistance because design teams don't have the luxury of taking time to investigate toolset options or to learn a new tool suite and processes. They are focused on getting the project out the door on time.

During economic declines, resources are stretched as companies make cutbacks in staff and spending. Getting sign-off on new development tools is not likely to get any attention while projects fall behind.

Several studies illustrate the benefits of using advanced development tools such as simulators, Model-Driven Development (MDD) tools, and other electronic design automation tools. How much time and money can be saved varies, but most reports reach the conclusion that definite savings can be achieved. A December 2008 report titled "The Economics of Embedded Development, Testing, Deployment, and Support" by Embedded Market Forecasters (www.embeddedforecast.com) presents an example that shows how companies can attain project improvement approaching 30 percent. There is no question that good, solid development tools can reduce development cycle times, shorten time to market, and improve the quality of your product.

> Don't let price be the sole driver. Sometimes the best tools are inexpensive; other times, "you get what you pay for" applies.

Selecting the right solutions is another story. Development tools come in all types, from simple and basic to very complex and robust. You must clearly understand each tool and how it will work in your design environment. The often inexpensive entry-level tools might not have the right sets of features. For instance, a low-end MDD tool might not provide validation or traceability to your requirements, reduce programming errors or test time, or improve the quality of the final product as expected.

On the other hand, deluxe tools can be overkill, with features that are not necessary for your development environment or that are so complicated that they are difficult to learn or use.

Don't let price be the sole driver. Sometimes the best tools are inexpensive; other times, "you get what you pay for" applies. You should employ an in-house specialist who tracks development tools, someone you can turn to when a decision needs to be made. A readily available expert who fully understands the pros and cons of a tool and can interpret its impact on your organization and projects is hard to come by. Relying on marketing hype and sales pressure can lead you astray.

My belief is that now is the right time to consider investments in upgrading your development tools. You will want to be in a position to recover from this downturn quickly, riding the upslope that will likely occur in the coming months.

With the right investment, you could save 25-30 percent on your next project, reduce time to market, meet schedule commitments, and produce better design results.

As you eventually start restaffing, look for engineers who are competent and skilled in using these new tools. Underemployed engineers should take advantage of this time to learn new tools, making them more marketable assets to the companies that will emerge out of this recession.

Feel free to share your comments through e-mail or visit our blog at www.embedded-computing.com to add your comments.

Jerry Gipper
Editorial Director
jgipper@opensystemsmedia.com

Technology Passport

Hermann Strass

Look Ma, no driver

Automated system secures subway

The city of Nuernberg is a pioneer in industrial technologies. In 1835, the first scheduled train service in Germany traveled between Nuernberg and the neighboring city of Fuerth. Last June Nuernberg launched the U3 line, Germany's first subway line to use driverless trains as well as the world's first underground metro to run both automated and conventionally operated trains over the same tracks. Figure 1, courtesy of Siemens, shows the U3 line on opening day.

Figure 1 | The U3 line in Nuernberg uses driverless trains.

Other driverless subway systems, such as the automated people mover at the airport in Atlanta, Georgia, control access using platform doors aligned with train car doors that always open on the same side in each direction of travel. In the Nuernberg system, cars are coupled and trains are switched automatically. Every inch of the railway track is monitored to detect objects.

Transit authorities typically equip automated subways with doors that block the dangerous area at the edge of the platform until the train stops. This wasn't possible in the U3 line because of its mixed automatic/manual operation and curved platforms.

To ensure safety, the U3 system uses video monitoring and a dense grid of sensing beams over the tracks near the platform edge. If a person or object falls onto the track or between cars, the system immediately halts all trains in the area. Solid sills extend from doors when a train is stopped to prevent objects from getting caught in the gap between the train and the platform. Sensors in the rubber edges of the doors register even the slightest pressure. The hem of a coat stuck in the door is all it takes to keep the train from leaving the station.

The control center monitors the train car interior via video cameras. Passengers who activate an alarm are automatically connected with the control center through digital voice radio. The automated system does not require traditional mechanical or electrical signals along the tracks.

Embedded computers steer trains

An Automatic Train Control (ATC) system from Siemens controls the U3 trains' movements and operates the signal boxes. These trains contain onboard embedded computers that continually exchange data with the higher-level control system. Data includes the destination and speed of each train, track switching information, and the side of the train that will face the platform at the next station. While one onboard computer uses data from the ATC to control the driving process, a second computer monitors the actions of the first and makes corrections if necessary.

The ATC system can monitor and control train movements autonomously. All control systems are connected in a triple redundant voting configuration, meaning that all trains are allowed to run as long as two computers provide identical results. If not, the system immediately halts the trains and central control takes over operations. Objects blocking the doors have presented the greatest problem thus far.

The U3 trains travel at an optimal speed in accordance with the timetable and distance between stations. Other benefits of the driverless system include shorter train intervals of 100 seconds instead of 200 seconds and the ability to quickly dispatch additional trains for major events. The centralized automated subway is more energy-efficient and safer than driver-operated systems.

The Georg Simon Ohm University of Applied Sciences in Nuernberg is working on a decentralized system for driverless subway operation. Other driverless subway lines are currently under construction in Barcelona, Spain; Uijeongbu, Korea; and other cities around the globe.

Our Advanced Managed Platforms™ will take you there!

Design challenges today are more acute than they were just a year ago. At Performance Technologies, we understand these challenges. Our Advanced Managed Platforms™ provide flexible and scalable solutions for MicroTCA™ and CompactPCI®. These pre-integrated hardware and software platforms enable you to reduce development costs and improve time-to-market while advancing your product design initiatives.

We are the only company that can offer you both pre-integrated embedded hardware and a CGL Registered 4.0 Linux®, with our NexusWare® suite of software.

So the next time you need a ready-to-develop solution, call Performance Technologies and discover how our Advanced Managed Platforms™ can meet your design challenges.

Flexible MicroTCA™ Platforms

Carrier Grade Linux® NexusWare® OS

Scalable CompactPCI® Platforms

PERFORMANCE TECHNOLOGIES

Phone: 585.256.0200 ◆ www.pt.com ◆ E-mail: info-request@pt.com

Consortia Connection

Smart standards for wireless technologies

IPSO Alliance

www.ipso-alliance.org

The IP for Smart Objects (IPSO) Alliance promotes the concept that Internet Protocol (IP) is the networking technology best suited for connecting sensor-equipped devices – referred to as *smart objects* – and delivering information gathered by those objects. Smart objects transmit information about their condition or environment (for example, temperature, light, motion, and health status) to locations where that information can be analyzed, correlated with other data, and acted upon. These objects are used in automated homes and offices, factory automation, asset tracking, patient monitoring, industrial and safety systems, and many other applications.

"More and more utilities and OEMs are viewing embedded IP as the long-term solution and proprietary approaches and *ad hoc* alliances as merely an interim step," states Geoff Mulligan, IPSO Alliance chairman. "They are recognizing that only IP can support a wide variety of networking technologies with the needed scalability and interoperability that organizations require."

The IPSO Alliance is planning three large-scale interoperability test events in 2009, the first of which will test end-to-end IP-based interoperability across the Internet by employing the next-generation IPv6 protocol over local and wide area communication media. The event will demonstrate open standards-based sensor networking solutions that deliver the global scalability, security, performance, and flexibility needed for future applications.

Other events later in the year will include demonstrations of multivendor devices communicating within a sensor network using the Internet Engineering Task Force 6LoWPAN (RFC 4944) standard for IPv6 over low-power wireless personal area networks. Each subsequent test will increase the scope of vendors and the diversity of interoperating media types including IEEE 802.15.4, Wi-Fi, Ethernet, and WiMAX.

ZigBee Alliance

www.zigbee.org

The ZigBee Alliance, a global ecosystem of companies creating wireless technologies for use in energy management, commercial, and consumer applications, finished 2008 with more than 300 members. Utilities across the United States and Canada have validated ZigBee Smart Energy as the leading wireless standard for implementing home area networks in conjunction with Smart Grid initiatives.

"When you consider that already more than 25 million homes in North America will be outfitted with a smart meter equipped with ZigBee with more on the way, the opportunities for our members to provide consumers with more control of their lives are incredible," asserts Bob Heile, chairman of the ZigBee Alliance. "Consumers will remotely control their homes and manage their energy use thanks to ZigBee Smart Energy's inherent Internet connectivity."

The ZigBee Smart Energy profile was ratified in May 2008 and made publicly available in June. Utilities and consumers can select from 20 ZigBee Smart Energy Certified products representing a range of devices for managing home energy consumption including electricity meters, thermostats, and in-home displays.

In February the ZigBee Alliance and the HomePlug Powerline Alliance announced that they are joining forces with the Electric Power Research Institute to develop a standard communication approach for home area networks to use advanced metering infrastructure. The initiative will provide the flexibility for utilities to integrate ZigBee and HomePlug devices when implementing smart metering programs as well as expedite the rollout of energy management and efficiency programs to consumers.

Ingenuity@work

Simplified HMI development

problem

Designing Human-Machine Interfaces (HMIs) is becoming a significant challenge for designers. Embedded devices are shrinking in size, making it difficult to develop useful and intuitive HMIs with the right combinations of features in a short time-to-market window.

solution

Software tools can help manufacturers build user interfaces at a high level using programs like Photoshop for graphics and Visio for screen flow. Developers can then integrate those pieces of technology into actual code that can run on the device itself.

Converting creativity into code

This decade has seen dramatic improvements in display technology, generating an explosion of uses for graphics displays in desktop, workstation, and embedded systems. From in-car navigation systems, mobile phones, and portable MP3 players to airports and power plants, flat-panel displays are showing up everywhere. Consequently, the HMI has emerged as a critical product differentiator that provides a window into an array of powerful product features.

Although display technology has improved dramatically, HMI software development has lagged behind, producing many abysmal user interfaces. This delay can be attributed to today's complex, programmer-centric HMI tools, which discourage the participation of the graphic artists, industrial designers, and application experts needed to develop effective user interfaces. Furthermore, because today's devices come with custom processors and/or Operating Systems (OSs), building user interfaces requires special skills and knowledge.

To aid designers in this difficult task, Altia provides cohesive, easy-to-use HMI development tools that wrap high-level modeling and graphical tools around detailed custom programming. The tools hide the processor from developers so they can focus on their applications. A code generator produces code for the chosen processor architecture, and everything from graphics to logic gets used and reused.

Quick facts

Altia, Inc.
Founded: 1991
Management: Michael Juran, CEO
Headquarters: Colorado Springs, CO
URL: www.altia.com

Altia helps bridge the gap between the widely dissimilar needs of the creative process and the programming process. The company's tools assist artists by providing a WYSIWYG graphics and HMI editor that allows them to draw and import graphics from their favorite graphics design tools. The software likewise aids programmers by providing code generators, language translators, APIs, and OS-specific graphics libraries that convert the artist's HMI design into deployable code that can be integrated with the programmer's application code and run on a variety of OSs and hardware.

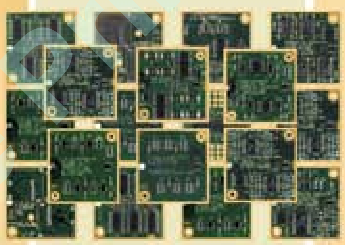
Create Your Own PMCs

Custom I/O as Easy as 1, 2, 3!

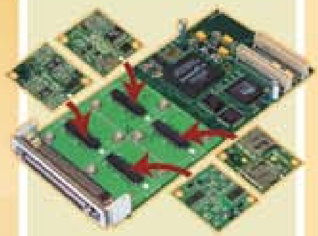
The Technobox ***Micro Mezzanine System***™ is based on a simple idea – provide embedded systems designers with a foundation for innovation and flexibility. Provide a highly-granular, modular architecture featuring a range of configurable FPGA-based carrier boards and an extensive variety of micro mezzanine Electrical Conversion Modules (ECMs) that can be assembled in thousands of combinations. Provide an environment in which a designer can create an array of unique, *future-proofed*, board-level solutions. But without the costs normally associated with custom board development and manufacture, while speeding development and reducing time to market. It's the logical next step in mezzanine systems.

1 Select an FPGA-based Carrier

2 Choose I/O Conversion Modules



3 Assemble with IP Core and ECM Code



Patent Pending

- ***Build Your Own Board by Mixing and Matching Modular Components***
- ***Thousands of Possible Combinations***
- ***Flexible, FPGA-based, Patent-pending Architecture***
- ***Incorporate Multiple Functions on a Single Board***
- ***Design and Build Application-specific, Future-proofed Solutions***
- ***Accelerate System Development, Reduce Time to Market***

To learn more about the Technobox Micro Mezzanine System, visit:

www.technobox.com/mmsintro-fp.htm

Technobox, inc.®

Micro Mezzanine System

What's in your platform?

By Jerry Gipper

Designing embedded computer systems is always difficult. Innovative technologies with increasing performance levels and smaller packaging present new obstacles every day. Fortunately, suppliers are making design easier by promoting the concept of a Platform-Oriented Architecture (POA), which provides a way to move up the supply chain and make the design and integration efforts go more smoothly. Just as politicians use their platforms to kick-start their programs, POAs provide a launching pad for embedded devices. So the question is, what should you know about platforms before starting your next project?

"In today's challenging business environment, developers are looking for ways to reduce cost through extensive software reuse and by leveraging turnkey platforms that combine best-of-breed hardware and software." – Tony Massimini, chief of technology, Semico Research Corporation

POA defined

The definition of Platform-Oriented Architecture varies slightly from software to chips to boards to systems, but the concept remains the same. It is a bounded and integrated suite of components consisting of either or both software and hardware optimized to enable further integration into a final product for a specific application. Advanced platforms combine hardware and associated software designed to serve as the basis for a number of different systems to be integrated. Many other devices – Systems-on-Chip (SoCs), Application-Specific Standard Products (ASSPs), SBCs, and systems in a variety of combinations – are now considered platforms.

"The ultimate Platform-Oriented Architecture is an FPGA because you can do anything with it," asserts Craig Rawlings, senior director of product management at Certicom. "The idea of doing something universal is a pipe dream. But if we bind the problem, then it makes a lot of sense, and you can scope things in a way that streamlines a number of options, plus save on R&D and manufacturing."

How platforms evolved

In the early days of electronics, devices were usually custom-designed for a specific objective. Hardware and software were designed from scratch and took forever to develop. As the market matured, suppliers started to anticipate the needs of developers, but they did so in haphazard ways. They tried to maximize their market coverage and design products that served as many users as possible. General-purpose processors, computer boards, and Real-Time Operating Systems (RTOSs) emerged. Developers had to force-fit or tweak components to meet their specific application requirements.

From Rawlings' perspective, the first POA was really a CPU because it was programmable; you could do anything with it. But microcontrollers were among the first to formally embrace the platform concept. Suppliers would package together the core processor with various configurations of memory and I/O to target specific controller applications such as industrial control or medical devices.

Rawlings speculates that system architects stepped in and said, “Let’s not build an architecture that tries to be everything to everybody.” They proposed building a platform for a PDA or a mobile telephone – something more specific with binded features that are known requirements. Instead of building three chips or boards, designers could build one chip or board with selectable modes that can be turned off and on.

Eventually, suppliers started making alliances with others in the market to provide more complete solutions for embedded systems developers. Early attempts were loose alliances or ecosystems that covered as many of the design bases as possible. This made it easier for developers to get all the right pieces in place, but it still was a long road to product completion. Designers had to contact and work with multiple sources, lacking the assurance that pieces were fully compatible or even available.

These alliances and ecosystems evolved over time. In many cases, the technologies were combined in packages that made the development path smoother and more efficient. Suppliers started talking about moving up the supply chain by offering more complete and integrated solutions. This strategy became even more effective as the electronic hardware and software suppliers began addressing specific application segments. Various hardware and software components were integrated, and the platform concept stuck.

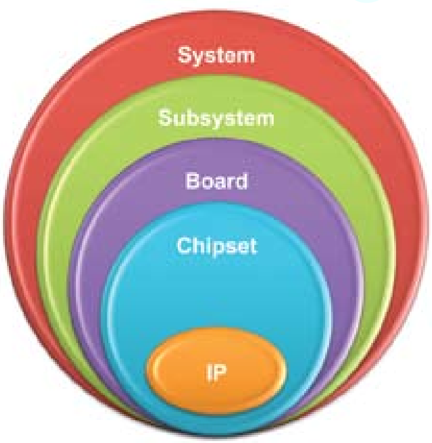


Figure 1 | Like matryoshka dolls, POAs can be nested in different layers, with additional features and value incorporated at each layer.

In time, the PC emerged as a dominant general-purpose platform. However, many embedded applications cannot use a PC platform because they have size, weight, and power restrictions that make it impractical to use a PC. This issue led to the development of platforms that address the specific needs of embedded applications. Functions specific to market applications, from mobile devices to communications infrastructure, were defined and developed.

Platform components

In many ways, POAs are like matryoshka dolls in that they can be nested beginning at the IP layer and moving through to the packaged system level (see illustration in Figure 1). Additional features and value are incorporated at each layer as integration becomes more complex. IP is packaged into a platform that can make integration into a chipset easier; chipsets are packaged into devices that make board design easier; boards are packaged into platforms that make systems integration easier; and systems are packaged in ways that make adding the final layers of value easier.

Chips, boards, and systems

Hardware platforms include the processing element, memory, and user I/O appropriate to certain applications. SoCs are usually targeted at specific applications, making them entry-level platforms by definition. ASSPs are designed for very targeted applications and thus are considered platforms. Add some specific software to support the hardware, and you get an even more robust and complete platform. Semiconductor suppliers often go the next step and develop reference designs that include not only the processor, but also a fabricated board and software package that speeds the use of the product in a final design.

Platforms were mentioned prominently in Xilinx’s recent launch of its Spartan-6 and Virtex-6 products. “We are reaching the tipping point at which FPGAs become the prevailing silicon platform of choice for electronics manufacturers who need customization to differentiate their products but are faced with incredibly unattractive ASIC development costs," remarks Moshe Gavrielov, Xilinx president and CEO. "But in order for customers to increase their adoption of FPGAs, it's essential that we provide a comprehensive design environment that enables global design teams to address the 'programmable imperative' and deliver products faster under these challenging economic and business conditions."

The Xilinx targeted design platform strategy encompasses the integration of five key elements:

- New Xilinx Virtex-6 and Spartan-6 FPGAs
- Design environments supporting and integrating industry-proven methodologies
- Scalable boards and kits adopting the industry-standard FPGA mezzanine connector
- Socketable IP cores
- Robust reference designs

These elements were emphasized as important features in another recent product debut. The CEVA HD-Audio solution is supported by a Software Development Kit (SDK) that includes software development tools, development boards, software system drivers, and an RTOS to enable quick and easy system development and integration. The CEVA-HD-Audio is further complemented by extensive algorithms and applications from a third-party development community.

OSs

OS platforms consist of an integrated suite of modules: the OS, firmware, and device drivers to run the target device's peripherals, file system, libraries, communications protocols for connectivity, and user application. OS suppliers have expanded the integration layer of additional software into their core OSs to incorporate much of the software that makes it easier to focus on the final application. They have continually improved the API, eliminating the need to worry about the routine middleware needed within an industry.

Tools

The platform strategy also applies to development tools. Greg Sykes, director of architecture and modeling at IBM Rational, points out that tools benefit from being packaged into platforms specific to certain market segments. Many companies such as cell phone and automotive manufacturers have their own methods for program management and development. Crafting platforms that conform to a familiar look and feel and providing tools that let designers quickly create modules needed by the application can save significant time in the lab.

The benefits of using a platform

Platforms resolve the problems involved in hardware and software component selection and ease the challenges of integrating and debugging the design, not to mention reduce the hassle of tracking down all the various components needed to develop a complete product. Today, suppliers tend to specialize in facets of the hardware or software needed for an embedded computer system. Because of this specialization, it can be very difficult to chase down remaining components for the final design.

Other suppliers have eased this challenge by integrating the specialized components into a platform. The level of integration can range from simply providing a reference, in which case it probably is not a true platform solution, to a fully integrated and tested configuration. The more integrated the platform, the higher the quality and reliability of the final product, if all goes to plan.

According to Wind River, development tools that are designed and tested with a platform strategy in mind can provide developers with visibility into the entire platform: application code, third-party libraries, and the OS. Developers can monitor variables, optimize performance, and find memory problems – all while the system is still running.

"Increasing competition coupled with challenging economic conditions place further demands on organizations to implement innovative services that reduce costs and streamline operations," states Greg Buzek, president of IHL Group. "By allowing plug-and-play connectivity with peripherals, embedded OSs such as Windows Embedded POSReady 2009 provide the flexibility in system components and software that retailers need, allowing them to lower the cost of ownership and increase efficiencies at the front end."

Targeted POAs help enable software and hardware designers alike to leverage open standards, common design methodologies, development tools, and runtime platforms. This allows designers to spend less time developing application infrastructure and more time building differentiating features into the end application.

Integration

Integration drives many of the other benefits of a platform, making it easier to add and replace components with some level of plug-and-play support. "We do the work of integrating all of this stuff together and making it work for a specific architecture," remarks Dan Cauchy, director of marketing at MontaVista. "In some cases, we write a lot of this stuff ourselves – for example, the porting of the Mozilla browser to ARM."

Cauchy mentions that getting integration to work at a high-quality level requires many staff-years of work. "Device manufacturers are telling us that this is really valuable because they get to start with an entire solution, and on top of that, it is fully supported by MontaVista," he says.

Features and common interfaces

Targeted POAs have the right set of features and interfaces for the target application. The choices have been well thought out and vetted through the target industry. Suppliers need to know their customers' markets to make the right choices.

OS platforms provide a common API, minimizing or even eliminating the need to agonize over hardware. Programmers can write a more generic interface and not worry about the details of the device. On the hardware side, interfaces like Ethernet, USB, CAN, and other application-specific choices are supplied.

IP licensing

As companies have tried to get to market faster and others have attempted to specialize, the use of third-party IP has skyrocketed. This has created a huge hurdle in the form of licensing, which can be very complex and expensive to manage and monitor. Passing the burden of IP management on to the platform supplier can ease this pain.

Inventory

A POA can impact inventory in many positive ways. A well-designed platform can be quickly configured to meet the needs of multiple customers in custom configurations. For instance, a chipset supplier can build a single superset product in mass volumes while enabling specific features on demand as required by each customer. This allows the supplier to forecast an aggregate of parts instead of each individual configuration. This means less inventory, improved operational efficiency, and less price erosion because they are not trying to clear inventory.

Debugging

Using a platform means that all of the modules do not need to be touched when troubleshooting. Platform components usually go through a rigorous debugging process before being deployed in many other related designs by other customers. POAs often have a better debugging interface that can make the whole process easier because it is designed with the complete platform in mind.

Testing

Many interfaces have industry test suites to ensure that the feature operates properly. For example, USB has test suites and compliance testing developed by the USB Implementers Forum. If the platform provider has completed the testing, this eliminates or reduces the need to test to the same level at the next step. In highly complex systems with many interfaces, this can save time and costs.

Standards and the ability to support changing standards

Organizations throughout the embedded community develop and evangelize standards necessary to the success of the industry. Platform suppliers are frequently key members of standards organizations, influencing the direction of the standard and ensuring its successful development. Many standards used in today's embedded devices are new or changing. Platform developers can reduce the burden on the design engineer by keeping track of the latest developments, incorporating them into the platform as they become available. You don't have to track all the nuances, develop solutions, and then figure out how to integrate and test.

Customizing

In reality, device manufacturers always need some level of customization because each device is a bit different. Well-developed POAs leave room for some degree of customization either by the customer or with the help of the platform provider. Many suppliers have design service teams that can be employed to add just the right degree of customization to help your product stick out in the market. Suppliers have the inside advantage because they know the platform well. They use the input they receive from customers when assisting with customization to incorporate additional value in next-generation platforms.

Time to market

Anyone who has ever tried to round up, integrate, and test all the right pieces knows how much time can be saved using a well-developed POA. "It's important for manufacturers to be able to deliver products to market quickly, efficiently, and on budget," states Russell Harris, CEO of MontaVista Software. "By leveraging a platform like Montabello [Figure 2], our device customers can focus on building the best products, not developing a complex software infrastructure. Device manufacturers get a 6-12 month head start on their project, improving time to market and enabling them to realize significant development cost savings."

Lower cost

All of the previously mentioned benefits involve some cost-savings element. Learning how to take advantage of these benefits can maximize your investments.

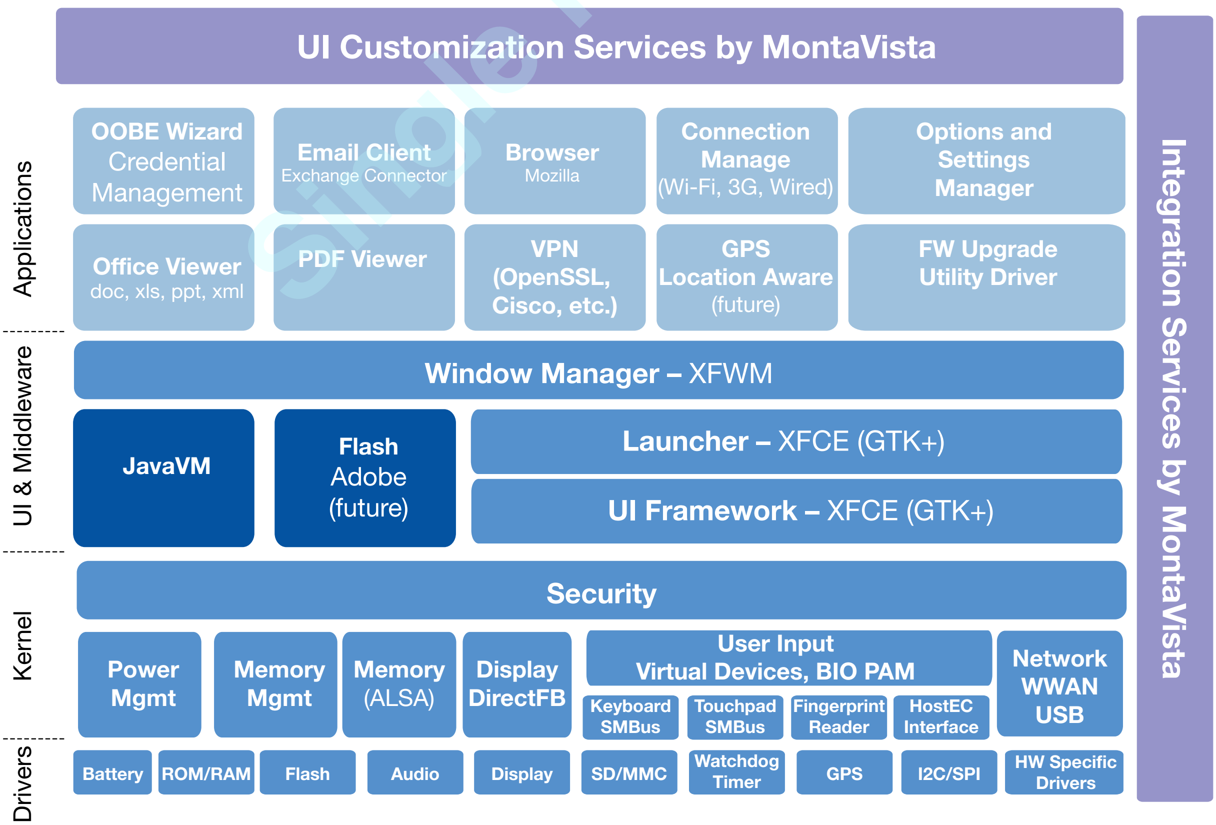


Figure 2 | Montabello is a Linux-based software platform that offers an integrated set of applications for mobile Internet devices.

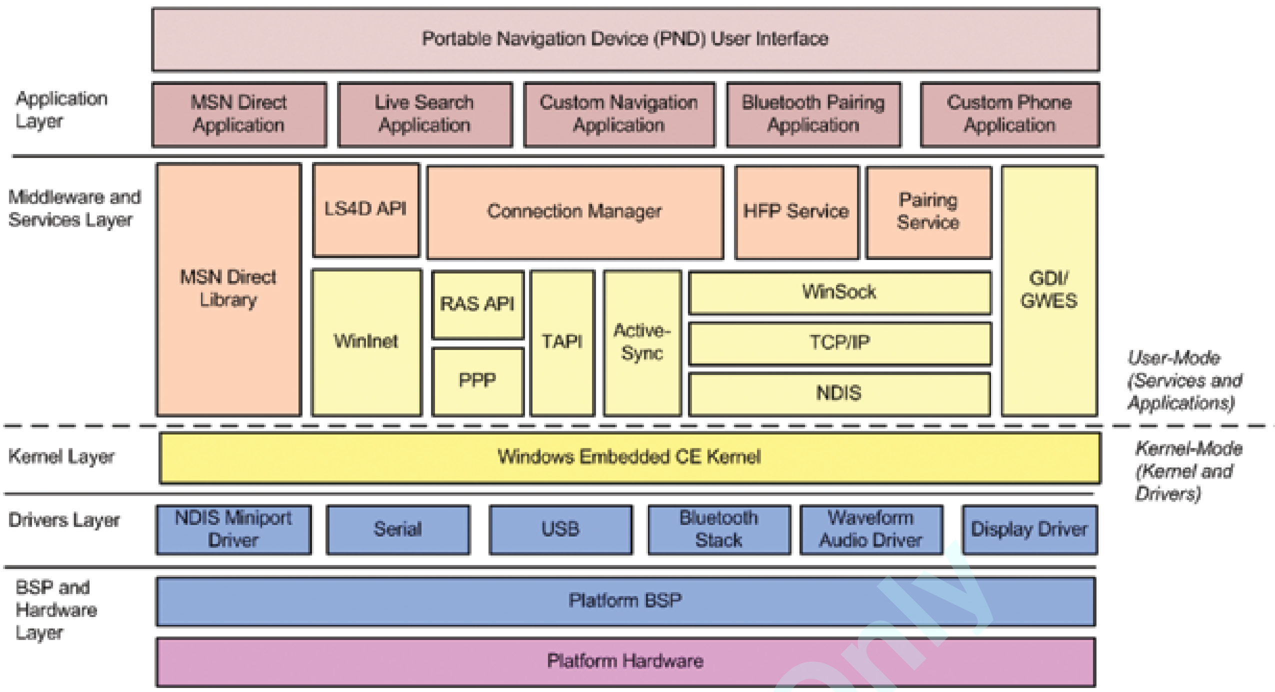


Figure 3 | Windows Embedded POSReady 2009 helps transition Point-Of-Service (POS) systems from transaction processing to enhanced customer service.

Risk management

POAs can significantly reduce risks in your design. Many customers contribute to the platform architecture and expose it to a myriad of testing and usage scenarios that measure the design in ways you may not have considered. The platform supplier provides an additional level of expertise that you can lean on if you run into design issues.

Customer loyalty

Every vendor strives to develop a loyal base of customers, and POAs are an excellent way to develop that loyalty. All the benefits are evident to customers, and they show their appreciation by sticking with their suppliers. The pressure is on the suppliers to keep the platforms relevant and high quality.

"In an increasingly connected world, retail and hospitality businesses need technologies that help the transition from transaction processing to enhanced customer service and relationship building," asserts Ilya Bukshteyn, senior director of Windows Embedded marketing at Microsoft. "Windows Embedded POSReady 2009 [Figure 3] is specifically designed to help enable this transition. With Windows technologies such as Microsoft Silverlight, .NET Framework 3.5, and Windows Presentation Foundation, the platform enables a differentiated and compelling user experience that can lead to greater customer loyalty."

The downside: Getting locked in

The disadvantages of POAs begin with getting locked into a particular platform containing a subcomponent that might not fully or correctly meet your product's needs. Changing a subcomponent can sometimes be difficult or impossible because of its integration into the POA. If you think this is going to be something that you may need to do during development, then you should ask if the platform components are interchangeable. This is where standards can provide assistance. Correct implementation of strategic standards can make subcomponents more interchangeable.

Sometimes the platforms have too little or too much functionality. Adding or deleting subcomponents can be very difficult or cost-prohibitive. Again, make sure to verify the platform architecture's scalability.

The future of platforms

"Platform design is the wave of the future," contends Bryan Lewis, semiconductor research VP for Gartner. "Design reuse, time to market, and risk management are of top importance to system designers in general and especially in this troubled economy. Platform design brings clear benefits to the market while controlling the cost for both chip suppliers and system designers."

Suppliers of components used in embedded computing devices will continue to roll out new platforms that are more specific to existing and future applications. Platforms have an untangible advantage that is difficult to measure with traditional ROI – the advantage of supplier focus. For suppliers to develop credible, industry-acceptable platforms, they must understand the market problems and needs on both sides of their position in the supply chain. Not having this knowledge prevents them from developing winning platforms.

Microsoft's Mike Hall, technical product manager for Windows Embedded, sees a strong future for platforms and is looking at new market segments to determine the next step. Platforms benefit everyone along the supply chain by easing the pain of integration and managing IP and licensing costs yet leaving the door open to quick customization that lets developers differentiate their products from the competition. ECD

Protocol analyzers simplify USB debugging

By Etai Bruhis

USB devices look pretty simple to use – at least when they're working correctly. Embedded engineers need the right set of tools to manage the details of proper device operation. The following examples show how USB protocol analyzers can do just that.

The widespread integration of USB into embedded applications presents many developers with the challenge of using this protocol for the first time. The complexity of USB can mask problems, leaving issues that are difficult to detect and isolate when a USB device misbehaves.

USB protocol analyzers allow engineers to gain greater visibility into the bus and help them quickly pinpoint the exact nature of a bug, whether it is in the physical, electrical, or protocol layer. Exploring how a USB protocol analyzer can be used to debug potential problems encountered in USB development shows how this can be accomplished.

Comparing tool options

Faced with a wide selection of debugging tools such as logic analyzers, oscilloscopes, and protocol analyzers, finding the ideal debugging tool can be a daunting task. Fortunately, the complexity of USB guides the choice of a suitable debugging solution.

As a result of this complexity, tools like logic analyzers or oscilloscopes may be limited by their low-level view, making it difficult to sort through large amounts of serial data. On the contrary, protocol analyzers can nonintrusively monitor the bus, view data as packets, and capture higher-level protocol-specific data in large volumes.

The setup for capturing USB data is a straightforward process. In Figure 1, the USB analyzer is connected in-line between the target host and the target device to nonintrusively capture data. While the target host and target device communicate with one another, the analyzer logs all of the bus traffic. Some analyzers store this data and display it once the capture is complete; others display and analyze the data in real time, as it is occurring on the bus.

In contrast with scopes and logic analyzers, USB capture software can display detailed information such as time stamp, device and endpoint address, Packet Identifiers (PIDs), and data in a human-readable format. The software also includes search and/or filter features to help developers quickly locate data of interest within a large amount of data.

The following examples demonstrate how a USB protocol analyzer can be used to help identify common problems in USB development.

USB data validity

USB employs two error-checking methods to ensure that data is sent correctly. A Cyclic Redundancy Check (CRC) is sent with all data transmissions to validate data integrity within a packet. In addition, a toggle bit is encoded in the data packet's PID to guarantee that packets are sent in the correct sequence. Correct data sequencing is especially important when attempting to transfer large files across multiple independent USB transmissions.

When transferring data over multiple packets, the data PID typically toggles between DATA0 and DATA1 on each consecutive successful transmission. As data is successfully transmitted, implying that the CRC is valid, the receiver acknowledges (ACK) the data, and both transmitter and receiver toggle their DATA bit. However, if there is a data error and the CRC check fails, the receiver will not reply with an ACK, and the transmitter will resend the data with the same toggle bit. The transmitter will continue to resend the same data with the same toggle bit until the receiver acknowledges its reception.

In some cases, the data is sent correctly, but the ACK handshake gets corrupted on the bus. When this occurs, the receiver

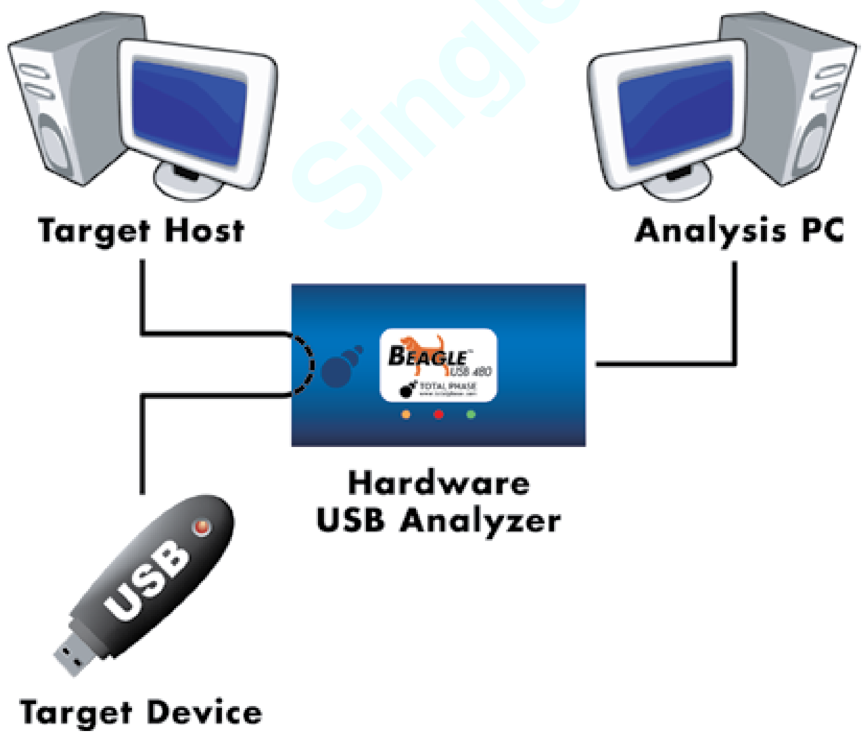


Figure 1 | In a typical device configuration for capturing USB data, the USB analyzer is connected between the target host and target device.

thinks that the data was sent properly and updates its toggle bit, but the transmitter does not actually know if the data was received correctly. Therefore, the transmitter will send the same data with the same toggle bit. Since the toggle bit has not changed, the receiver assumes that this is a retransmission of the same data and silently ignores the data. The receiver will then ACK, causing the transmitter's toggle bit to update correctly.

Finding problems in data bit toggling

Incorrectly handling the toggle bit is a common USB problem that is hard to identify because the symptoms do not necessarily render a device unusable. A device may simply appear to have a reduced throughput, or individual data transmissions may be dropped. Without the aid of a hardware protocol analyzer, it is nearly impossible to deduce that improper data toggling is the cause of the problem.

To illustrate this issue, consider a situation where a host side application is failing to receive any data from the device. To help in the debugging process, the device is configured to send a counter value that is updated with each successful transmission. The root of the problem can be traced to a variety of bugs related to firmware, software, and/or hardware.

Using a hardware protocol analyzer can quickly pinpoint this type of error. In Figures 2 and 3, data is being captured from two devices; one is functioning properly and the other is not. In both cases, it is clear that low-level hardware is functioning correctly, as valid data is being transmitted without CRC errors. To aid in the analysis, software display filters are used to display only DATA packets, as shown in Figures 2 and 3.

Sp	m:s.ms.us	Len	Err	Dev	Ep	Record	Data
HS	0:00.100.011	7 B		01	02	DATA0 packet	C3 00 00 00 00 FF D8
HS	0:00.100.023	7 B		01	02	DATA0 packet	C3 01 00 00 00 FE 27
HS	0:00.100.035	7 B		01	02	DATA0 packet	C3 02 00 00 00 FE 63
HS	0:00.100.046	7 B		01	02	DATA0 packet	C3 03 00 00 00 FF 9F
HS	0:00.100.058	7 B		01	02	DATA0 packet	C3 04 00 00 00 FE EB
HS	0:00.100.070	7 B		01	02	DATA0 packet	C3 05 00 00 00 FF 17

Figure 2 | The consecutive DATA0 PIDs in the record column show that the device is not toggling its data PID.

Sp	m:s.ms.us	Len	Err	Dev	Ep	Record	Data
HS	0:00.100.011	7 B		01	02	DATA0 packet	C3 00 00 00 00 FF D8
HS	0:00.100.023	7 B		01	02	DATA1 packet	4B 01 00 00 00 FE 27
HS	0:00.100.035	7 B		01	02	DATA0 packet	C3 02 00 00 00 FE 63
HS	0:00.100.046	7 B		01	02	DATA1 packet	4B 03 00 00 00 FF 9F
HS	0:00.100.058	7 B		01	02	DATA0 packet	C3 04 00 00 00 FE EB
HS	0:00.100.070	7 B		01	02	DATA1 packet	4B 05 00 00 00 FF 17

Figure 3 | The alternating DATA0 and DATA1 PIDs show proper toggling between subsequent packets.

Upon inspection, it is obvious that while one device did not toggle the data PID (Figure 2), the other one did toggle the data PID after each packet (Figure 3). As discussed earlier, sequential DATA0s should not be passed to the application because the receiver will ignore packets that repeat the same toggle bit. This explains why data is not being passed to the application. However, the reason why the same toggle bit is being used is still unknown.

To investigate this issue further, the entire transaction sequence can be examined (Figure 4). In this view, it is clear that the transaction is completing successfully because the capture shows the ACK for each data packet, but the DATA bit is not toggling. Furthermore, transmissions that use sequential toggle bits are supposed to resend identical data.

Because the device in this case continues to update its counter, the firmware must be processing the ACK from the host. The error therefore lies in the handling of the DATA toggle within the device. Specifically, the firmware is not toggling the bit on each successful transmission. Without a hardware protocol analyzer, this small mistake could take days or weeks for a developer to fix.

Low-level bus events

Another common error occurs with low-level bus events. The USB specification defines a number of crucial bus-level signaling events that follow specific timing criteria and determine such things as suspend, resume, and the high-speed handshake. Mistakes during these events can cause a number of errors, including a host's failure to recognize the device. These types of events are difficult if not impossible to debug without the aid of a hardware tool.

As an example, the high-speed handshake requires the host to issue a minimum of three pairs of alternately driven D- (Chirp K) and D+ (Chirp J) for 40-60 microseconds. Even though the USB specification only requires three pairs for this chirp sequence, hosts will often send hundreds of them. While it is possible to use a scope to measure this sequence of events and calculate durations with the cursors, utilizing engineering time to verify each chirp with a scope is a tedious and error-prone process. A hardware protocol analyzer, in contrast,

High-speed USB 2.0 monitor

The examples in this article were generated using the Beagle USB 480 Protocol Analyzer, a low-cost, nonintrusive, high-/full-/low-speed USB 2.0 bus monitor that can capture, display, and filter USB traffic and bus states in real time. An onboard 64 MB buffer ensures that sustained bursts of 480 Mbps traffic can be captured with no data loss. Other major features include On-The-Go support, automatic speed detection, hardware-based packet suppression, and multiple digital inputs and outputs for synchronization with external logic.

This protocol analyzer is compatible with Windows, Linux, and Mac OS X and comes with free software, API, updates, and technical support.

Sp	m:s.ms.us	Len	Err	Dev	Ep	Record	Data
HS	0:00.100.010	4 B		01	02	IN txn	00 00 00 00
HS	0:00.100.010	3 B		01	02	IN packet	69 01 C1
HS	0:00.100.011	7 B		01	02	DATA0 packet	C3 00 00 00 00 FF DB
HS	0:00.100.013	1 B		01	02	ACK packet	D2
HS	0:00.100.021	4 B		01	02	IN txn	01 00 00 00
HS	0:00.100.021	3 B		01	02	IN packet	69 01 C1
HS	0:00.100.023	7 B		01	02	DATA0 packet	C3 01 00 00 00 FE 27
HS	0:00.100.025	1 B		01	02	ACK packet	D2
HS	0:00.100.033	4 B		01	02	IN txn	02 00 00 00
HS	0:00.100.033	3 B		01	02	IN packet	69 01 C1
HS	0:00.100.035	7 B		01	02	DATA0 packet	C3 02 00 00 00 FE 63
HS	0:00.100.036	1 B		01	02	ACK packet	D2

Figure 4 | An expanded view of the transaction shows new data being sent with the same DATA toggle bit.

Sp	m:s.ms.us	Len	Err	Dev	Ep	Record	Data
FS	0:00.107.526	50.0 us				<K chirp>	
FS	0:00.107.576	50.0 us				<J chirp>	
FS	0:00.108.026	30.0 us	U			Bus event	<Reset> / <K chirp> / <Tiny K>
FS	0:00.108.056	50.0 us				<J chirp>	
FS	0:00.108.106	5.05 ms				[50 K-J Chirp Pairs] [1 K Chirp]	
FS	0:00.108.106	50.0 us				<K chirp>	
FS	0:00.108.156	50.0 us				<J chirp>	
FS	0:00.108.156	50.0 us				<J chirp>	

Figure 5 | The highlighted row shows an unexpected bus event halfway through the chirp sequence.

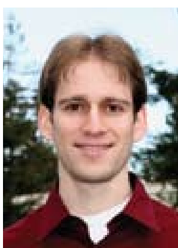
can save time by automatically measuring each signal and indicating potential errors. Furthermore, with an analyzer, these measurements can be done on every test run, thus automatically catching new or intermittent bugs.

In Figure 5, the capture software highlights an error with a mistimed chirp sent from a USB host under development. In this particular example, the mistake occurred halfway through the chirp sequence, and a cursory look on a scope would have missed it. The consequences of such an error are undetermined as this is out of spec, and any number of processes could malfunction.

While it is possible that a device is robust enough to handle this situation and can continue to function properly, other devices may be more sensitive to the out-of-spec signaling. If internal testing was only run with a small subset of devices that all passed, a developer without a hardware protocol analyzer may never know that such an error exists. A malfunctioning product could be sent out to the field, where the error would be exposed later – to the frustration of many customers. By using a hardware-based analyzer, engineers can avoid escalated costs due to unforeseen errors.

Quick and easy troubleshooting

The development and debugging stage is a crucial step in the product life cycle. As the aforementioned situations illustrate, using a hardware-based USB protocol analyzer presents the data packets of a complicated protocol such as USB in an accessible and human-readable format. Using an analyzer, engineers can easily test their applications and quickly identify problem areas while reducing development time and simplifying the debugging process. **ECD**



Etai Bruhis is an engineer for Total Phase, based in Sunnyvale, California, where he specializes in hardware development. He graduated magna cum laude from the University of California at Berkeley with a Bachelor's degree focusing on Mechanical and Electrical Engineering.

Total Phase
408-850-6500
sales@totalphase.com
www.totalphase.com

Software Bill of Materials improves Intellectual Property management

By Mahshad Koohgoli, PhD, and Sorin Cohn-Sfetcu, PhD

Accurate record keeping and proper Intellectual Property (IP) management enhances embedded system development throughout the design chain and ensures more effective product life-cycle support.

Software has become a ubiquitous part of cell phones, cameras, computers, and other mass-distributed consumer products. This pervasiveness can hinder embedded system developers given that software development costs sometimes outweigh those of hardware development, and product support issues are more often related to software rather than hardware problems.

However, embedded developers can reduce software development costs and schedules through software reuse, reliance on third-party code, and increasingly, open source code. Indeed, companies rarely create all of the software in their products. Much of the code is independently developed by the sources mentioned and then integrated into the final product with various degrees of value added throughout the development cycle. The cell phone example illustrated in Figure 1 demonstrates this integration and value-add process.

The cell phone combines software developed by the manufacturer and outsourced developers as well as the software that comes with the chipsets, which are typically developed in-house or acquired from third parties or open source directly or through various layers of chained suppliers.

An end product – in this case, the cell phone – is thus the sum of the code provided by the many organizations and individuals involved in the overall cell phone software supply chain. However, an end product rarely provides a complete and up-to-date view of all of these contributors and their respective software components. This can lead to increased costs, delayed schedules, and significant business risks if any of the software components do not meet proper IP and copyright obligations or if they have to be corrected once the product reaches the market. Imagine that a security fault is discovered in the protocol stack supplied by one of the players. Not only would it be difficult to ascertain which of thousands of products are affected, it would also be extremely tedious and costly to find a solution and correct the problem.

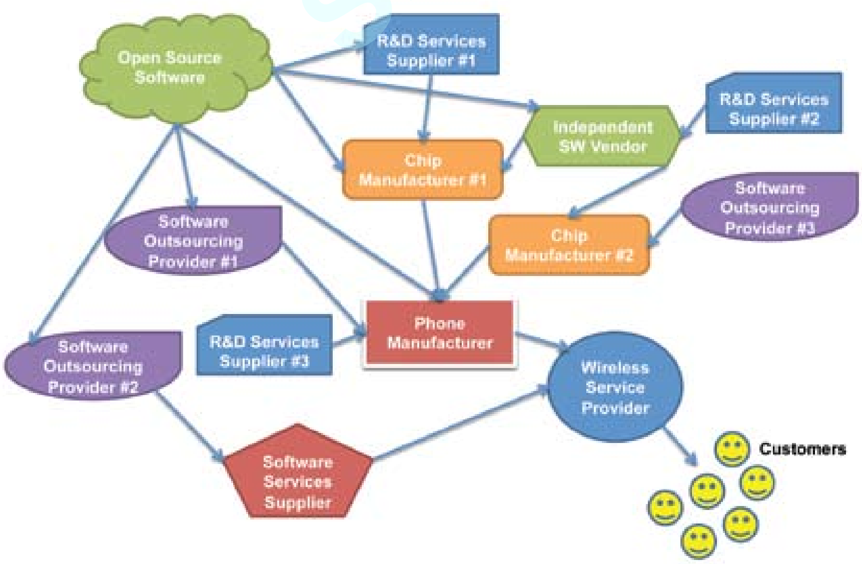


Figure 1 | The software code in a cell phone is provided by multiple parties involved in the product development cycle.

These issues would not exist if the software code came with proper records and pedigrees for all of its components. Few companies have managed to capture and deliver a software Bill of Materials (BOM) because until recently, most methods for determining what is in the code and ensuring correct IP management were retrospective; companies used either cumbersome manual audits or expensive tools for automatic code analysis. Such after-the-fact corrective methods can result in costly redesigns and delays in product availability.

Automatic tools check code history

Embedded developers can avoid these problems by adopting real-time record gathering and preventive IP management processes. To accomplish this, companies must set acceptable software adoption and IP policies and use newly released automatic tools to analyze, record, and compliance-check legacy code as well as any new code brought into the project.

Good software development practices have evolved to include systems for checking syntax, managing software versions, and tracking software bugs. Nonetheless, certain disciplines that are accepted practice in structured hardware development have yet to be adopted in software development:

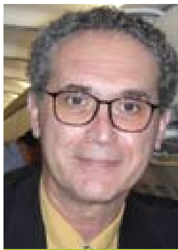
- An approved vendor list that contains the approved components and licenses, including commercial terms, vendor history, versions, and pricing so that a developer can select components from the list without concern
- Automatic notification when someone tries to use code with unapproved licenses or code modules governed by incompatible licenses
- A BOM that fully records which components are used in the final product, including details to enable production, determine costs, identify where it can be exported, and track vendor upgrades and other post-design activities

The best approach is to make record keeping and source code IP management an integral part of the software development and quality assurance processes.

Automatic tools are now available to handle these tasks in an unobtrusive manner and with minimal training, enabling project managers to define appropriate policies for record keeping, source code adoption, and IP management. For example, tools like Protecode's Enterprise IP Analyzer can be applied to existing (legacy) code for establishing an up-to-date map of its components and their pedigrees. Another tool, the Development IP Assistant, is integrated within specific development environments, where it operates unobtrusively in the background at each development workstation to detect, log, and identify in real time each piece of code brought by the developer into the respective project.

These tools check the attributes of each piece of code against the adoption and IP management policy for the project and take appropriate action according to the established policy. Furthermore, these tools provide a software BOM that enables developers and clients throughout the embedded system design chain to be fully cognizant of what is in the code and how to address support issues effectively.

Applying real-time record keeping and preventive IP management reduces development costs, avoids wasted resources in after-the-fact corrective activities, shortens development cycles, and enhances the overall lifelong value of embedded software systems. ECD



Sorin Cohn-Sfetcu *works in the marketing department at Protecode. He has 30 years of international business and technology experience and holds several patents in Web services, wireless, and digital signal processing. Sorin has an MSc in Physics from the University of Calgary, an MEng in Engineering Physics from the Polytechnic Institute of Bucharest, and a PhD in Electrical Engineering from McMaster University in Canada.*

Mahshad Koohgoli *is the CEO of Protecode, based in Ottawa, Ontario, Canada. He has more than 25 years of experience in the telecommunications industry and specializes in technology start-up businesses. Mahshad has a BSc and a PhD in Stochastic Control Processes from the University of Sussex, England.*

Protecode
Sorin: 613-301-0066
scohn@protecode.com
Mahshad: 613-721-5936
koohgoli@protecode.com
www.protecode.com

The high price of low-cost FPGA development boards

By Rob Evans

Low-cost FPGA development boards are a convenient option when starting a new project, but that choice carries a sting in its tail. These boards automatically constrain engineers' design options before they even start, forcing them to design in a fixed and predefined way that ultimately costs more money. As an alternative, designers should consider using a vendor-independent hardware development system that also communicates with the design software, resulting in a flexible, real-time development system that does not stifle innovation by restricting choices.

An expedient choice that bites back

A major challenge for any business, particularly in the current economic climate, is determining how much to invest in staff and equipment to achieve profitability goals. While overspending can wipe out potential increases in profit, underinvestment leaves companies ill-equipped to capitalize on market possibilities or even exposed to the risk of not achieving them.

Good business is all about finding the right investment-versus-results balance, making informed choices, and working toward fulfilling the company's needs in smarter ways. For the most part, companies both large and small accomplish this balancing act successfully. This frees them to focus on fine-tuning the corporate machine so that its long-term performance matches all those squiggly PowerPoint graphs business leaders are so fond of.

But in the electronics design industry, the rise of programmable devices such as FPGAs has unearthed an aberration in this normally sensible industry behavior. That quirk comes as a result of the FPGA development hardware and tools selection process, in which the usually thorough considerations of cost versus results, long-term implications, and workflow efficiency often take a holiday and are replaced by an equipment choice based on short-term expediency.

That convenient and often impulsive choice is a basic FPGA development board that costs about $49 and is supported by free development tools from the FPGA device vendor.

The cost of convenience

Although a $49 FPGA development board is undeniably attractive, it is nonetheless a curious and risky choice when placed in the framework of professional product design economics.

For example, say that a new product has a development cost of at least $1 million as well as potential revenue of more than $10 million, and is being designed by an engineer with a salary of $100,000 – not uncommon figures in today's industry. Considering that an extremely critical part of this multimillion-dollar development is consigned to a system investment of $49, these figures look somewhat misbalanced and even disturbing.

While it appears that the usual checks and balances failed in this case, they probably didn't; they just never happened, perhaps because a designer opportunistically decided that the $49 board could do the job, given that it has a suitable FPGA device, some useful peripherals, and a bunch of external connectors. The matching design tool set is a free download, so by making this quick decision, the designer can get cracking on embedded hardware development and embedded software developers can get one step closer to testing on real hardware.

On the surface this might seem like a reasonable solution to an immediate need, but in a professional design project where thousands or even millions of dollars are at risk, that unchecked decision carries a sting in its tail. Along with the quality limitations one might expect from a $49 piece of development hardware, the real "gotcha" is that the range of possible design choices is vastly reduced by the built-in constraints of that system. These limitations are likely to cause costly design compromises and delays.

One constraint is the fixed FPGA device on the board, which narrows the design path to that device family and vendor. An initial decision of selecting a device that has excess capacity means engineers won't run out of gates or I/O, but all other device capabilities and features must be accurately predicted before serious design can begin.

If designers get that choice wrong – the device turns out to be too slow, uses too much power, needs a hard-coded processor or DSP, or has been superseded – there's no other option but to look for an alternative device and a new development board. The new board might only cost another $49, but little of the existing design work can be transferred to the new device. This forces a substantial redesign and a costly delay in project development.

That scenario assumes that designers can source a suitable alternative device from the same vendor, but the situation is even worse if the only viable option is an FPGA from a different vendor. In this case, the incompatibility of the new device architecture means a total redesign and additional delays and cost. And all this time, the embedded software engineers are still waiting for the embedded hardware to arrive.

Another perhaps less obvious constraint is the free proprietary tool chain provided by FPGA vendors. While these tools are developed to support the vendor's products and encourage sales, they are understandably devoid of support for competitors' products. So if engineers change the FPGA device supplier to solve their design problems, they will also need to adapt to a new set of tools and methodologies.

All these factors add up: Designers have much less chance finding an optimal design solution; the change in device type forces a substantial redesign; switching vendors requires that designers learn new tools and methodologies; and above all, the outcome of a design project that potentially involves millions of dollars is placed at risk. In short, what was an expedient and possibly impulsive choice of development hardware turns out to be a decision that can severely compromise engineers' ability to explore design options for that project.

A sticky issue

In practice, the creeping truth is that the $49 approach has also created a strong motivation for designers to stick with that particular vendor and device family to avoid extra work and delays. The more designers use devices and IP from that supplier in subsequent designs, the more their collective design resources become narrowly locked to that vendor.

This means that the lack of design choice within a given project and the compromises it introduces spread virally through future designs. Reusing vendor-centric designs in subsequent projects narrows the possibilities from the beginning, so engineers tend to adapt the design to suit the vendor's FPGA rather than selecting an FPGA that best suits the design, effectively locking into one restrictive design path.

It's also likely that engineers source IP cores from the device vendor as a convenient kick start to their designs. That IP is only useful with a specific range of FPGA devices from that particular vendor, so it is stuck to a reduced range of silicon. This *sticky IP* compounds the issue of limited design choice by stopping designers from jumping between devices supplied by different vendors when they are exploring design options.

The short of it is that by taking the expedient path of a low-cost development board in the face of established equipment selection criteria, designers create a restricted vendor-sticky FPGA design environment. This environment automatically constrains the design options before the project starts, forces engineers to design in a fixed and predefined way, and devalues the design IP for future projects.

FPGAs change priorities

So why is it that rational, intelligent design engineers frequently adopt an approach that restricts their ability to design and places critical projects at risk?

The idea that this is a normal or acceptable way of working probably harks back to the early days of implementing FPGAs, which at the time were only regarded as a convenient and efficient host for large amounts of supporting glue logic. In this case, the decision to use an FPGA was probably made late in the design cycle, the functional value of that logic was low, and the need to reuse it was minimal.

As FPGA design evolved into a System-on-Chip (SoC) approach, where more functionally critical elements such as processors, memory, and data processing are implemented in an FPGA, the device and embedded hardware design became fundamentally important elements. The decision of which device to use was critical and came early in the design cycle, and the design IP it hosted represented a significant and valuable design investment. Design choices and design reuse became important for embedded hardware.

Today, the role of FPGAs has advanced to the point where they have become the core or central platform for a design. This is the next step beyond an SoC approach, where along with hosting high-level functions, an FPGA acts as the interfacing fabric for the design's hard and soft elements. A processor, memory, or DSP might be implemented as a soft core, physical hardware, or both, while reprogrammable layers hosted by the FPGA stitch it all together.

The key differentiating elements of product designs are now defined in both software and programmable hardware. All of this is critically influenced by the FPGA capabilities and the IP it hosts, so an approach that was acceptable in the days when FPGA-based simple glue logic was added as an afterthought is no longer valid. The need for a free range of choices for design exploration is now critical, and the cost implication of not having those choices is huge.

The question is, with thousands of dollars or more at stake, can engineers afford to take the risk of adopting a cheap FPGA development board and all it implies?

Investing in design freedom

What's needed is an FPGA development system that does not impose these limitations and design constraints. Ideally, this would be a reconfigurable development board that can host any device through a system of plug-in FPGA daughterboards (see Figure 1). The collection of daughterboards could be added to as needed, progressively increasing the range of device choices at hand during the design process.

Figure 1 | Investing in a smart, reconfigurable development board that features plug-in FPGA boards and peripheral hardware delivers long-term dividends.

The physical hardware aspect of embedded development is then independent of the type of FPGA and its vendor. This concept can be extended to hardware peripheral boards, where the development board offers a plug-in system for common peripheral stages such as LCD screens, I/O interfaces, or audio/visual signal conditioning. This can also include matching IP, making it fast and easy to move from one peripheral to another or to incorporate that hardware in the final design.

If that system offers a healthy range of expansion connectors and is built to a level of quality that reflects its importance, as opposed to built down to a low price, the hardware is then in place for an unrestricted approach to design.

The next step is exploiting that device freedom by removing the same constraints in the FPGA design tools. This can be done using a system of targeted drivers and constraint files that disconnect the embedded hardware design itself from the device it's hosted on. In this way, a new constraint file is simply loaded when the FPGA device is changed, the design source is still valid, and little or no redesign is required.

The result is an FPGA development system that opens the door to a vastly extended range of device and IP possibilities. The ability to change devices with minimal redesign means the final choice can be made much later in the design cycle when its requirements are fully known. Sticky IP, while still locked to certain devices, no longer constrains the current or future design path.

Most importantly, the quality, flexibility, and longevity of the FPGA development system reflect the importance and investment of the larger product development process. The financial risk of a restricted design choice is eliminated, and embedded developers are free to explore and choose the best possible design options for what is now a crucial part of project development. **ECD**

Rob Evans *is technical editor at Altium Limited, based in New South Wales, Australia. He has more than 20 years of experience in the electronics design and publishing industry, including several years as the technical editor for* Electronics Australia. *Rob studied Electronic Engineering at the Royal Melbourne Institute of Technology.*

Altium Limited
+61 2 8986 4400
rob.evans@altium.com
www.altium.com

Trends are good for press, not necessarily for sockets

By Jean J. Labrosse

It's easy for Real-Time Operating System (RTOS) providers to jump on the multicore and virtualization bandwagons. However, before going off in another direction, vendors should consider if these trends represent the requirements of most designs and ask themselves if existing design/performance issues have been sufficiently satisfied. Jean explains why "not yet" is the correct answer to this question.

Current buzz indicates that multicore and virtualization are the next move for RTOS vendors. However, in taking a closer look at the market, it appears that less than 10 percent of today's designs require the overkill provided by multicore or virtualization.

Certainly, these offerings have a place in particular applications and specific industries; however, designers seem to continually chase the latest and greatest fads before the overall industry has maximized previous trends. Consider the following challenges yet to be solved by embedded designers and vendors:

- Many companies are still struggling with moving from Assembly language to C. Some designers are moving from 8-bit to 32-bit processors, skipping 16 bits and still using Assembly language. Because 32-bit processors open a whole new world of possibilities, migrating to a high-level language, using an RTOS, and buying COTS products are more sensible choices.
- Approximately 45 percent of products today either don't use an RTOS or are still roll-your-own even though a commercial RTOS has substantial time-to-market advantages. A 2008 Embedded Market Forecasters survey of RTOS users revealed that 44.3 percent of projects that used an in-house RTOS and 41.4 percent of those that used open source were completed late by an average of three months.
- Is processor performance exhausted to the extent that multicores are a must? Performance bottlenecks in most cases are due to memory, not processors.
- As microprocessors become more complex, the visibility into their inner workings diminishes. Debuggers are great at proving algorithms and debugging the system statically (a breakpoint must be hit to step through code) but fall short with dynamic systems. Instead of adding more processor cores, semiconductor manufacturers need to add logic that can greatly enhance debugging.
- Code reuse is an extremely important design, time-to-market, and quality issue that is often all but ignored. This also applies to semiconductor vendors who don't always use the same hardware blocks when developing different chips. Two chips within the same family from the same manufacturer typically use two different USB device controllers. How many different SPI controllers, UARTs, and timers do designers need?

While it is important for designers to consider the future, it is even more imperative that they first close the loop on their own design/performance issues and determine if they are using the right tools and becoming more efficient at designing reliable systems.

Although designers will always be interested in the next best thing that can catapult the industry forward, they must make sure that the majority of design needs are met before taking too long to get designs out the door. Building or rebuilding a product with the complexity involved in multicore and virtualization designs is a daunting task. Instead, developing quality, user-friendly code, reusing code whenever possible, and following a pattern of logical steps for growth are the best design strategies, at least for now. ECD

Jean J. Labrosse *is president of Micrium, based in Weston, Florida. In addition to serving as a regular speaker at the Embedded Systems Conferences, he has written numerous articles for magazines as well as two books,* MicroC/OS-II: The Real-Time Kernel *and* Embedded Systems Building Blocks: Complete and Ready-to-Use Modules in C. *Jean has a BSEE and an MSEE from the University of Sherbrooke, Quebec, Canada.*

Micrium
954-217-2036
info@micrium.com
www.micrium.com

Fidus Systems Inc.
900 Morrison Drive, Suite 203 • Ottawa, Ontario K2H 8K7 Canada
866-883-4387
www.fidus.com

Electronic Product Development

Fidus Systems develops electronic products for a wide range of industries including aerospace, defense, consumer, medical, industrial, semiconductors and telecommunications. Whether it is turnkey product development or targeted assistance on a project, Fidus has the bench strength to offer highly qualified engineers. As a design partner, Fidus offers companies greater flexibility and capability in their product development with access to the expertise, process and tools to successfully move their concepts to revenue-generating products. Fidus uses proven product development and design methodologies combined with a comprehensive suite of tools. Fidus has delivered on more than 700 products and projects for 140 customers across North America.

fidus™
Electronic Product Development

CAPABILITIES

- System design and architecture
- Hardware design
- DSP/FPGA/ASIC design
- Software/firmware design
- Wireless/RF design
- PCB layout
- Signal integrity/EMC
- Prototype design and testing
- Regulatory compliance
- Environmental and reliability
- RoHS compliance/component obsolescence

For more information, contact: info@fidus.com RSC# 38782 @ www.embedded-computing.com/rsc

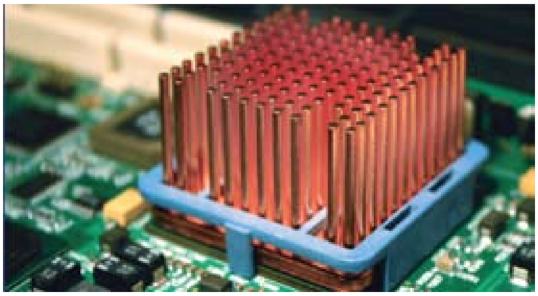
Radian Heatsinks
2160 Walsh Avenue • Santa Clara, CA 95050
408-988-6200
www.radianheatsinks.com

INM-PCU Series

The INM-PCU Series of copper round pin BGA heatsinks includes high efficiency cooling products that are ideal for omni-directional airflow.

These devices mount with EZ Snap™ Mounting Clips and/or Thermal Tape to provide optimum cooling for various package sizes and airflow. These off-the-shelf, high efficiency solutions are easy to install and require no special board modifications or complex assemblies.

radian
ISO 9001:2000 Certified



FEATURES

- High efficiency copper round pin design provides low pressure-drop characteristics
- Constructed of Forged CU1100 Oxygen-Free Copper for optimum heat transfer
- Ideal for omni-directional airflow
- Designed specifically for BGAs and other surface mount packages
- Optional EZ Snap Mounting Clip is made of UL94-V0 Rated Nylon
- Use Clip Tool HS8063 to attach or remove heatsink assembly directly to BGA Chip
- Finished with clear anti-oxidation finish
- Selected Clip and Thermal Pad Options are pre-assembled at the factory

For more information, contact: sales@radianheatsinks.com RSC# 41324 @ www.embedded-computing.com/rsc

Tundra Semiconductor

603 March Road • Ottawa, ON K2K 2M5 Canada
613-592-0714
www.tundra.com

PCI Express Bridges

The Tundra Tsi384™ and Tsi381™/Tsi382™ bridge between x4 PCIe and x1 PCIe, respectively, to PCI-X and PCI standards. All parts are compliant to the latest specifications including PCI Express Base Specification 1.1. Delivering low latency, high performance, and simple design and board layout requirements, the Tsi384™, Tsi382™, and Tsi381™ offer significant advantages in: cost, power, board space, and ease of design. The Tsi38x bridges offer extensive flexibility by supporting transparent, opaque, and non-transparent addressing modes. With best-in-class performance, solution cost, and quality, these devices are providing customers access to new design opportunities in a wide range of PCI Express applications.

FEATURES

- Most advanced PCIe bridges: Compliant to the latest PCIe and PCI-X specifications
- Smallest footprint: Tsi382™ x1 PCIe to PCI bridge enables designs where board space is constrained
- Highest quality: Proven interoperability ensures lower development risk and design churn
- Simplest design: No power sequencing restrictions and only two power supply voltages required
- Highest performance: Low latency, high throughput, and innovative features provide significant advantages
- Pinout compatible with other PCIe bridges offering low risk replacement or second source for existing designs

For more information, contact: sales@tundra.com   **RSC# 35975 @ www.embedded-computing.com/rsc**

Highland Technology, Inc.

18 Otis Street • San Francisco, CA 94103
415-551-1700
www.HighlandTechnology.com

T346 Arbitrary Waveform Generator

The T346 includes 4 independent DDS-based waveform generators, referred to as channels 0, 1, 2, and 3 with four additional internal channels, 4, 5, 6, and 7, which have no electrical outputs but can be used as modulation, summing, or control sources.

An internal microprocessor manages all data I/O and communicates via an RS-232 interface or 10/100 Ethernet.

Relays are provided to reroute channel 0-3 outputs to the internal test bus, then to the built-in self-test block, or to the dedicated SMB test connector for external calibration checks without disrupting field wiring.

FEATURES

- 4 channels of independent or synchronized sine, sawtooth, triangle, Gaussian noise, or square/pulse/PWM waveform generation
- 4096-point arbitrary waveform memory per channel
- Four additional internal waveform generator channels capable of complex modulations: AM, FM, PM, PWM
- Programmable channel summing
- Output frequency range 0 to 32 MHz with 0.015 Hz resolution
- DC coupled outputs to 10.24 volts p-p
- Programmable offset allows wave+offset or direct DC DAC functionality
- Programmable channel phase allows generation of quadrature or polyphase waveforms

For more information, contact: info@highlandtechnology.com   **RSC# 41306 @ www.embedded-computing.com/rsc**

Octasic Inc.
4101 Molson Street, Suite 300 • Montreal, H1Y 3L1, Canada
514-282-8858
www.octasic.com

Vocallo MGW

Vocallo MGW is a multi-core processor for voice and video over IP. Vocallo MGW offers a complete suite of features and focuses on reduced system cost, low-power, and high-density solutions. Vocallo MGW is the industry's lowest power consumption media gateway and allows you to increase your system density, therefore reducing system cost. Through Vocallo MGW's scalable pricing, you can select the features and capacity you need at optimal price points and create a wide range of products from a single hardware design.

Furthermore, with software development and verification being a critical path in any development schedule, Vocallo MGW's Megaco-based API integrates easily with your application software so that you can deploy your solution quickly.

Vocallo MGW supports applications such as 3G-324M, video phones, video conferencing, and video-enabled services with capabilities such as real-time video transcoding and video transrating and conferencing. Vocallo MGW's media API integrates H.263, MPEG-4, and H.264 codecs and several real-time video processing functions. Access to uncompressed native YUV video bitmaps enables developers to integrate their own video processing algorithms along with Vocallo MGW's software.

Opus

Vocallo MGW is based on Opus, Octasic's high-performing, low-power, clock-less DSP core architecture. Opus is designed to stay ahead of the technology curve. Its revolutionary clock-less architecture is three times more power efficient than other leading media processors.

With a standard programming model, Opus provides a rich instruction set that addresses both traditional DSP functions as well as header processing and task management code. Octasic's aggressive roadmap for the Opus core is made possible by this future-proof design.

FEATURES

› **Optimal Price Points**
- Feature selection
- Scalable and upgradable capacity selection
- User programmable and extensible
- Flexible I/O

› **Reduce System Cost**
- Lowest power per channel
- Best performance-to-power ratio in the industry
- Smallest space per channel

› **Quick to Deploy**
- API uses terminations with a connection-based model
- H.248 objects are reflected in the Vocallo MGW API

› **Pristine Quality**
- Low latency
- Designed for wideband
- Leading quality in voice and video

For more information, contact: marketing@octasic.com **RSC# 41099 @ www.embedded-computing.com/rsc**

Texas Instruments
12500 TI Blvd. • Dallas, TX 75243
972-995-2011
www.ti.com

Texas Instruments Family of Products

Digital Signal Processing (DSP) from Texas Instruments offers technologies for innovative system development and application design. Find DSPs, system solutions, OMAP™ applications processors, DaVinci™ technology, software development tools, evaluation modules, codecs, algorithms, and more.

DaVinci™ Digital Media Processors
TI's portfolio of DaVinci processors leverages the TMS320C64x+™ DSP core and consists of scalable, programmable Digital Signal Processing SoCs, accelerators, and peripherals that are optimized for a broad spectrum of digital video end equipment.

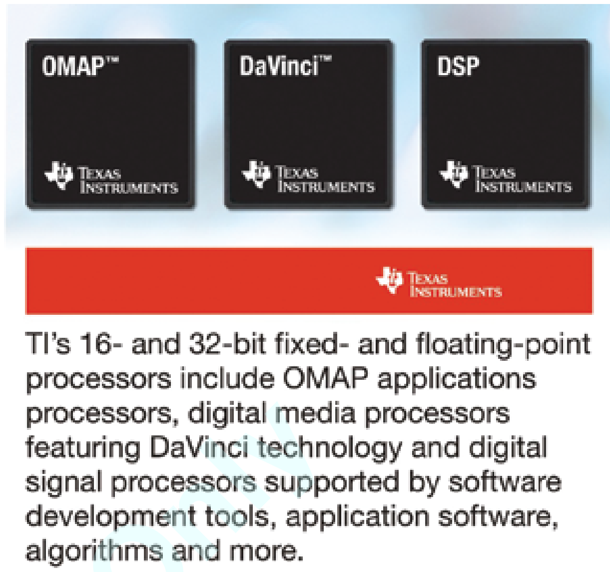
OMAP™ Applications Processors
TI's OMAP™ platform delivers a variety of high-performance applications processors with fast, portable power and a robust support network with a software portfolio that includes open source.

TMS320C6000™ High-performance fixed-point DSPs
High-performance TMS320C6000™ DSPs offer the industry's highest-performance fixed-point DSPs ideal for imaging, broadband infrastructure, and performance audio applications.

TMS320C6000™ Performance Value DSPs
C6000 Performance Value DSPs offer the industry's most efficient Performance Value fixed-point DSPs ideal for broadband infrastructure and performance audio applications.

TMS320C6000™ Floating-point DSPs
C6000™ processors, the industry's highest-performance floating-point DSPs, offer precision, speed, power savings, and dynamic range for professional audio, medical, industrial, and more.

TMS320C5000™ Low Power DSPs
C5000™ DSPs enable designers of power-sensitive systems to find the device that best suits their design. The TMS320C5000 DSP platform includes a broad portfolio of over 20 devices with the optimal combination of high performance, peripheral options, small packaging, and the best power-efficient performance in the industry.



FEATURES

DIGITAL MEDIA PROCESSORS

- TMS320DM646x is a multicore SoC consisting of DSP+ARM9 core specifically tuned for real-time, multi-format, HD video transcoding at 10x the performance and 1/10th the price
- TMS320DM644x consists of the fully programmable TMS320C64x+™ DSP core and a scalable, programmable ARM926-based SoC, plus accelerators and peripherals optimized for digital video end equipment
- TMS320DM643x is based on the C64x+ DSP core and features video, memory, and network interfaces ideal for networked video, vision applications, and other cost-sensitive digital media applications

OMAP APPLICATIONS PROCESSORS

- OMAP35x applications processors are based on the market's first broad offering of the ARM® Cortex™-A8 core to provide an unprecedented combination of laptop-like performance at handheld power levels in a single chip
- OMAP-L1x applications processors combine high levels of connectivity with low power to enable developers to integrate GUIs into their portable designs. The OMAP-L1x product line includes ARM9 and ARM9-plus-DSP architectures

C6000 FIXED- AND FLOATING-POINT DSPs

- TMS320C6455 is the highest-performance fixed-point DSP generation in the C6000 DSP platform and is based on the advanced VelociTI™ VLIW architecture developed by TI, making these DSPs the ideal choice for video and telecom infrastructure and imaging/medical applications
- TMS320C674x processors combine the high precision of floating-point DSPs with low power to enable portable innovation. TMS320C640x DSPs offer the lowest power consumption at high performance levels. These DSPs give designers the ability to add portability to processing-intensive applications
- TMS320C550x DSPs maximize battery life with the industry's lowest power fixed-point DSPs

For more information, contact: support@ti.com

RSC# 38790 @ www.embedded-computing.com/rsc

Tri-M Engineering
100-1407 Kebet Way • Port Coquitlam, BC V3C 6L3 Canada
604-945-9565
www.tri-m.com

VSX104+

The VSX104+ is a 300MHz PC/104-*Plus* CPU module with dual 10/100 LAN. Its 300MHz DM&P Vortex86SX System-on-Chip (SoC) is a fully static 32-bit x86 processor designed to work with embedded operating systems including Windows® CE, Linux, DOS, and most popular 32-bit RTOSs. Standard features of the VSX104+ include soldered 128MB DDR2 RAM, four COM ports, two USB 2.0, and two 10/100 LAN ports. An 8-bit GPIO port and redundancy port are also standard features. In addition to 2MB onboard SPI flash, the VSX104+ includes a Type I CompactFlash™ and microSD socket. System expansion is supported by the PC/104-*Plus* interface. The VSX104+ has an operating temperature of -40°C to +85°C. Single +5VDC power is supplied through the PC/104 bus or 2-position screw terminal, and total power consumption is a mere 2.5W.

FEATURES

- 300MHz Vortex86SX SoC
- 128MB soldered DDR2 RAM
- Integrated dual 10/100 LAN, 4x RS-232, 2x USB 2.0, 1x LPT, keyboard, mouse
- 2MB onboard SPI flash
- PC/104-*Plus* compliant
- Fanless operation
- 2.5W power consumption
- Type 1 CompactFlash™ and microSD sockets
- Extended temperature operation
- RoHS compliant

For more information, contact: info@tri-m.com

RSC# 41282 @ www.embedded-computing.com/rsc

Tri-M Engineering
100-1407 Kebet Way • Port Coquitlam, BC V3C 6L3 Canada
604-945-9565
www.tri-m.com

HE104+DX

The HE104+DX is a high efficiency 108W DC-DC converter that can supply +3.3V, +5V, +12V, and -12V DC outputs. The HE104+DX is designed for low noise embedded computer systems, has a wide input range of 6V to 40V DC, and is ideal for battery or unregulated input applications. The HE104+DX is specifically designed for vehicular applications and has heavy-duty transient suppressors (9,000W on both main and secondary inputs) that clamp the input voltage to safe levels, while maintaining normal power supply operation. The HE104+DX is a MOSFET-based design that provides outstanding line and load regulation with efficiencies up to 90 percent. Organic Semiconductor Capacitors provide filtering that reduces ripple noises below 20mV. The low noise design makes the HE104+DX ideal for use aboard aircraft or military applications or wherever EMI or RFI must be minimized.

FEATURES

- 108W DC-DC converter
- +3.3V, +5V, +12V, and -12V DC output
- 6V to 40V DC input range
- Extended temperature: -40°C to +85°C
- PC/104-*Plus* compliant
- High efficiency up to 90 percent
- High transient suppression
- Low output ripple
- Remote on/off standard
- Removable connector blocks

For more information, contact: info@tri-m.com

RSC# 16985 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

2.0 GSps 10-bit A/D

The Annapolis Single Channel 2.0 GSps A/D I/O Card provides one 2.0 GHz A/D input with a resolution of 10 bits. The board has one e2v AT84AS004 that is fed by an onboard analog input circuit, which converts the single-ended 50 ohm SMA input into differential signals for the ADC. There is a universal single-ended 50 ohm SMA clock input and a high-precision trigger input allowing multiple A/D I/O cards to be synchronized together. Synchronization of A/D I/O cards can be facilitated by the Annapolis 4 or 8 Channel Clock Distribution Boards.

In concert with the WILDSTAR 4 or WILDSTAR 5 FPGA processing main boards, this mezzanine board supplies user-configurable real-time continuous sustained processing of the full data stream. Up to two A/D and up to two Serial I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS or IBM Blade main board or up to one A/D and up to one Serial I/O card on each PCI-X or PCI Express main board.

Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. VHDL source is provided for the interfaces to A/Ds, D/As, DRAM/SRAM, LAD bus, I/O bus, and PPC Flash. CoreFire™ users will have the usual CoreFire Board Support Package.

The combination of our COTS hardware and our CoreFire FPGA Application Development tool allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed.

FEATURES

- One e2v AT84AS004 (2.0 GHz, 10-bit) A/D
- Four SMA front panel connectors: one 50 ohm analog input, one single-ended 50 ohm clock input, or differential 1.65 V LVPECL clock input
- One high-precision trigger input with Fs precision. High-precision trigger input – 1.65 V LVPECL, 2.5 V LVPECL, 3.3 V LVPECL
- Analog input bandwidth is 100 KHz-3.0 GHz
- I/O card plugs onto WILDSTAR 4 or 5 VME/VXS/PCI-X/PCI Express/IBM Blade main boards
- JTAG, ChipScope, and Serial Port access
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for board level interfaces
- Proactive thermal management system
- Includes one-year hardware warranty, software updates, and customer support
- We offer training and exceptional special application development support, as well as more conventional customer support
- Designed and manufactured in the USA

For more information, contact: wfinfo@annapmicro.com **RSC# 36021 @ www.embedded-computing.com/rsc**

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

Quad 600 MSps 16-bit DAC

The Annapolis Quad 600 MSps 16-bit DAC I/O Card provides up to four 16-bit output streams at up to 600 MSps each. The board has four Max 5891 16-bit DACs. Use the high-precision trigger to synchronize the four onboard DAC channels or to synchronize DACs between multiple boards (<1 Fs period).

The Quad 600 MSps board has six SMA front panel connectors: four single-ended DAC outputs, a high-precision trigger input with Fs precision, and a universal single-ended 50 ohm clock input. It has excellent SFDR and IMD performance, ultra-low skew and jitter saw based clock distributions, and main board PCLK sourcing capability.

In concert with the WILDSTAR 4 or WILDSTAR 5 FPGA processing main boards, this mezzanine board supplies user-configurable real-time Analog to Digital conversion and digital output. Up to two A/D or D/A and up to two Serial I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS or IBM Blade main board, or up to one A/D or D/A and up to one Serial I/O card on each PCI-X or PCI Express main board.

Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. VHDL source is provided for the interfaces to A/Ds, D/As, DRAM/SRAM, LAD bus, I/O bus, and PPC Flash. CoreFire users will have the usual CoreFire Board Support Package. The combination of our COTS hardware and our CoreFire FPGA Application Development tool allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES

- Four 16-bit Analog to Digital Converters: Max 5891
- Six SMA front panel connectors: four single-ended DAC outputs, one high-precision trigger input with Fs precision, and one universal single-ended 50 ohm clock input
- High-precision trigger input manufacturing options – 1.65 V LVPECL, 2.5 V LVPECL, 3.3 V LVPECL
- I/O card plugs onto WILDSTAR 4 or 5 VME/VXS/PCI-X/PCI Express/ IBM Blade main boards
- JTAG, ChipScope, and Serial Port access
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Industrial temperature range
- Proactive thermal management system
- Save time and effort. Reduce risk with COTS boards and software
- Achieve world-class performance; WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: wfinfo@annapmicro.com

RSC# 38791 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

SFPDP UNI6 I/O

Annapolis Micro Systems Inc.'s FPGA-based WILDSTAR family provides 24 SFPDP channels per VME slot.

The Annapolis SFPDP cards (UNI3 or UNI6) come with an easy to use Serial FPDP interface supporting up to 12 lanes of 2.5 Gb full duplex data. Three frame types are supported: Normal Data Fiber Frame, Sync Without Data Fiber Frame, and Sync with Data Fiber Frame in Point-to-Point Mode.

The card has three individually configurable, industry-standard 4X connectors, providing four lanes per connector, with dedicated signal conditioners to ensure clean communication. It supports up to 7.5 GB full duplex per I/O card and a wide variety of readily available copper and fiber cables.

Up to two serial I/O cards and two LVDS I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS main board, with half that number for the PCI-X or PCIe. The SFPDP card (UNI6) supports RocketIO protocol at up to 75 Gb full duplex per I/O card, three ports of 10G full duplex InfiniBand per I/O card, or 10G full duplex Ethernet per I/O card.

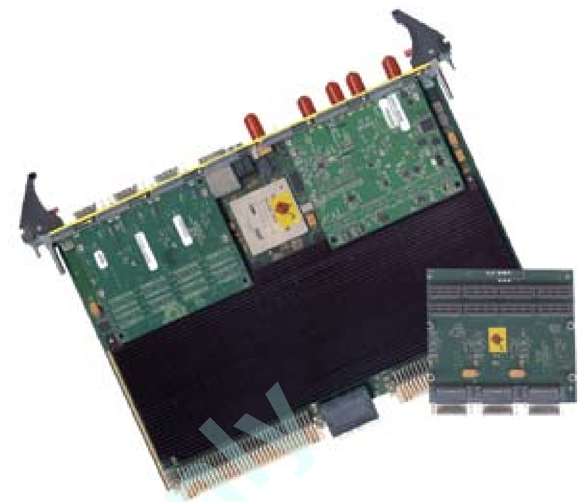
No other FPGA board vendor can match the volume of data we can send straight into the heart of the processing elements and then straight back out again.

An FPGA-based high-performance processing engine thrives on data streaming in and out at high rates of speed. The FPGAs should be part of a balanced and unified system architecture, providing maximum performance, with memory, processing power, and I/O speeds designed and integrated for performance, scalability, and growth.

Annapolis Micro Systems, Inc.'s WILDSTAR 4 (Xilinx Virtex-4 based) and WILDSTAR 5 (Xilinx Virtex-5 based) families of FPGA-based processing boards also support an extensive set of extremely high-quality A/D and D/A boards.

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed.



FEATURES

- Three individually configurable 4X connectors – four lanes per connector
- Up to four 2.5 Gb full duplex Serial FPDP ports per connector
- Up to 25 Gb full duplex RocketIO per connector
- Up to 10 Gb full duplex InfiniBand per connector
- Up to 10 Gb full duplex Ethernet per connector
- Optional onboard oscillators for other line rates like Fibre Channel
- I/O card plugs onto WILDSTAR 4 or 5 VME/VXS/IBM Blade Chassis/PCI-X/PCI Express main board
- JTAG, ChipScope, and Serial Port access
- Proactive thermal management system. Available in both commercial and industrial temperature grades
- Includes one-year hardware warranty, software updates, and customer support
- We offer training and exceptional special application development support, as well as more conventional customer support
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces

For more information, contact: wfinfo@annapmicro.com

RSC# 35968 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

WILDSTAR 4 for VXS

Annapolis Micro Systems is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. Our tenth-generation WILDSTAR 4 for VME64x/VXS uses Xilinx's newest Virtex-4 FPGAs for state-of-the-art performance. It accepts one or two I/O mezzanine cards in one VME64x or VXS slot, including Quad 250 MHz 12-bit ADC, Single 2.5 GHz 8-bit ADC, Quad 130 MHz 16-bit ADC, Dual 2.3/1.5 GSps 12-bit DAC, Quad 600 MSps 16-bit DAC, Universal 3 Gbit Serial I/O (RocketIO, 10 Gb Ethernet, InfiniBand), and Tri XFP (OC-192, 10G Fibre Channel, 10 Gb Ethernet). Our boards work on Windows, Linux, Solaris, IRIX, ALTIX, VxWorks, and others. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. With a graphical user interface for design entry, hardware-in-the-loop debugging, and proven, reusable, high-performance IP modules, WILDSTAR 4 for VME64x/VXS, with its I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES

- Four Virtex-4 FPGA processing elements – two XC4VFX100 or XC4VFX140, and two XC4VSX55 or XC4VLX40, LX80, LX100, or LX160
- Up to 6 GB DDR2 DRAM in 12 banks or up to 2 GB DDR2 DRAM and up to 64 MB DDRII or QDRII SRAM
- Available for either VME64x or VXS backplanes
- High-speed DMA multichannel PCI controller
- Programmable Flash to store FPGA images and for PCI controller
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Host software: Windows, Linux, VxWorks, and more
- Available in both commercial and industrial temperature grades/ Integrated heatsink for cooling and stiffness
- Proactive thermal management system – board level current measurement and FPGA temperature monitor, accessible through Host API
- Save time and effort. Reduce risk with COTS boards and software
- Achieve world-class performance; WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: wfinfo@annapmicro.com

RSC# 33233 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

WILDSTAR 5 for IBM Blade

Perfect Blend of Processors and Xilinx Virtex-5 FPGAs. Eleventh Annapolis Generation.

Direct Seamless Connections – No data reduction between: external sensors and FPGAs, FPGAs and processors over IB or 10 Gb Ethernet backplane, FPGAs and standard output modules.

Ultimate Modularity – From zero to six Virtex-5 processing FPGA/memory modules, and two Virtex-5 I/O FPGAs. Accepts one or two standard Annapolis WILDSTAR 4/5 I/O mezzanines: Quad 130 MSps through Quad 500 MSps A/D, 1.5 GSps through 2.2 GSps A/D, Quad 600 MSps DAC, InfiniBand, 10 Gb Ethernet, SFPDP.

Fully Integrated into the IBM Blade Management System – Abundant power and cooling to ensure maximum performance.

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. A graphical user interface for design entry supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules.

WILDSTAR 5 for IBM Blade, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Achieve world-class performance; WILDSTAR solutions outperform the competition.

FEATURES

- From two to eight Virtex-5 FPGA processing elements – LX110T, LX220T, LX330T, FX100T, FX130T, or FX200T. Six are pluggable with power module and memory
- Up to 10.7 GB DDR2 DRAM per WILDSTAR 5 for IBM Blade board
- 144 x 144 crossbar. 3.2 Gb per line. Two external PPC 440s – 1 per each I/O FPGA
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Available in both commercial and industrial temperature grades
- Proactive thermal management system – board level current measurement and FPGA temperature monitor, accessible through Host API
- Includes one-year hardware warranty, software updates, and customer support
- Blade management controller. USB, RS-485, Ethernet, KVM, 16 RIO, Switch to 1 GbE over backplane
- Save time and effort. Reduce risk with COTS boards and software
- We offer training and exceptional special application development support, as well as more conventional support
- Famous for the high quality of our products and our unparalleled dedication to ensuring that the customer's applications succeed

For more information, contact: wfinfo@annapmicro.com

RSC# 35882 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

WILDSTAR 5 for PCI Express

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS, FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications.

Twelfth-generation WILDSTAR 5 for PCI Express uses Xilinx Virtex-5 FPGAs for state-of-the-art performance. It accepts one or two I/O mezzanine cards, including Single 1.5 GHz 8-bit ADC, Quad 250 MHz 12-bit ADC, Single 2.5 GHz 8-bit ADC, Quad 130 MHz 16-bit ADC, Dual 2.3/1.5 GSps 12-bit DAC, Quad 600 MSps 16-bit DAC, Universal 3 Gbit Serial I/O (RocketIO, 10 Gb Ethernet, InfiniBand), and Tri XFP (10G Fibre Channel, 10 Gb Ethernet, OC-192). Our boards work on a number of operating systems, including Windows, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on data flow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules.

WILDSTAR 5 for PCI Express, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed.

FEATURES

- Up to three Xilinx Virtex-5 FPGA I/O processing elements – LX110T, LX220T, LX330T, or FXT
- Up to 7 GB DDR2 DRAM in 12 memory banks per WILDSTAR 5 for PCI Express board or up to 2 GB DDR2 DRAM in two memory banks and up to 40 MB DDRII, QDRII SRAM, or up to 1.4 GB RLDRAM
- Programmable Flash for each FPGA to store FPGA image
- 8x PCI Express bus. High-speed DMA multichannel PCI controller
- Supports PCI Express Standard External Power Connector
- Available in commercial or industrial temperature ranges
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- We offer training and exceptional special application development support, as well as more conventional support
- Includes one-year hardware warranty, software updates, and customer support
- Proactive thermal management system – board level current measurement and FPGA temperature monitor, accessible through Host API
- Save time and effort. Reduce risk with COTS boards and software
- Achieve world-class performance; WILD solutions outperform the competition

For more information, contact: wfinfo@annapmicro.com

RSC# 36017 @ www.embedded-computing.com/rsc

Connect Tech Inc.

42 Arrow Road • Guelph, ON, N1K 1S6 Canada
519-836-1291 | 800-426-8979
www.connecttech.com

FPGA & Digital I/O

Connect Tech's reconfigurable FreeForm FPGA computing modules save valuable time and project dollars. Based on the Xilinx Virtex-5 and Spartan-3E FPGAs, FreeForm provides a versatile platform for design flexibility.

FreeForm/PCI-104
Virtex-5 FPGA, 5 million gates, 8MB Flash, 128MB DDR2-400 memory, 64 single-ended or 32 LVDS I/O, RocketIO, 2x10/100 Ethernet, 2xRS-485, PowerPC option.

FreeForm/104
Spartan-3E FPGA, 500,000 gates, 4MB Flash, standard/custom cores, counter/timers, digital I/O, Opto-22 compatibility, 5V power connector for stand-alone usage, LEDs, rotary switch, reset button.

FreeForm is perfect for real-time applications where speed and accuracy are critical.

FEATURES

- Provides external 5V power connector for stand-alone operation
- Industrial temperature range models available (-40°C to +85°C)
- Free ISE WebPACK for complete FPGA design
- Reconfigurable in the field or through Connect Tech's Engineering Services
- Lifetime warranty and free technical support

For more information, contact: sales@connecttech.com

RSC# 32921 @ www.embedded-computing.com/rsc

Annapolis Micro Systems
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
410-841-2514
www.annapmicro.com

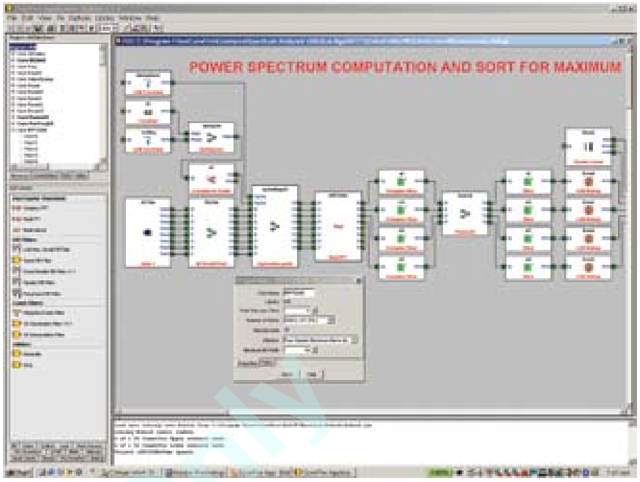
CoreFire

Develop your application very quickly and easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field.

Use CoreFire's graphical interface to drag and drop library elements onto the design window. Modify your input and output types, numbers of bits, and other core variables by changing module parameters with pull-down menus. The modules automatically provide correct timing and clock control. Insert debug modules to report actual hardware values for hardware-in-the-loop debugging. Hit the Build button to check for errors and as-built core sizes and to build an encrypted EDIF file. Use the Xilinx ISE tool to place and route each FPGA design. Modify and use the jar file or the C program created by the CoreFire Build to load your new file into your WILDSTAR and I/O card hardware. Use the CoreFire Debugger to view and modify register and memory contents in the FPGA and to step through the data flow of your design running in the real physical hardware.

Our extensive IP and board support libraries contain more than 1,000 proven, reusable high-performance cores, including FIR and CIC filters, a channelizer, and the world's fastest FFT. We support conversion between data types: bit, signed and unsigned integers, single precision floating point, integer and floating point complex, and arrays. A few of the newly added array cores include array composition and decomposition; slice, parallelize, serialize, repack, split, merge, reorder, rotate, and concatenate transformations; matrix math, sliding windows, and convolutions.

The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES

- Data flow-based – automatically generates intermodule control fabric
- Drag-and-drop graphical interface
- Work at high conceptual level – concentrate on solving algorithmic problems
- Hardware-in-the-loop debugging
- More than 1,000 modules incorporate years of application experience
- Reduce risk with COTS boards and software
- Save time to market
- Save development dollars
- Easily port completed applications to new technology chips and boards
- Training and custom application development available
- Achieve world-class performance; WILD solutions outperform the competition
- Annual node locked or networked license; includes customer support and updates

For more information, contact: wfinfo@annapmicro.com

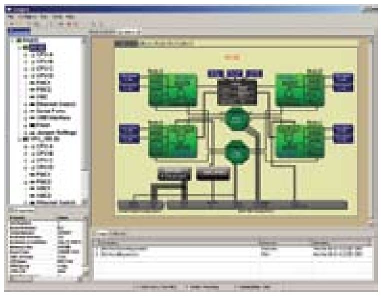
RSC# 33544 @ www.embedded-computing.com/rsc

Curtiss-Wright Controls Embedded Computing
741-G Miller Drive, SE • Leesburg, VA 20175
613-254-5112
www.cwcembedded.com

Continuum Insights

Continuum Insights is a suite of GUI-based software tools designed to ease and optimize the development of application software for multi-computer embedded systems. Designed to support systems ranging from a few to hundreds of processors/cores, Continuum Insights enables application programmers greater visibility into the entire system through the collection of critical, periodic, non-intrusive, real-time data. Continuum Insights aims to provide the level of information needed by developers of complex systems to accurately tune their system and ultimately speed time to market.

Continuum Insights harnesses the advantages of complementary Continuum products such as Continuum Firmware & BSP, Continuum Vector, and Continuum IPC. Continuum Insights is supported on Curtiss-Wright's VPX/VPX-REDI based single board computers, and DSP and FPGA engines.



FEATURES

- Quickly and easily visualize multi-computer system
- Hierarchical views of system provide status and health information at the system level down to the component level
- Event data collection across multiple processors and cores, correlated in time using a common time base
- Initialize entire multi-computer or a group of processors with a set of executables (define, download, and launch) from a simple, configurable, user-defined launch plan
- Multi-Node Debugger extends the capabilities of a source level debugger by supporting multiple nodes concurrently
- Set breakpoints across all processing nodes that when reached, will halt the entire system or a subset of the system

For more information, contact: sales@cwcembedded.com

RSC# 40988 @ www.embedded-computing.com/rsc

Altia, Inc.

7222 Commerce Center Drive, Suite 240
Colorado Springs, CO 80919
719-598-4299
www.altia.com

Altia DeepScreen

Altia DeepScreen is a graphics code generator that converts Altia Design prototype graphics into deployable graphics code. By simply selecting the design objects that represent the display portion of a product and clicking on the "Generate Code" menu, ANSI C code is generated in seconds. This code can be generated for any RTOS that DeepScreen supports (Windows, Windows CE and .NET, UNIX, Linux, QNX, and more). DeepScreen will also generate code for a proprietary or limited RTOS and quickly integrate with an existing graphics library. Changes to interfaces can be accomplished quickly. Graphics code can be used on both high- and low-end targets – from Windows machines to FPGAs to 8-bit micros. DeepScreen saves programmers from the grunt work of graphics coding and allows developers to meet aggressive schedules. DeepScreen supports 8-, 16-, and 32-bit processors with fixed point or floating point arithmetic.

FEATURES

- Easily try different targets – dialog driven choice of target RTOS
- Choice of code generation optimizations
- Generates code for graphics, animation, stimulus, and control
- From Altia Design select items for code generation
- No limit to combination or number of objects that can be selected
- Link in your application code and use your own main loop
- Porting kit to generate code for currently unsupported OSs or GLs
- Supports 8-, 16-, and 32-bit processors
- Supports fixed point and floating point processors

For more information, contact: info@altia.com

RSC# 32775 @ www.embedded-computing.com/rsc

CodeSourcery

9978 Granite Point Court • Granite Bay, CA 95746
888-776-0262
www.codesourcery.com

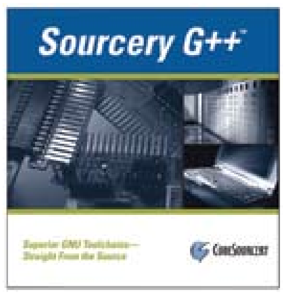
Sourcery G++

Sourcery G++™ professional C/C++ development tools from CodeSourcery offer high value at an affordable price. Sourcery G++ includes an IDE, compiler, debugger, simulator, and more tools for the embedded developer.

Sourcery G++ is available for the ARM®, ColdFire®, fido™, MIPS®, Power Architecture®, Stellaris®, and x86 processor architectures. Sourcery G++ runs on GNU/Linux® and Windows® host systems and targets bare metal, uClinux™, GNU/Linux and Windows systems.

Sourcery G++ Professional Edition features unlimited support from CodeSourcery's expert engineers, and Sourcery G++ Personal Edition is designed for individuals and small development teams.

Download a free 30-day evaluation of the new spring 2009 release!



FEATURES

- Eclipse™-based integrated development environment
- Optimizing ISO-compliant GNU C/C++ compilers (GCC 4.3 plus enhancements)
- C/C++ runtime libraries
- Flexible GNU macroassembler and powerful GNU linker
- Source- and assembly-level GNU Debugger
- Debug Sprites for hardware debugging using a JTAG/BDM device
- Instruction set simulator and GNU/Linux application simulator based on QEMU™
- Easy-to-use graphical installer and comprehensive documentation

For more information, contact: sales@codesourcery.com

RSC# 37420 @ www.embedded-computing.com/rsc

TeamF1, Inc.
39159 Paseo Padre Pkwy., Suite 121 • Fremont, CA 94538
510-505-9931
www.TeamF1.com

Managed Access Point Solution

TeamF1's Managed Access Point Solution is a comprehensive turnkey Wi-Fi® Access Point and router software package that combines a rich set of field-proven, standard components with an array of customizable options to provide OEMs/ODMs the ultimate in product flexibility. A member of TeamF1's SMBware™ family of innovative pre-packaged solutions, the Managed Access Point Solution enables OEMs/ODMs to deliver leading-edge 802.11 a/b/g/n devices to the Small-to-Medium Business (SMB) market in record time at far less risk than traditional development approaches. Devices built around the Managed Access Point Solution offer end-customers advanced wireless security, easy-to-use device management features, and multiple add-on options for VPN, Firewall, NAT, and authentication functionality. TeamF1's Managed Access Point Solution also includes Krypto-Lite, TeamF1's FIPS-certified common crypto framework, along with a suite of encryption and integrity components to secure and manage wireless traffic. Krypto-Lite allows the seamless integration of other optional security protocols developed by TeamF1 such as SSL/https, SSH, and IPsec/IKE to meet additional security requirements common in managed gateways. The Managed Access Point Solution allows embedded device OEMs to bring wireless AP-based products to market faster than ever before, combining a rich feature-set with the latest security technologies.

TECHNICAL SPECS

- Standard, field-tested software solution in a production-ready custom package, with all hardware integration, porting, testing, and validation completed by TeamF1
- Wireless AP or AP/Router with advanced SSL + IPsec VPN/Firewall and NAS add-ons available for an all-in-one wired + wireless LAN solution
- Friendly browser-based remote web-management provided by interfaces that utilize an easy-to-understand, step-by-step wizard for simpler configuration
- Advanced security including 802.11i in Personal and Enterprise modes, MAC Access List, and Rogue Access Point Detection
- Branding options offer a cost-effective, customized look and feel

FEATURES

- Support for multiple simultaneous radios and multiple LAN interfaces enables robust enterprise-grade AP features
- Support for advanced 802.11 standards for security, QoS, mobility, and roaming
- VLAN aware multiple Virtual Service Sets/Virtual AP enable delivery of services of various types/quality from multiple providers on the same physical AP
- Support for advanced technologies including WDS, wireless bridging, fast-roaming, mesh extensions, and RSTP
- Advanced management capabilities including SNMPv3, CLI, AJAX, and HTML web-management, TR-069
- Complete turnkey solution for building Wi-Fi devices with secure, managed access points lessens OEMs' development costs, risk, and time to market
- Selected MAPS and SMBware networking and security modules enable OEMs to easily differentiate products
- Support for a broad range of Wi-Fi chipsets

For more information, contact: Sales@TeamF1.com

RSC# 33643 @ www.embedded-computing.com/rsc

TeamF1, Inc.
39159 Paseo Padre Pkwy., Suite 121 • Fremont, CA 94538
510-505-9931
www.TeamF1.com

Secure Gateway Solution

TeamF1's Secure Gateway Solution is a comprehensive turnkey software package that combines a rich set of field-proven, standard components with an array of customizable options to provide OEMs/ODMs the ultimate in product flexibility. It enables OEMs to build fully integrated UTM devices allowing users to carve out security zones and manage security policies in a centralized manner. A member of TeamF1's SMBware™ family of innovative prepackaged solutions, the Secure Gateway Solution enables OEMs/ODMs to deliver leading-edge VPN/Firewall/IPS/Gateway AV devices to the Small-to-Medium Business (SMB) market in record time at far less risk than traditional development approaches. Devices built around the Secure Gateway Solution offer end-customers ironclad, advanced networking security, easy-to-use device management features, and multiple gateway options. TeamF1 also offers OEMs different ways to customize, or "brand" the Graphical User Interfaces (GUIs) of gateway devices. With the Secure Gateway Solution, OEMs can build gateways between multiple LAN, WAN, and DMZ interfaces – plus any other security zones – of several different types. WAN interfaces can include DSL, cable modem, Ethernet, cellular data (3G) links, or even a Wi-Fi® client link. LAN interfaces can include a simple Ethernet port connected to an external switch, a built-in Ethernet switch (an unmanaged or a "smart" managed switch), or an 802.11 a/b/g/n Wi-Fi access point.

TECHNICAL SPECS

- Standard, field-tested software solution in a production-ready custom package, with all hardware integration, porting, testing, and validation completed by TeamF1
- Wireless AP Gateway with advanced SSL + IPsec VPN/Firewall/IPS capabilities for an all-in-one wired + wireless LAN solution
- Friendly browser-based remote web-management provided by interfaces that utilize an easy-to-understand, step-by-step wizard; simplifies configuration of even the most advanced VPN tunnel schemes
- TR-069, SNMP, and powerful SSH-secured Command Line Interface (CLI) provided to configure and monitor a gateway device and automate common tasks
- Extensively validated on a variety of embedded OSs (including VxWorks and Linux), and CPU platforms that include ARM/XScale, MIPS, PowerPC, and x86 processors

FEATURES

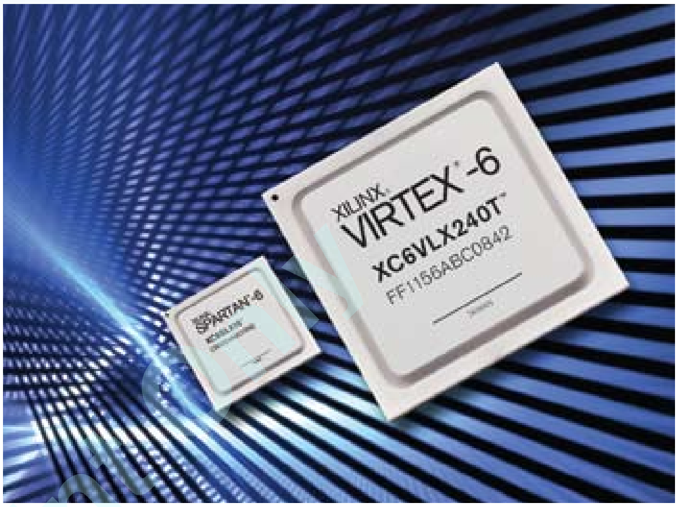
- Proven TeamF1 software components and common framework lessen OEMs' risk
- Comprehensive set of features packaged to provide full customization of devices: TeamF1 modules, validated third-party or OEM modules, professional services
- Extensive IEEE 802.11 (including 802.11n) support, with emphasis on security and Quality of Service
- Advanced protocols (IPsec VPN, SSL, etc.) provide ironclad networking security features
- Management features make it easy to configure VPN tunnels
- Multiple gateway options enable OEMs to build more flexible devices
- TeamF1's validated software modules include extensive protocol support
- Performance features make possible high-throughput applications, fast VPN tunnel creation, and hardware acceleration
- Branding options offer a cost-effective, customized look and feel

For more information, contact: Sales@TeamF1.com

RSC# 33638 @ www.embedded-computing.com/rsc

Editor's Choice

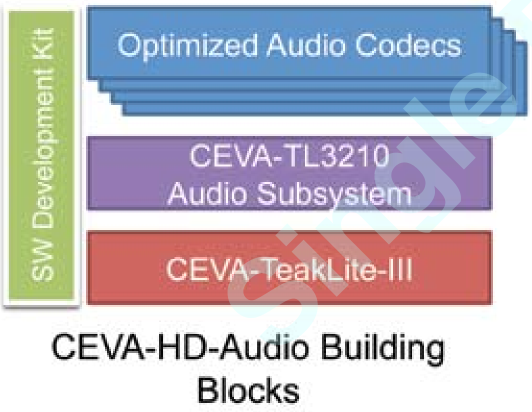
This month's Editor's Choice Products all share the common theme of "platform." We feature a range of platforms from processors to Operating Systems (OSs) to illustrate how popular the platform strategy is in the world of embedded computing.



FPGA families lay programmable foundation

Programmability is increasingly becoming a requirement for electronics manufacturers to keep their innovative edge in challenging business and technological environments. The new high-performance Virtex-6 and low-cost Spartan-6 FPGAs from Xilinx and its network of third parties lay the foundation for a new generation of targeted design platforms that can enable system designers to increase productivity and minimize development costs. These FPGA families will provide system designers with simpler, smarter, and more strategically viable methodologies for creating FPGA-based System-on-Chip (SoC) solutions targeting a wide variety of markets and applications.

Xilinx
www.xilinx.com
RSC# 41325



DSP-based platform brings HD audio to life

CEVA, Inc. recently introduced its configurable and programmable CEVA-HD-Audio platform that addresses the demanding audio requirements of home entertainment and consumer products including Blu-ray DVDs, DTVs, set-top boxes, and other A/V devices.

CEVA-HD-Audio combines a proven, high-performance DSP engine with customized audio implementation capabilities in a single-core system, helping product developers implement advanced audio functions in their next-generation products more efficiently. A Software Development Kit (SDK) including software development tools, development boards, system drivers, and a Real-Time Operating System (RTOS) allows licensees to develop and integrate their systems quickly and easily. Extensive algorithms and applications from the third-party development community are part of the platform.

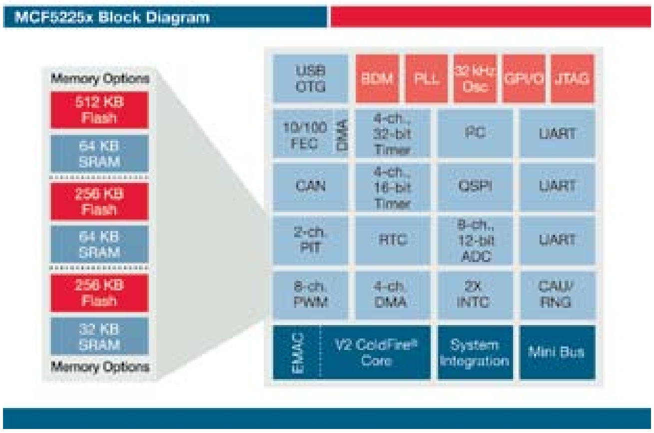
CEVA, Inc.
www.ceva-dsp.com
RSC# 41326

RTOS-equipped MCUs offer one-stop-shop

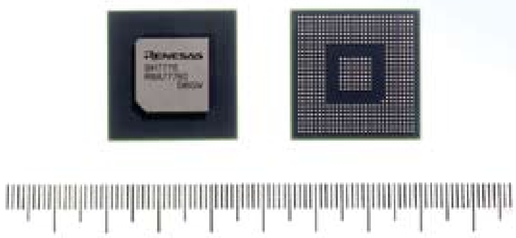
Embedded developers face constant pressure to do more with less – enhance application performance and connectivity, reduce costs, and speed time to market. To help developers successfully meet their design challenges, Freescale Semiconductor offers an industrial connectivity solution that combines its highly integrated 32-bit ColdFire MCF5225x MCU family with the MQX RTOS.

With on-chip USB, Ethernet, CAN, and encryption, the combined silicon and software solution gives developers exceptional design flexibility, connectivity options, and fast time to market backed by a full-featured, scalable RTOS platform. To ease the development process, Freescale provides a comprehensive ecosystem of software development tools, evaluation boards, reference designs, software examples, and webinars.

Freescale Semiconductor
www.freescale.com
RSC# 41327



Editor's Choice Products are drawn from OSM's product database and press releases. Vendors may add their new products and submit press releases at submit.opensystemsmedia.com. OSM reserves the right to publish products based on editors' discretion alone, and does not guarantee publication of any product entries.



Dual-core SoC handles image recognition

Renesas Technology America, Inc. recently announced the SH7776 (SH-Navi3), a dual-core SoC device with enhanced graphics functions and a high-performance image recognition processing function for next-generation car information terminals.

The device integrates two high-performance SH-4A 32-bit CPU cores that deliver processing performance up to 1,920 MIPS. On-chip peripheral modules required by car navigation systems include a serial ATA interface, an audio encoder and other sound interfaces, a USB 2.0 host/function interface, a TS interface for receiving terrestrial DTV broadcasts, and a GPS baseband processing module. This complement of peripheral functions makes it possible to reduce the total number of components in these types of systems.

Renesas Technology America, Inc.
www.renesas.com
RSC# 41328

Embedding Wireless USB in consumer electronics

Jungo and Wisair have collaborated on a complete Wireless USB solution for Linux-based and embedded platforms used in consumer electronics devices. One of the many products that debuted during the Consumer Electronics Show in January, this solution combines Jungo's USBware protocol software stack with Wisair's single chip-based Wireless USB reference designs. The new offering enables OEMs to embed Wireless USB into non-Windows consumer electronics devices such as set-top boxes, TV sets, smart phones, and DVRs, providing more options for consumers to connect external devices with a higher throughput delivered.

Jungo
www.jungo.com
RSC# 41329

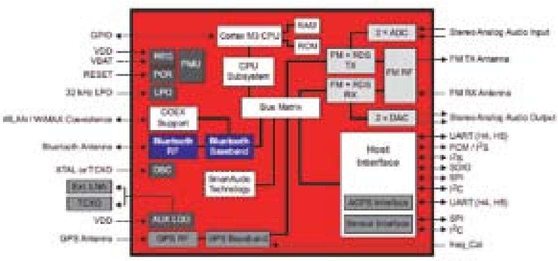
Wisair
www.wisair.com
RSC# 41447

Multiple radios in one chip

Broadcom Corporation has extended its chip portfolio with a highly integrated GPS, Bluetooth, and FM radio IC that delivers location-based services and advanced multimedia in a single-chip platform. With its InConcert coexistence technology, the BCM2075 allows these radios to operate simultaneously with minimal interference.

This connectivity processor significantly reduces host and application processing, enabling greater adoption in mass market handsets, portable media players, and personal navigation devices. The BCM2075 includes network support for accurate indoor and outdoor positioning, enabling advanced location-based services regardless of user location.

Broadcom Corporation
www.broadcom.com
RSC# 41330



BCM2075 Block Diagram

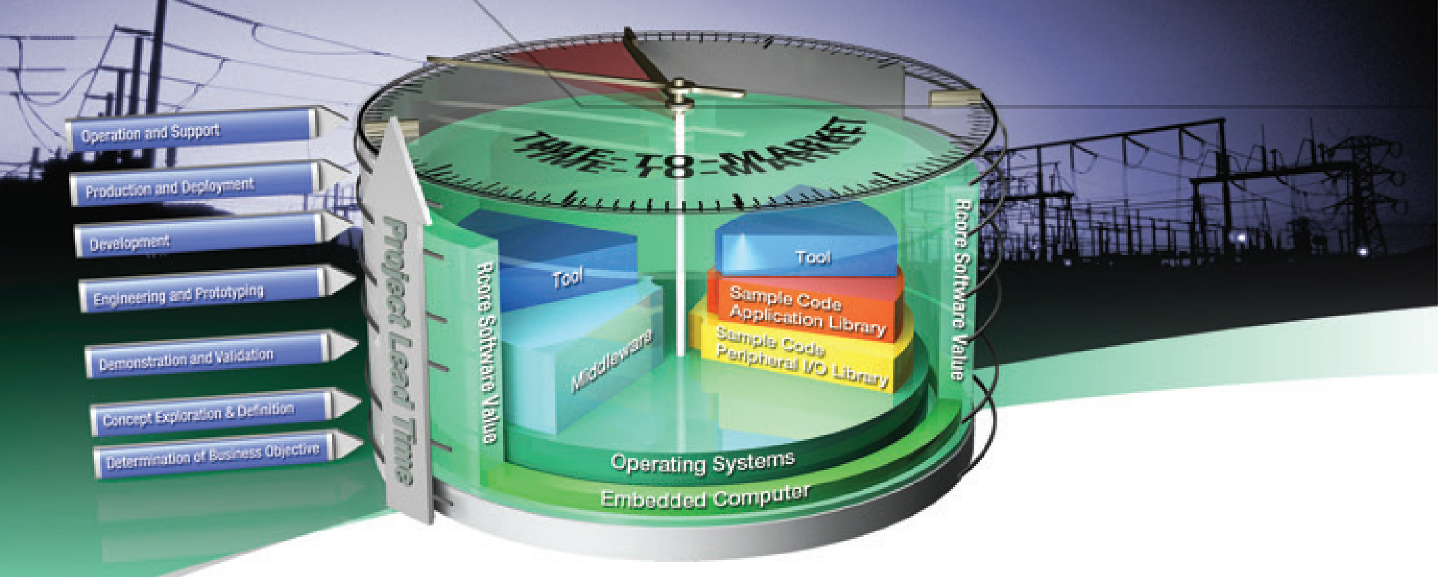
PROFILE INDEX

Advertiser	Category	Page
Altia, Inc.	Software	49
Annapolis Micro Systems	Programmable logic	40
Annapolis Micro Systems	Programmable logic	41
Annapolis Micro Systems	Programmable logic	42
Annapolis Micro Systems	Programmable logic	43
Annapolis Micro Systems	Programmable logic	44
Annapolis Micro Systems	Programmable logic	45
Annapolis Micro Systems	Software	47
CodeSourcery	Software	49
Connect Tech Inc.	Programmable logic	46
Curtiss-Wright Controls	Software	48
Fidus Systems Inc.	Design aids	34
Highland Technology, Inc.	Interfaces	35
Octasic Inc.	Microcontrollers and processors	36
Radian Heatsinks	Design aids	34
TeamF1, Inc.	Software	50
TeamF1, Inc.	Software	51
Texas Instruments	Microcontrollers and processors	37
Tri-M Engineering	Microcontrollers and processors	38
Tri-M Engineering	Power management	39
Tundra Semiconductor	Interfaces	35

Advertiser Information

Page #	Advertiser	Ad title
54	ACCES I/O Products, Inc.	USB embedded I/O solutions
31	ACT/Technico	Solid state storage solutions
13	Aitech Defense Systems	On land or in the air
38	American Portwell Technology	Your trusted provider
5	Annapolis Micro Systems, Inc.	WILDSTAR 5
53	Cogent Computer Systems, Inc.	CSB7xx
18	Concurrent Technologies, Inc.	x86 processor boards
48	Contec USA	BOX-PC 950 Series
55	Embedded Systems Conference	We speak embedded
6	Interface Concept	Switches & IP routers
56	Jacyl Technology Inc.	XG-5000K
46	LiPPERT Embedded Computers	Embedded efficiency
23	MEN Micro Elektronik GmbH	ESMexpress COM: Rugged PowerPC
27	Micro Digital, Inc.	Looking for the right software
1	Moxa Technologies, Inc.	Empower your competitiveness
33	North Atlantic Industries	MIL-STD is the only thing
11	Performance Technologies	Our advanced managed platforms
39	Precision Analog Systems (PAS)	Your source for VMEbus & PCI Express
17	Swissbit	Experience the value
15	Technobox, Inc.	Create your own PMCs
19	Technologic Systems	7" touch panel computer
48	TEWS Technologies LLC	COTS I/O solutions
25	Tri-M Systems Inc.	PC/104 Can-Tainer
29	Tri-M Systems Inc.	100MHz PC/104 module
9	Vector Electronics & Technology, Inc.	VME and cPCI system packaging
7	VersaLogic Corporation	You design products
2,3	WinSystems, Inc.	A 1GHz fanless industrial SBC


Empower Your Competitiveness
for Faster Time-to-Market
Rcore
Time-to-Market
Project Lead Time
Operation and Support
Production and Deployment
Development
Engineering and Prototyping
Demonstration and Validation
Concept Exploration & Definition
Determination of Business Objective
Tool
Tool
Middleware
Sample Code Application Library
Sample Code Peripheral I/O Library
Operating Systems
Embedded Computer
Rcore Software Value
express
MOXA
Rcore



Rcore - Moxa's Embedded Software Platform

Take advantage of Moxa's Rcore platform to increase your competitiveness and ensure a faster time-to-market. The Rcore platform provides the following hard-to-beat benefits:

- Easy-to-use application libraries
- Proven and bug-free sample code
- Consulting-level advice for application development
- Fast concept validation and development cycle

Operating Systems

Moxa's x86 and RISC-based embedded computers offer a powerful computing environment and stable system for a variety of industrial applications. These computers use either a Linux or Windows (CE and XPe) embedded operating system to provide programmers around the world with a user-friendly environment for application development, and help reduce the effort required for system integration. Moxa continues to look for real-time operating systems that are suitable for mission critical applications.

Middleware

Moxa offers a variety of middleware to help you easily integrate these application modules into your system. This is essential for leveraging the key features of these modules and reducing the effort required for application development. The VPN (OpenVPN, L2TP, and IPSec) middleware makes it easy for user applications to create secure tunnels between communication parties. The firewall (iptable) middleware protects enterprise information from un-friendly access. The database system (MySQL and MSSQL) middleware can be used to manage field-data acquisition, with web services (Web, PHP, ASP) included to give programmers an integration framework for building Internet accessible field applications, such as WebSCADA.

Sample Code

To lower customers' development cost, Moxa provides sample code for a wide range of embedded applications, such as serial-to-Ethernet (S2E), serial-to-serial (S2S), and Modbus TCP and RTU. This high-level sample code or application libraries hide the details of implementing complex data communication by presenting relatively simple function prototypes for user applications. In addition, low-level libraries that manage direct access to peripheral I/O devices, such as LCM, key pad, digital IO signals, and watchdog functions, are also included.With ready access to such a rich assortment of embedded applications, programmers obtain a much greater flexibility than would otherwise be possible.These libraries help programmers quickly grasp the full functionality of their applications, and in this way gain the confidence needed to complete their project, essentially speeding up product development and ensuring that code is efficient and bug-free.

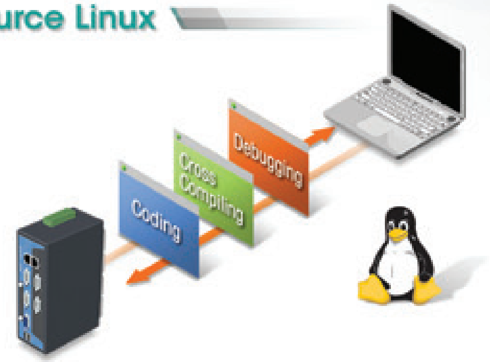
Tools

Moxa provides a Windows PC-based tool (MDM) that auto-detects, configures, and manages Moxa's embedded computers over an Internet environment. This tool provides features for setting IP addresses, managing files, monitoring memory usage of computers, and helping application developers deploy their programs en masse to an entire army of computers.

Embedded Computing with Open Source Linux

Open Source Linux architecture for easy development

The pre-installed Linux OS provides an open source software operating system for your software development. This means that software written for the desktop PC is easily ported to Moxa's embedded computers by performing a GNU cross compile without needing to modify the code.



Source level debugging

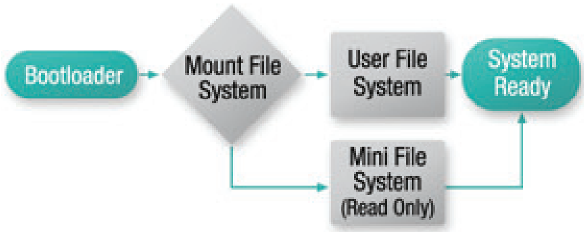
Moxa's embedded computers (UC-7400 Series, UC-7400 Plus Series, DA-660 Series, IA240 Series, IA260 Series, and UC-8410 Series) have a built-in GDB server that enables software developers to use freeware, such as DDD in Linux environments, for source level debugging.

Embedded web server for web applications

Moxa's embedded computers have a pre-installed web server daemon that lets you set up your web application easily. Edit your web application with any familiar web tool, and then download the site to the Moxa embedded computer, and enjoy the benefits of web applications that are viewable with any popular web browser.

Robust self-recovery file system

Moxa's embedded computers provide a self-recovery file system to ensure reliable operation. There are two file systems inside. One is the User File System, and the other is a Mini File System. If mounting the user file system fails, Moxa's embedded computers will auto-boot from the Mini File System to ensure a successful boot-up.



Embedded Computing with Windows Embedded

In addition to being part of the Linux community, the Moxa embedded computer family also includes models running the Microsoft® Windows® Embedded operating system.

Adopting a widely used programming environment makes our embedded computers suitable for software development and legacy system migration.

Easier Application Development with IDE Tools

Software written for the desktop PC can be easily ported to a Moxa embedded computer with very little or even no modifications. Both porting and new development can be done using any number of friendly Integrated Development Environment (IDE) tools. Choose the tools based on the application language you plan to use and install them on your development PC. For detailed installation steps, please refer to the user's manual.

C/C++ Applications:

Using Embedded Visual C++ (eVC) 4.0

The eVC 4.0 tools can be downloaded for free from MSDN's download page. Install the eVC 4.0 tools and import service pack 4. Note that eVC is used for CE versions under 5.0.

Using Visual Studio 2005 or Visual Studio 2008

Microsoft Visual Studio 2005/2008 is a complete set of development tools for building C/C++ applications. You can develop WinCE applications with the Moxa SDK using Visual Studio 2005/2008 for WinCE 5.0/6.0/XPe.

VB.NET/C# Applications:

Using Visual Studio 2005 or Visual Studio 2008

Microsoft Visual Studio 2005/2008 is a complete set of development tools for building ASP.NET Web applications, XML Web services, and mobile applications. Visual Basic, Visual C++, Visual C#, and Visual J# (XPe only) all use the same IDE, which allows them to share tools and facilities when creating mixed-language solutions.

If you are building applications under WinCE, after installing the IDE tool you will also need to install a Windows Embedded SDK (provided by Moxa) on your development PC. After doing so, the SDK will be integrated with your IDE tool.

The Win CE SDK includes C libraries and run-time libraries, Microsoft Foundation Classes (MFC), SOAP Toolkit, .NET Compact Framework, XML, and Winsock for you to develop your applications.

VPN Middleware

Unbeatable middleware for integrating application modules into proprietary systems

VPN Middleware makes it easy for users to create secure tunnels between communication parties

Virtual Private Network (VPN)

A Virtual Private Network (VPN)allows the provisioning of private network services for an organization or organizations over a public infrastructur e, such as the Internet, instead of with physical wir es. The network is said to be " virtual" because it links two "physical" networks (local area networks) using an unreliable connection (the Internet), and "private" because only comp uters that belong to a local area network on either end of the VPN can "see" the data. The technologies intr oduced today ar e applied to IP-based VPNs rather than frame relay or ATM networks.

OpenVPN

OpenVPN is one of the virtual private network (VPN) solutions that establish secure tunnels between host computers. Two networking techniques are supported by OpenVPN: Ethernet bridging and IP routing. Moxa provides a ready-to-run OpenVPN middleware to enable Moxa embedded computers to be used as OpenVPN gateways with IP routing capability.

IPsec Protocol

Internet Protocol Security (IPsec) is a suite of protocols for securing Internet Protocol (IP) communications by authenticating and/or encrypting each IP packet in a data stream. IPsec protocols provide a set of security services to create secure channels between a pair of security gateways, such as a router or a firewall. Since IPsec provides reliable encryption, integrity, authentication, and replay protection, adding IPsec to Moxa's embedded computers helps prevent threats from intruders.

Openswan

Openswan is an implementation of Internet Protocol Security (IPsec) for Linux platforms. Moxa provides Openswan configuration examples for integrators who want to use RSA (Asymmetric key cryptography) and PSK (Symmetric key cryptography) authentication algorithms to create host-to-host, subnet-to-subnet, or host-to-subnet IPsec connections.

SAMPLE CODE @ Rcore

Sample Code Makes Software Development a Piece of Cake!

In addition to being part of the Linux community, the Moxa embedded computer family also includes models running the Microsoft® Windows® Embedded operating system.

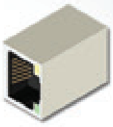
Adopting a widely used programming environment makes our embedded computers suitable for software development and legacy system migration.

LCM

The LCM Programming function helps developers easily program LCM displays on the UC-7410/7420 and DA-660 series computers.

Keypad

The Keypad Programming function helps developers easily program keypad buttons on the UC-7410/7420 and DA-660 series computers. In addition to the primary function, additional API functions are provided, such as a callback function defined by programmers to associate with an event.



Socket

Moxa embedded computers come with network interfaces that allow client-server applications to communicate with each other across a computer network. A Socket Programming function helps developers implement socket programming with TCP or UDP protocols.

Serial

In addition to the primary Serial Port Programming function, Moxa embedded computers offer higher level APIs for serial connections.

Real Time Clock

Developers can use the RTC Programming function to get the current time, set the hardware clock time to a specified time, set the hardware clock time to the system time, and set the system time from the hardware clock, by use of the function sample codes.

Buzzer

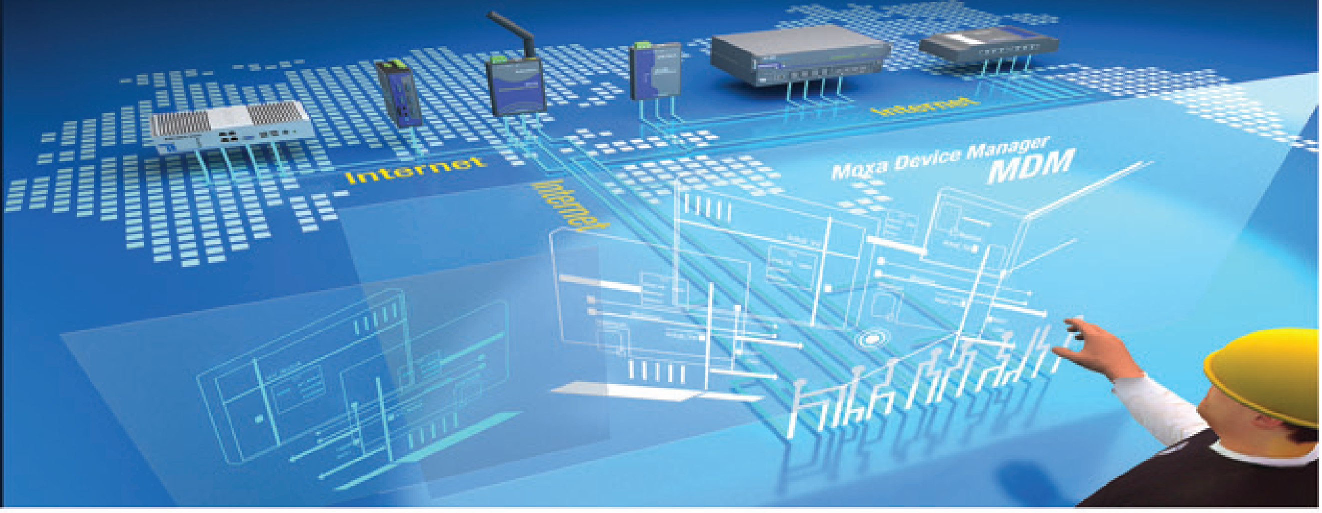
A Buzzer Programming function allows developers to trigger alarm beep for unusual events.

Watchdog Timer

Moxa's embedded computers are also equipped with a Watchdog Timer Programming function that sets the system back to normal if applications don't acknowledge.

Moxa Device Manager

Boundless Management of Moxa Embedded Computers



Systems that incorporate several devices located at remote sites present a big challenge to solution providers. This is particularly true for industrial applications that use several headless embedded computers distributed over a wide area. Although this type of computer is generally accessible from over the network, the existing remote management options present a rather clumsy solution for managing large numbers of embedded computers.

The Telnet/SSH Solution

Perhaps the most common method of managing embedded computers remotely over the network is to use Telnet/SSH. However, one of the main drawbacks to this type of management is that you can only connect to one embedded computer at a time. In addition, the administrator must actively type in the IP address of the embedded computer to establish the Telnet/SSH connection. It can be a real nightmare to keep track of which IP address is associated with which embedded computer.

The Command Line Solution

Another method of managing an embedded computer includes working from the command line. Although this can be done from over the network, most administrators find it difficult to remember all of the commands that are required to manage files and run programs. Script files that combine several commands in one text file can be used to automate the command line method, but this option can also be quite time-consuming for administrators that manage tens if not hundreds of machines.

Using MDM (Moxa Device Manager) to Manage Embedded Computers

Moxa Device Manager (MDM for short) is an easy-to-use remote management tool for managing Moxa's ready-to-run embedded computers over the Internet. Moxa's embedded computers make excellent front-end computers at remote sites for on-site data collection and industrial control applications. MDM is designed to make it easy for system administrators to manage their remote embedded computers. One of the key benefits of MDM is that management tasks, such as configuring the network, managing and/or transmitting text and binary files, and monitoring and controlling processes, can be handled easily using a Windows-based user interface. In addition, MDM can be used to manage different models of embedded computers, and embedded computers that use different operating systems, all from one centrally located computer. As long as the individual embedded computers are pre-installed with an MDM agent, they can be recognized and managed by the unified MDM tool from your PC. These features help ensure that MDM gives system integrators an efficient tool for handling all remote devices from one computer.

In addition to controlling heterogeneous computer systems, the traffic between the MDM tool and any of the MDM agents is encrypted. This feature protects data transmitted from the system. Users can comfortably manage the remote devices without worrying about the usual risks associated with transmitting data over a network.

The Benefits of MDM

Remote Control and Management

- Supports all models of Moxa's embedded computers and Linux, WinCE, WinXPe operating systems
- Control and monitor remote embedded units over the Internet
- Broadcast search for Moxa embedded computers on the same LAN
- Get instant device status
- List basic information (IP, Model, Firmware version, OS, hostname, CPU, product image, memory information, and storage information) of all devices on the main page

Easy-to-use User Interface

- User-friendly "click and operate" interface for remote device management
- Friendly windows-based utilities for easy configuration

Easy Installation and Setup

- An MDM Agent program running on an embedded computer can be started automatically at boot-up
- MDM Tool and Gateway can be installed on any PC running Windows XP

Command-line Free Configuration and Maintenance

- Launch programs automatically when booting up
- One-to-multiple file transfers
- Perform remote file system management
- Configure network interfaces
- Monitor and kill processes
- View detailed system information
- Reboot devices
- Upgrade firmware for multiple devices at one time
- Update system time

How to Get MDM

Moxa Device Manager comes with MDM Agent, MDM Tool, and MDM Gateway. Users can download the Moxa Device Manager package from the "Support --> Software" page on Moxa's website.

Web-based Management System

Moxa's embedded computers are network-centric programmable platforms designed to be used as front-end computers for data acquisition and industrial control. The embedded computer is often located away from the system administrator in the same harsh environment as the controlled devices. This makes the task of managing the computer remotely an important aspect of the embedded computer's operation.

To resolve this remote management issue and reduce the work load of the system administrator, the Moxa embedded computer is installed with a Web-based management system. The system incorporates often-used features into an internal site and categorizes the features on a menu bar, as shown in the accompanying figures.

- System Information
- Networking/Server Configuration
- Process (Thread) Monitoring/Control
- Services Monitoring/Control
- Binary/Text File Management and Upload

This web-based management system allows you to manage web sites, the registry database for system and application programs, and many other aspects of the computer's operation.

Moxa Inc.

www.moxa.com
info@moxa.com

Moxa Americas

Toll-free: 1-888-MOXA-USA (1-888-669-2872)
Tel: +1-714-528-6777
Fax: +1-714-528-6778
www.moxausa.com
USA@moxa.com

Moxa Europe

Tel: +49-89-3 70 03 99-0
Fax: +49-89-3 70 03 99-99
www.moxa.com
Europe@moxa.com

Moxa Asia-Pacific

Tel: +886-2-8919-1230
Fax: +886-2-8919-1231
www.moxa.com
info@moxa.com

Moxa China

Shanghai Office

Tel: +86-21-5258-9955
Fax: +86-21-5258-5505
www.moxa.com.cn
China@moxa.com

Beijing Office

Tel: +86-10-6872-3959/60/61
Fax: +86-10-6872-3958
www.moxa.com.cn
China@moxa.com

Shenzhen Office

Tel: +86-755-8368-4084/94
Fax: +86-755-8368-4148
www.moxa.com.cn
China@moxa.com

P/N: 1900030901010