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Is PC/104 still relevant?

By Rory Dear, Technical Contributor
rdear@opensystemsmedia.com

PC/104 is a veteran of embedded computing. Yet, with all the changes in the embedded space since its inception, does it still have a future?

PC/104 has been around almost as long as I have, conceptualized within Ampro almost three decades ago back in 1987. In 1992, the now world-famous form factor was standardized and the PC/104 Consortium was born. This revolutionary thinking created the first multi-stackable computing platform.

The backplane and slot card method, long characteristic of desktop computing, has limitations in its compactness and the ruggedness (thus reliability) of peripheral interconnects via slots – both critical aspects of embedded systems.

The format initially provided a single common bus (ISA), though PCI and PCIe capability was introduced in 1997 and 2008 respectively, following logical demand for increased bandwidth. All standard PC I/O connections were, and are still, satisfied by flying leads from onboard pin headers – a flexibility strength that has served PC/104 well over the years.

New applications for the compactness of PC/104 then emerged by the day and our industry is indebted to the success of the format by the exponential growth that it brought with it. It inspired a generation of engineers and indeed the subsequent generations of Single Board Computers (SBCs) that we see today; yet seemingly it refuses to succumb to old age and we still see new PC/104 boards released each week, albeit satisfying a smaller segment of applications than in its heyday.

PC/104’s popularity is self-perpetuating with legacy re-designs; if a mechanically identical board still exists, this cuts swathes of time and cost and PC/104 remains naturally the successor elect.

The continued availability of data acquisition peripheral cards in PC/104 format has also had its bearing; many OEMs continue to provide Analogue and Digital I/O alongside industry-specific proprietary communications interfaces as such, with the sole alternative often being our old friend the slot card.

The final aspect must be low production quantities. Low quantity, specialist product doesn’t have the room to encompass hardware Non-Recoverable Engineering (NRE) – often I see these projects not even using the peripheral bus, delivered with cropped pins. PC/104’s success in these projects is owed to its truly “off-the-shelf” nature, but the format’s success specifically must lie in the lack of a real competitor. 3.5", 5.25", EBX, EPIC, etc. are less compact and contain few benefits for many, so PC/104, for now, stays!
At lunch the other day with my friend Paul Stevens of Advantech’s Networking & Telecom Group, I asked how the Internet of Things (IoT) was impacting their datacom plans. Rifling through a Kung Pao dish riddled with peanuts, Paul responded that the IoT is nothing compared to the challenges of increased demand for video bandwidth. “But,” he said as he worked to spear one of the few scallops remaining on his plate, “it will be.”

In retrospect, networking in the IoT will be much like Paul’s lunch: fishing for key data (the scallops) in a sea of less-significant information (the peanuts), then clearing a path for that mission-critical data through the depths of phone calls, YouTube cat videos, and “House of Cards” episodes streaming over Netflix. To ensure those paths, network engineers are turning to Software-Defined Networking (SDN).

In short, SDN differs from other approaches to networking in that it utilizes a software layer to abstract the network control plane from the data plane (for a more complete overview, read “Infrastructure-as-a-Service Explained” atopsy.st/iaaSExplained). This philosophy enables network operators to better classify, group, and route various data packets, which effectively allows certain information to be prioritized so it can traverse the network more freely. In essence, this means that IoT applications sourcing status data from thousands of end nodes could flag various data sets as high-priority and send them across the lowest latency network path. It also turns traditional concepts of networking upside down in that the network is now altered based on the needs of the application, rather than the application being subject to network constraints. As network transmission costs look to be among the most expensive in the IoT infrastructure, this ability to earmark relevant data will be key to reducing Operating Expenditures (OPEX).

**SDN solutions**

Spark Integration Technologies, Inc. is a network connectivity vendor based in Vancouver, British Columbia whose flagship Distrix Gateway router is an embeddable, small-footprint SDN solution that provides IP and non-IP connectivity to existing applications and infrastructure (www.sparkintegration.com). The Distrix solution is essentially a network virtualization tool that uses a restful Application Programming Interface (API) to define and configure end-to-end tunnels at different layers of the network, from basic Layer 2 Ethernet connectivity through the application layer (Layer 7 in the Open Systems Interconnection (OSI) model).

In addition to network configuration, the Distrix API also provides Deep Packet Inspection (DPI) monitoring streams that generate a real-time heartbeat for calculating network latency. Distrix then allows the application or management system to dynamically adjust the network based on available bandwidth and route traffic over the lowest latency link.

**Spearing the scallops**

The marriage of SDN and DPI technology in a single platform yields two key benefits for IoT networks, one of which is the opportunity for data reduction or consolidation of redundant traffic. The second is the previously mentioned prioritization, which can be conducted by establishing a second, separate tunnel for mission-critical data, or by identifying a traffic flow’s source port number.

Take, for example, a modern cruise liner that streams a variety of data, including critical ship telemetry data and Voice-over-IP (VoIP) from passenger cell phones and tablets. While at sea, an SDN system like Distrix would maintain satellite connectivity for ship-to-shore communications, giving priority to alarm and control information from the ship’s telemetry data. As the ship approaches shore, however, Distrix would then pick up cheaper cellular networks and Wi-Fi hotspot connections as they became available, essentially bonding multiple types of connectivity to manage any ongoing network sessions while still ensuring a path for telemetry data.

Another benefit of the programmable network methodology found in SDN is that networks theoretically only exist based on the needs of the application, and therefore don’t necessarily have to be running 24/7, 365. Therefore, network operators can rest assured that vital information is always transmitted in real time, and also capitalize on the OPEX savings afforded by “on-demand” networks.

We’ve saved some money and sorted out the scallops. Let’s eat.
DIY and wearable sensors

By Monique DeVoe, Managing Editor

Sensors are key to making interactive systems that gather, analyze, and put to use massive amounts of data about the world around us. The Internet of Things (IoT) and wearable devices wouldn’t be nearly as enticing without the capabilities made possible by sensors, as our devices, cars, homes, and more are getting smarter and improving our daily lives thanks to the wealth of information they’re able to gather. DIY projects are also becoming more advanced and sophisticated thanks to the availability of low-cost, high-quality sensors, as well as communities that can help makers put them to use.

“There are so many great sensors coming out,” says Limor “Ladyada” Fried, Founder and Engineer at Adafruit (www.adafruit.com), an open-source DIY tools, equipment, and electronics company. “A single-axis accelerometer used to be $40. Now you can get a full 9-degrees-of-freedom sensor for $5! Incredible how the demand for sensor-enabled cell phones and wearables has increased what’s available.”

Though inexpensive and widely available with limitless project possibilities, working with sensors in a DIY project can be challenging and time consuming. Fried, who has been named Entrepreneur of the Year by Entrepreneur magazine and made many “innovator” and “influencer” lists, cites considerations such as figuring out if a sensor is analog, ratiometric, absolute, or digital I2C output, and if the sensor requires repeated start. But instead of taking the time to figure out all the details alone, Fried and the Adafruit team have a system down to help alleviate the difficulties of working with a new sensor.

“Every sensor has its own little quirks,” Fried says. “One of the things we do for every sensor in our shop is go through and make an Arduino library with a demo. That way you can get it wired and read valid data as soon as possible. Having a known-good platform is key, and an Arduino is only $30 – it’s like a universal eval board.”

Adafruit offers nearly 200 sensor parts among a variety of sensor types that are compatible with multiple platforms. In addition to selecting, testing, and designing products of her own, Fried also contributes to the Adafruit Learning System, which contains tutorials on integrating sensors into DIY projects and other maker tips in a Pinterest-style format (learn.adafruit.com). Dozens of sensor tutorials range from teaching makers the basics of different sensor types, to more advanced lessons on creating garden monitoring systems, spatial navigation systems, GPS-enabled pet collars, and biometric lockboxes with a variety of sensor components.

Where sensors meet accessories

Out of all the sensor products and tutorials available, Fried says those related to wearables are the most popular.

“We have hundreds of tutorials on using sensors, but our most popular ones by far are the wearable ones,” Fried says. “The best place to see the cool future of DIY sensors is wearable electronics.”

The possibilities of wearables go way beyond the traditional smartwatches and fitness bands that have recently exploded in popularity. The Adafruit team, for example, used a TAOS TCS34725 RGB color sensor with an IR filter that detects light bouncing off an object to make color-changing accessories (Figure 1). Another example would be a wearable accessory with a UV sensor that detects when it’s time to put on a hat. In addition, Adafruit has a whole #WearableWednesday blog and video series and its own FLORA and GEMMA DIY wearable platforms.

A better feel on future sensors

Though sensors have come a long way, there are still opportunities to bring certain capabilities down in scale and increase their availability to the general public. For example, Fried sees gesture-sensing capabilities like those of the Xbox Kinect as an area that could use more work.

“A low-power Kinect-type sensor, something you could power off of 3 V and small enough to embed into anything would be so great,” Fried says. “People love the idea of gesture and location-mapping sensing.”

With how far sensors have progressed in the last decade, it’s exciting to think of what new sensing capabilities will become widely available next for makers. ECD
Accelerating processing with Course Grain Reconfigurable Arrays

By Monique DeVoe, Managing Editor

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RESEARCH REVIEW

With increasing performance demands and a push for lower power designs, more efficient methods to perform processing tasks are needed, as throwing more processors at performance issues is no longer viable due to power constraints. Accelerators aim to do computations faster and with lower power consumption, but today’s accelerators have shortcomings in power consumption and performance.

The accelerator lineup

Aviral Shrivastava, Associate Professor at Arizona State University’s School of Computing, Informatics and Decision Systems Engineering is conducting research into programmable accelerators to enhance today’s acceleration technology. Shrivastava lists three common types of accelerators in use today: hardware accelerators, FPGAs, and GPUs. Hardware accelerators dedicate specific compute elements to processing calculations rather than running them on the CPU. They are fast and low power, but not suited for today’s quickly changing technology iterations as they aren’t programmable. FPGAs are programmable—developers can program any logic onto them and they can act as accelerators—but Shrivastava says they’re often too generic and consume too much power. GPUs are popular accelerators today, but they can only accelerate parallel loops, and not all applications use parallel loops.

Course Grain Reconfigurable Arrays

Shrivastava is working on developing Course Grain Reconfigurable Arrays (CGRAs) that can accelerate non-parallel loops and enable more accelerating functionality on top of GPUs’ parallel loop strengths. CGRAs consist of a two-dimensional mesh of Processing Elements (PEs) made of Arithmetic Logic Units (ALUs) and registers that receive input and instructions, compute the instructed arithmetic or logic operation, and send the output to its four neighbors to compute the next step.

CGRAs’ potential comes from their ability to perform an operation while spending very little power. Executing an addition operation in a regular processor requires a lot of power: it has to flow through more than 20 stages of pipeline. In a CGRA, power is needed only to get the operands from neighbors and to perform the addition operation. CGRAs can accelerate by pipelining—the operations of the loop are laid out on the PEs of the CGRA, and the data flows between them.

CGRAs themselves aren’t new, but developers program existing CGRAs to do only one type of computation. The challenge is in mapping, Shrivastava says, as loop kernels need to be mapped onto the CGRA, operations mapped to nodes, and data dependencies mapped onto the CGRA’s paths. Shrivastava’s goal is to remove time-consuming manual coding and enable any type of loop or computation to be mapped to the CGRA by a compiler, a relatively new method. He is developing a compiler toolchain that generates mapping code.

Shrivastava says the CGRA research has interested IBM, who wants to apply this sort of method to parallel-loop-light server applications. Graphics and high-performance computing for scientific research and multimedia extensions can also gain from using CGRAs.

Taming the branch divergence problem

A challenge faced by all existing acceleration technologies is that of “branch divergence.” When executing a loop that has an “if-then-else” construct, the accelerator allocates resources to execute instructions from both paths of the branch—the true path, and the false path—then discards the effects of the false path’s instructions. FPGAs map the functionality from both paths on computational resources, and GPUs execute instructions from both branch paths and discard the results of the false path instructions. Accelerators have to do this because the outcome of the branch is not known at compile-time when branch path resources are allocated (the outcome of the branch is computed at runtime, when the branch is executed). This redundant execution causes the branch to take double the performance time and power to execute.

In a paper accepted at the Design Automation Conference (DAC) and set to be published in June, Shrivastava and his team propose a solution to the branch divergence problem through smart hardware-software co-design. Instead of allocating some PEs for the true path and some for the false path, the same PEs are assigned to execute instructions from both paths. The instructions from both the true path and from the false path are issued to the PE. At runtime the PE selects only the correct one to be executed.

For more information visit aviral.lab.asu.edu/?page_id=1533
I2C bus buffer
ASSPs address wide-voltage-level translation ranges

By Peter Stonard

The technological trend in Microcontrollers (MCUs) and related devices is smaller geometry, and with that the need for much smaller operating voltages. Circuit designers are challenged to connect low-voltage signals to the wide variety of other device voltages. The I2C Bus poses a unique problem to these efforts with its defined protocol and bidirectional signal flow. Integrating a level-translating bus buffer Application Specific Standard Product (ASSP) can address this issue, but comes with its own set of obstacles.

The latest embedded computing devices have lower supply voltages due to advancing technology in semiconductor fabrication. This is creating smaller transistor geometries, which in turn means lower breakdown voltages. As a result, signal swings are now much smaller than before, to as low as 1 V (Figure 1).

For a pure digital signal there are several interface devices available that can translate the smaller signals to higher swings for CPU output ports. Similarly, these same devices can be used to step down existing signals to smaller and safer inputs for a new low-voltage core. For instance, Voltage-Level Translators (VLTs) address any mismatch of signal operating voltages, but bidirectional VLTs are tricky to design. Application Specific Standard Products (ASSPs) address the problem.

**I2C bus basics**

The I2C bus relies on two electrical connections and two external resistors for full bidirectional signaling. The protocol is comprehensive, allowing multiple nodes to act as both transmitter and receiver while avoiding bus collisions thanks to a simple and reliable multi-master arbitration.

The flow of data on the I2C bus is controlled by the master, which supplies a clock signal called the Serial Clock (SCL). Data is passed along a second electrical connection, called Serial Data (SDA), and data on SDA may flow from the master to the slave, or in the other direction.

A unique feature of the I2C bus is the Wired-OR logic connection of nodes. When the bus is idle, none of the nodes draw current and the bus signals are held at logic 1 (typically +5 V) by the pull-up resistors, one each on the SCL and SDA. Signals are asserted by a node pulling these lines low through an open-drain driver (though older devices built on bipolar technology use an open collector device for the same outcome).

**Figure 1**

Shrinking transistor geometries are resulting in lower breakdown voltages and smaller signal swings than in the past.
The master initiates each data transaction, and the responding node pulls the SDA line low (the responding device may also pull the SCL line low, but this mode, called “clock stretching,” is rarely used).

**Bidirectional Voltage Level Translators (VLTs)**

There is no hardware flow control in the I2C bus protocol, which makes VLTs protocol agnostic but also creates a circuit design challenge (Figure 2).

Data flow direction changes on the I2C bus often occur frequently, in fact after each eight clock cycles or the delivery of one byte of data. The ninth clock period reads the slave device to confirm the sent data has been understood. During the ninth clock period the master looks on the SDA line for either a logic 0 acknowledge (called “ACK”) or a logic 1 not acknowledge (called “NACK”). It falls to the VLT to pass these signals back and forth reliably.

In the first generation of VLT designs, the typical voltage step was from 5 V on the high side to 3.3 V on the low side (usually the side with new technology). A common and low-cost translation solution was the single Field-Effect Transistor (FET) device (Figure 3).

Limitations creep into this topology. While the single FET can pass signals in both directions, with appropriate VLTs there’s no isolation. Loading on one side has to be carried by the other side, putting a limit on their appeal. Worse yet, the available low-cost FETs are not well suited to these lower bus voltages. Imagine the case of a 1 V to 2.5 V interface required for connecting a CPU core (1 V signals) to the controller seen in a DDR4 RDIMM design (a 2.5 V part). FETs with lower gate thresholds are necessary and available – for a price – but I2C bus buffer ASSPs can also address these lower bus voltage designs. A superior solution to FET-based VLTs is the I2C bus buffer ASSP.

**I2C bus buffer Application Specific Standard Products (ASSPs)**

ASSPs to support I2C expansion have been around for a while, and newer designs address VLT over an impressive range, including the next generation of CPUs and Systems-on-Chip (SoCs) that run on only 1 V supplies. Because ASSP devices are buffers, they separate loading to each side of the I2C bus buffer. This is important for not burdening the CPU or the SoC’s I/O pins, and allows for the attachment of even more nodes on the other side of the buffer device; for example, new smart phone and personal electronic architectures have many more sensors (nodes) that are attached to the I2C bus.

Caution is needed when adding any bus buffer to a design because these devices must manipulate the bus voltage levels to avoid a deadly bus lockup condition. Simply put, an I2C bus buffer must determine if a low on side “A” is from its own output (that is, the buffered low coming in on side “B”) or another external device on the side “A” bus.

---

**Figure 2**

Hardware flow control does not exist in the I2C bus protocol, which creates a circuit design challenge.

**Figure 3**

Using a Field-Effect Transistor (FET) and passive Voltage Level Translators (VLTs) is one common, relatively low-cost voltage-stepping solution, though it comes with limitations.
Bus buffer designs use one of a handful of techniques that change the bus buffer’s output voltage. In one such method, a small offset voltage is added that is small enough to not interfere with other devices on the bus but big enough for the bus buffer to know the difference between an external (and much lower) signal from another node on the bus, as well as its own logic 0 signal. A typical static offset is only 90 mV.

Bus speed improvements
While early I2C buses moved at modest speeds (clocking in at 100 kHz or less) and served the applications of the day, newer applications demand more data throughput and therefore faster clocks. The current I2C specification, which defines the timing of signals, has added several new clock speeds up to 1 MHz. Called “Fm+” (Fast mode plus), these clock speeds are 250 percent faster than the previous Fm (Fast-mode) speed increase that limited clocks to 400 kHz.

Keep in mind that it is the action of the bus master – often a function already built into the MCU, CPU, or SoC device – that determines the bus clock speed. Slave devices and bus buffers don’t generate clocks, and don’t care about clock accuracy; an 800 kHz bus clock might actually operate with a 20 percent tolerance. To increase speed the bus loading (capacitance) must be reduced. Bus buffers split the bus and isolate capacitance for each segment.

Increasing the clock frequency is not without its hardware challenges. Untamed faster clock and data transitions will likely cause ringing and undershoot, because the I2C bus is not a transmission line and does not have adequately small termination resistors to dampen fast signal edges. The I2C specification puts limits on both the rise time and fall time of edges.

Rise times of the bus segments are set by the system loading capacitance, which is the sum of node and interconnecting signal trace capacitances. Board-level circuit designers only have freedom to select the I2C bus signal pull-up resistors.

When the I2C bus is driven by modern high-performance digital devices (CPU, MCU, and SoC types), care is needed to slow down the falling edge of both the clock and data bus signals generated by these lightning-fast devices. If necessary, an external series resistor should be added to work with the stray capacitance to create a controlled fall time and dampen any ringing on the I2C bus segment. Alternatively this can be achieved by adding a small capacitor.

If a design needs more data throughput and newer technology components that operate from lower supply voltages, expect to add an I2C bus buffer to your design (Figure 4). Treat the two sides of the I2C bus buffer as separate buses, and choose pull-up resistors to suit.
Application Specific Standard Products (ASSPs) control many basic functions of embedded systems, and work well when customization isn’t necessary. Microcontrollers (MCUs) that are optimized for specific system applications can provide designers with more options for customization and differentiation. *Embedded Computing Design* spoke with Mike Copeland, System Applications Manager and Principal Engineer, Industrial Microcontrollers and Motor Control Systems, Infineon Technologies about the role of ASSPs and application-optimized MCUs in embedded computing. Edited excerpts follow.

**Q** What is Infineon’s take on the Application Specific Standard Product (ASSP) market? What applications are driving their use?

We do see widespread adoption of ASSPs in the power supply portion of many applications. In general, ASSPs are selected when the innovation in a project does not arise from the function provided by the ASSP. This may be in well-established product categories where the differentiation isn’t in the chip-level feature set. In emerging product categories or existing categories that are evolving rapidly, the project team is more likely to look at an application-optimized Microcontroller (MCU), which lets designers add their own “secret sauce” in the software and hardware.

**Q** How do ASSPs address the needs of embedded device design teams’ goals? When are they most useful? When are they not useful?

ASSPs can jump-start a product design project, but the design team is limited to the fixed functionality of the device. While some ASSPs include an MCU or programmable elements, the available resources are typically limited or the full capabilities of the MCU are not exposed.

Markets with fewer “standards” tend to use application-optimized MCUs. This can include both high-volume and relatively small application segments where there is a lot of room for design innovation. For these areas, an application-optimized MCU such as the Infineon XMC family combines general-purpose or even application-specific features as peripherals on the same silicon die, and provides programming flexibility to add differentiation in the hardware/software design.

Looking at ASSPs and MCUs, the processor choice will vary even within a product category. For example, there are good ASSPs for straightforward power conversion or simple motor control systems. But if the design team is pushing the envelope for overall efficiency or control precision, then an optimized MCU offers the right combination of programmability, cost, and design time advantage.

Infineon designed its XMC application-optimized MCUs to address these limitations. Each device family is based on a different 32-bit core – the ARM Cortex-M4 for the XMC4000 and the ARM Cortex-M0 for the XMC1000. Both product families are optimized for industrial applications, such as drives, factory automation systems, lighting control and renewable energy systems. Examples of this type of optimization include implementing a Pulse-Width Modulation (PWM) unit with resolution down to 150 picoseconds; the high accuracy helps improve efficiency in power applications. The peripheral set includes 12-bit resolution ADC modules, with up to four available on our higher-end devices, specialized math units, and timers. Another example is error correction in flash memory, which relates to safety issues in factory automation.

Equally important to the concept of application optimization is that we make these features very easy to program and give designers complete access to the MCU core and peripheral code.
We implement a flexible gating structure for all peripherals that can power down any component not used. You can set up the application to never power up portions of the chip, even during boot, which saves the kind of in-rush power drain at startup that's common to many systems.

The typical approach to application support is to offer sample code and libraries that a design team can plug in to its project. We decided that an ecosystem for application-optimized MCUs had to offer more, which led to a very powerful development environment called DAVE, or the Digital Application Virtual Engineer. It supports component-based programming where the developer configures and combines different elements — like ADC and PWM generation. The various hardware elements and software components — called DAVE Apps — are combined without touching the source code. The next step is to map the defined components to the XMC hardware. The tool suggests the specific chip resources to use and can even suggest the pinout. For example, it says that a specific analog to digital channel can use pin 12. When the developer is satisfied with the configuration, the environment automatically generates the C code for compilation in any tool chain.

With this approach it's much easier to combine and configure available components compared to editing the source code. Constrained logic handles potential device conflicts and greatly simplifies set up of the real-time operation. It handles potential device conflicts and greatly simplifies set up of the real-time operation. It also allows peripherals/gates to be shut off if not needed.

A good example of this is motor control for a cooling fan application. Perfectly good ASSP solutions are available. But if there's a requirement for very high efficiency and super quiet operation, then a dedicated effort to implement optimized control, variable speeds, temperature sensitivity, and other features is best served with an MCU-based approach. Similar examples apply in lighting design, renewable energy, and high resistance to shock and vibration allow it to excel in harsh environments, such as vehicle applications.

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EDA and the cloud

By Curt Schwaderer, Editorial Director

The effect of the cloud can be seen everywhere, in just about every industry. I had the opportunity to talk with Larry Drenan, Services Group Director with Cadence Design Systems, about the current state of EDA as well as trends and thoughts on EDA relative to the cloud.

“The thing that’s always driving EDA is the next-generation designs,” Drenan says. System-on-Chip (SoC) designs tend to advance quickly. The main drivers are trying to keep up with the always-changing requirements of these advanced designs.”

There is a trend of an increasing amount of Intellectual Property (IP) from multiple parties involved in making most large designs these days. When there is third-party IP involved, it’s important to treat third-party IP in a secure manner. Today’s SoC designs are so large you don’t have the time to do it yourself, so there are a lot more third party capabilities being incorporated into those designs.

Hosted EDA design resources

The Cadence (www.cadence.com) Hosted Design Solutions provide software licenses, equipment, CAD, and IT support to facilitate customer designs. This isn’t a cloud service per se – it’s access to EDA design center resources where designs can be developed and tested. Cadence runs these services out of a number of large design centers in various countries around the world. Customers can plug into these development teams with established processes and not have to buy capital equipment or incur long, expensive set-up time. The main advantage is a known-good environment that can be used right away. Customers focus on designing chips and Cadence takes care of the process, materials, and resources. Cadence has been offering hosted design services for about six years now. It’s not a large part of their business, but as design complexity increases, hosted design services become a more attractive option.

Drenan mentioned companies of all sizes utilize hosted design services. Small companies may want to do something new, and having the latest capabilities available without investment is attractive. Medium and large companies can utilize hosted design services as a more cost-effective option versus starting a design center in a different region. Or sometimes there is a new project that would be more advanced than anything they’ve done before. The Cadence Hosted Solutions option provides lower investment in new equipment in order to execute on the project.

Once the customer uses the design services, they typically handle their own process/foundry relationship. Once the design is done, companies can download the resulting package to the foundry. This foundry information is valuable, and it’s important that the package not be exposed to others using the same hosted services. Cadence assigns an independent “chamber” for each customer. The chamber is a secure area distinct from other customers that provides data security. Only people approved by the company owning the chamber can have access to it.

When asked about the business model of using the hosted design services, Drenan mentioned two options:

› “Electricity model” – the customer is billed at the end of each month based on resources the customer has used
› “Hotel model” – at any given time, the provider of the resources allocates some amount of disk space, licenses, and equipment over the course of the project

The hotel model estimates what kinds of resources are needed month-to-month and the monthly charge is set accordingly. This may ebb and flow over the course of a project. For example, when companies are going through the tape-out process, they need more equipment and disk space. Based on agreeing to provide a designer the capabilities, Cadence offers a fixed price by month. Drenan was quick to point out that when it comes to chip design estimates can be wrong, so if the company is running early or late, the billing can take that into account and adjust the resources and billing accordingly.

When asked about any kind of ISO processes or certifications, Drenan says Cadence participates in security assessments. And although they follow ISO and security standards in the 2700 series, they aren’t directly certified by independent third parties. They follow those standards and work with customers if they need those certifications. Cadence doesn’t get certification because each foundry wants to evaluate their processes anyway, so the certification doesn’t really help.

Cadence uses the “chamber” isolation model with a number of foundries and this has been certified and familiar with security models, so there is a comfort
level among foundries. There have been instances where a contract called out the need for ISO-27001. So, working with the customer to get the proper certifications is possible on a case-by-case basis.

Cadence is making a significant investment in building their own IP portfolio and many hosted projects use that IP as part of their contract. There is still a large market where many players and people bringing in their own IP. Drenan mentioned that Cadence often has to make a security presentation with those third parties in order to assure separation.

**Leveraging the cloud**

Drenan says that many customers are looking to use the cloud and are coming up with concepts and designs. Cadence is evaluating how the cloud can be leveraged for its own purposes.

“Everyone sees the potential, yet everyone [also] sees the problem where people are taking things like 100 CPUs and 30 terabytes to use,” Drenan says. “It’s getting more capital-intensive – people are hoping that the cloud can provide solutions there.” However, from what he can see, it fits from the cost perspective, but people are still working out the issues on how to do a large percentage of designs using the cloud model because of possible security issues and resource issues. Cloud security is getting better and improving constantly – at least from the top vendors. But you have to convince not only your team, but also your IP vendors, of the security. There may be models where you do things yourself, but go to the cloud to get extra compute power.

The challenge of bringing terabytes of libraries and test cases to a different place is problematic. People are working on and thinking about these kinds of issues, but it’s still a ways off. There is certainly motivation, and EDA vendors that are working in the cloud are now working on parts of the design where this is less of an issue – for example, highly mathematical simulation. In this situation you don’t have to carry data around or worry about third parties.

There is some FPGA design happening in the cloud. A large Altera or Xilinx design has the same resource and security concerns, but for smaller scale FPGA designs the cloud is viable.

**A potential future in the cloud**

Drenan says Cadence EDA is driven heavily by their customers’ “care-abouts.” Cadence sees customers are doing work in the cloud and trying to figure it out. At this point the cloud is not making their customers’ top three care-abouts. Customers’ priorities always vary by project, but accuracy, faster simulation, and ability to handle new foundry processes are higher priority concerns for many projects. So at this point that’s where the most Cadence brainpower is focused.

Developers are dabbling in aspects of cloud services for EDA designs, but the massive data storage and I/O requirements for large-scale designs are currently problematic. Part of the challenge is to gain acceptance from designers and third-party IP vendors by establishing a comfort level with the security, performance, and storage capabilities available in the cloud. As these concerns are better understood and deemed acceptable by all parties within the EDA ecosystem, the cloud will evolve to provide more service capabilities within the EDA world.
Managing SoC complexity with scenario model verification

By Thomas L. Anderson

Developing a System-on-Chip (SoC) requires managing many complex aspects of design. The sheer number of transistors is overwhelming, but complexity is not just about quantity. An SoC contains highly sophisticated features with precise functional specifications and an array of requirements. In addition to the complexity of the design, verification that each of the features and the entire SoC meet their specifications and requirements is also a huge challenge.

Beyond design and verification complexity, project management of the overall process is daunting. No single solution can address all, or even most, aspects of SoC complexity. However, some techniques can tackle specific parts of the problem such as with graph-based scenario models, a formalism that directly reduces verification complexity while providing side benefits for managing SoC design and project complexity.

SoC verification
The role of graph-based scenario models can be illustrated in the context of an example digital camera SoC design (Figure 1). The raw image is captured from a Charge-Coupled Device (CCD) array (front or back) by the camera block. It can be displayed for the user, manipulated by the photo processor, transmitted via a USB port, or saved to an SD card. A series of such images may be treated as a video stream and handled similarly by the video processor and the other Intellectual Property (IP) blocks in the SoC.

The SoC has intertwined data flows and supports some parallelism. With two embedded CPUs, it’s possible to simultaneously program multiple IP blocks. Further, if the fabric has crossbar capabilities, multiple data flows can run in parallel between different IP blocks and memory, or directly between IP blocks if a memory buffer is not needed. Verification requires that all these possible flows be exercised, in parallel when the architecture supports it, in ways that mimic the actual end use in the camera.

The verification team must understand all of the data flows and all possible interactions if it is to develop a testbench environment. Treating an SoC purely as a black box does not provide adequate verification; it’s hard to stimulate deep behavior in a large design strictly by manipulating the inputs. Thus, SoC verification teams almost always develop C tests to run on embedded processors as part of their methodology. Of course, hand-writing tests is also difficult, and it’s virtually impossible to hand-write tests for multiple processors that coordinate with each other and the testbench to fully exercise the SoC.
Graph-based scenario models

The verification team faces a challenge in understanding all the possible behavior and data flows within the chip. A paper specification is hard to digest and subject to all the imprecision of a natural language. Attempts to describe a full SoC using purely formal methods have been unsuccessful due to the description’s complexity and the fact that not all design types are a good fit for declarative languages.

One method gaining acceptance is the graph-based scenario model. Such a model is a formalism – a directed graph – but does not require a formal language. It can be described using the standard C/C++ language plus a few constructs from the standard Backus-Naur Form (BNF) notation. The graph shows interconnections and legal data flows among IP blocks in the SoC. A scenario model looks like the data flow diagram that an SoC architect might draw on the board, except that it is drawn with outputs and outcomes on the left and inputs on the right.

As shown in Figure 2, possible end-user scenarios include:

- A raw image read from one of the CCD arrays and displayed on the screen, written to the SD card, or sent out the USB port
- A raw image read from one of the CCD arrays, encoded to JPEG by the photo processor, and written to the SD card or sent out the USB port
- A series of raw images read from one of the CCD arrays, encoded to MPEG by the video processor, and written to the SD card or sent out the USB port
- A raw image read from the SD card or USB port and displayed on the screen, written to the SD card or sent out the USB port
- An MPEG stream read from the SD card or USB port, decoded by the video processor, and displayed on the screen, written to the SD card or sent out the USB port

Because scenario models are hierarchical, each graph node (goal) in Figure 2 can be expanded to show details of the corresponding IP block design. The model can be developed top-down by the SoC team or bottom-up by the IP developers. Top-down development is more common since projects usually start using scenario models to address full-chip SoC verification. This may require some involvement from IP developers to fill in lower-level details. If a project fully embraces the methodology, then scenario models are also used to verify individual IP blocks and then combined into a full-chip model.

The scenario model provides insight into the SoC design and the verification space that must be covered before the

![Figure 2](https://www.embedded-computing.com)

A high-level scenario model for the digital camera SoC.
chip is fabricated. This addresses verification complexity by helping define the test plan. The scenario model also helps to address design complexity since it is much like an expanded version of a data flow diagram that the chip architect might draw to explain how the design works. Thus, the graph becomes a common model that can be used among architects, designers, verification engineers, embedded programmers, and the bring-up team. This reduces project management complexity as well, both within a single project and across multiple projects that share parts of the design.

**Automation with scenario models**

Perhaps the greatest value of a graph-scenario model is that it can be used to generate C test cases to run on embedded processors in simulation, In-Circuit Emulation (ICE), Field Programmable Gate Array (FPGA) prototypes, or the SoC silicon in the bring-up lab. A generator walks through the graph from left to right, from desired results to inputs, assembling a series of steps that work back to the set of input values required to produce a particular outcome. Graph decision points and data values are randomized so that each walkthrough produces a unique test case. This automation eliminates the need to hand-write tests at any stage of the SoC project, from simulation all the way to the lab. Users report that they can achieve better, automated results using 20 percent of the team formerly used to hand-write tests, freeing the remainder to work on applications and other revenue-generating software.

Constraints can be added to graph to block paths that are illegal according to the specification, wall off portions of the design not yet ready to be verified, or bias the test case generation in certain directions. For example, the graph shown in Figure 2 allows the scenario of a raw image being read from the SD card, processed by the photo processor, and then displayed on the screen. This is an unnecessary step because a raw image can be displayed directly; the user can easily add a constraint that only JPEG-encoded images are sent to the photo processor to eliminate unnecessary tests.

Generated test cases are multi-threaded and multi-processor, with all communication across threads, processors, and the testbench built in. The goal is to stress test the SoC with the maximum amount of traffic and parallelism allowed. In the camera SoC, it might be possible for a camera image to be written to the USB port at the same time that a previous image is read from the SD card and displayed on the screen. This level of activity is unlikely to occur with hand-written C tests or a traditional simulation testbench and therefore provides a more complete verification of the design.

**Putting it all together**

As with any automatic test generation approach, the SoC team needs a way to assess the thoroughness of the verification and determine when to tape out. In addition to capturing the design and the verification space, the scenario model also serves as the system-level coverage model. Because of the definitive nature of walking through the graph, verification engineers know at test-case generation time precisely which end-user scenarios (paths) and goals in the graph have been covered. They don’t need to collect and consolidate run-time coverage to assess verification progress. More importantly, they can avoid spending weeks running additional simulation tests that add little if anything to coverage results.

Scenario models and automatic test case generation form a closed-loop coverage system. A verification engineer can point to any uncovered path or goal and the generator will produce a test case that will cover it. The same applies to cross-coverage spanning paths or goals. The TrekSoC family of products from Breker provides closed-loop coverage and the other benefits of scenario models.

Graph-based scenario models capture critical design and verification knowledge, enable better communication among SoC project team members via common models, reduce manual effort at multiple points in the process, accelerate the schedule, and verify the design more completely to increase the chances for first-silicon success.

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Functional and performance verification of SoC interconnects

By Nick Heaton and Avi Behar

Verifying interconnect Intellectual Property (IP) – the “glue” that holds together the cores and IP blocks in a System-on-Chip (SoC) – has become more complicated with advanced SoCs, which require special interconnect IP to perform the on-chip communication function. As a result, functional and performance verification of these SoC interconnects has taken on a new level of complexity. Tools have been developed to simplify verification while providing design engineers the ability to find and fix interconnect problems much earlier in the design cycle.

Remember the days when engineers used to be able to rely on buses to perform the on-chip communication function in chips? Those days are clearly in the past, especially as our increasingly connected world demands so much more functionality from our chips. Today’s advanced SoC calls for an interconnect to serve as the communication hub for various IP cores within the SoC. Verifying the functionality and performance of SoC interconnects can be a complex task, given the amount of masters and slaves, the different protocols, different types of transactions, and multilayered topology involved. A more holistic approach using tools and technologies can simplify the process of verifying the functionality and performance of SoC interconnects.

Preventing surprises with functional verification

With functional verification, designers want to ensure that the multicore chip implements the functions needed, while handling errors in a relatively smooth manner. From a practical standpoint, designers want to verify the SoC IP blocks together with the chip’s interconnect. There are two steps here. First is verifying that the IP blocks implement the given interface protocol correctly via verification IP, which can alert to any protocol violations. Verification IP monitors simulation results and performs corner-case testing against the protocol specification; during this process, verification IP with embedded assertions can automatically detect protocol violations. Furthermore, test suites and verification plans in the IP can move the verification process quickly to closure.

The second step in verifying the IP blocks with the interconnect is to verify that the commands and data will arrive at the proper destination and in the right format. Designers will want to look out for issues such as data splitting, upsizing, and downsizing. This is important because different interfaces on the interconnect subsystem are using different protocols; for example, a data transaction that entered the interconnect as a series of APB transfers can come out as an AXI burst at the destination port. Operations such as snoop conversations, snoop propagation, snoop filter operation, and cross-cache line should also be verified. In other words, they should be sure that the cache-coherent interconnect performs its role as the coherency manager correctly. To save remote memory access time, the coherent interconnect snoops the caches of relevant masters and, based on their responses, determines whether to return the requested data from the cache or from the remote memory, and updates the cache line status of the relevant masters accordingly. This behavior is defined by the coherent protocol. If the interconnect isn’t following the protocol, the system would soon enter a non-coherent state and most likely crash.

Meeting bandwidth and latency targets with performance verification

Performance verification is where designers should make sure that the design will meet its targeted bandwidth and latency levels. Consider an SoC design with multiple interconnects to prevent localized traffic from affecting the rest of the device’s subsystems. Interconnect IP plays an important role here, as it can tune each port for unique bus widths, address maps, and clock speed. Usually, there are also mechanisms to adjust bandwidth and latency to tune the interconnect IP in each domain.

However, there are still instances where traffic conflicts will occur, as shown in Figure 1. How can traffic in these situations be balanced? Most systems don’t have enough main memory bandwidth to accommodate all IP blocks being active simultaneously. What’s important is preventing one IP block from...
dominating and overwhelming the others; otherwise, system performance degrades. Performance analysis can be helpful in this situation, minimizing the impact of system performance degradation.

To analyze performance, designers need to compare bandwidth and latency measurements from different SoC architectures or different SoC use cases. This comparison involves modeling, running simulations on, and measuring performance of two or more (typically several) SoC architectures (or implementations of a specific architecture), which is not practical to do manually. After all, a manual effort would entail building testbenches around various SoC architectures under comparison. In the case of complex SoCs – where performance analyzing and tuning are most important – creating the requisite testbenches can easily take a few days for an experienced engineer and much longer for the less experienced.

**Five important areas of focus for performance analysis**

To make performance analysis as effective and efficient as possible, there are five aspects you should strive to integrate into the process:

1. **Cycle-accurate modeling** – With cycle accuracy, the logic simulation yields the same ordering of events with the same timing as will be seen in the actual chip. Cycle-accurate simulation models include the RTL-level Verilog or VHDL created during the SoC design process.

2. **Automatic RTL generation** – Automatically generated interconnect RTL is a step toward creating a full SoC cycle-accurate model. To determine the combination that provides the best overall performance, designers need to be able to quickly generate multiple variations of the interconnect IP.

3. **Verification IP** – As previously discussed, verification IP helps find protocol violations.

4. **Testbench generation** – Generating testbenches automatically saves several weeks that development can otherwise take to create a test environment for interconnects.

5. **In-depth analysis** – The ability to gather all simulation data – design assessment, the testbench, and traffic – is necessary to debug performance problems and determine how design changes might affect bandwidth and latency.

**Graphical interconnect simulation comparison**

A tool has been developed that provides a graphical way to compare interconnect simulation runs, for quick and accurate assessment of interconnect performance. Cadence Interconnect Workbench helps find and fix interconnect problems earlier in the design cycle to achieve the bandwidth and latency levels that the SoC requires. Using the tool, whose flow is illustrated in Figure 2, engineers can throw aside cumbersome spreadsheets and take advantage of a GUI with built-in filters to select masters and/or slaves and the path(s) to evaluate and perform “what if” analyses. The GUI makes it fast and easy to get a view into how design changes impact bandwidth and latency for the simulation results of interest. For example, engineers can compare and find the ideal configuration for a particular use case, or for multiple use cases running on a single configuration. They can quickly see what proportion of traffic goes to each slave and what their latency distribution looks like. Live filtering and analysis features eliminate what can be a very cumbersome process with spreadsheets.

Interconnect Workbench integrates with Cadence Interconnect Validator, a verification IP component that collects all transactions and verifies the correctness and completeness of data as the data passes through the SoC interconnect fabric. Interconnect Validator connects to all of the interface-level verification IP instances (which are monitoring the correct protocol behavior of the IP blocks) and, therefore, has a deep understanding of the data and commands coming in and out of the interconnect. By matching this data, the tool can verify if the data is being delivered to the right destination. If an interconnect doesn’t follow the protocol it issues an error.
Efficient and effective interconnect verification

With incessant time-to-market pressures and increasingly complex SoC designs, it'd be hard to find an engineer who doesn't want to shave off time from his/her design cycle. Particularly at advanced nodes, verifying SoC interconnects has become a time-consuming step. However, tools can now perform cycle-accurate performance analysis and verification of interconnects efficiently and effectively.

Figure 2

The flow of data through Cadence Interconnect Workbench. On the left, RTL, verification IP, and traffic pattern descriptions move into the tool, which automatically generates a testbench for simulation. The tool also generates other testbenches as other variations of the SoC are generated. The performance GUI provides an overview of simulation results.

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<td>Image sensor and display technology innovations have impacted many market areas. Industrial and automotive to energy and automation are leveraging mobile semiconductor device technology cost, power, and form factor advantages and FPGA-based solutions.</td>
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<td>opsy.st/FPGAandEDAAdvances</td>
<td>The ever-shifting SoC, IC, PCB and electronic systems design paradigm is burdened with numerous challenges that make an engineer’s job complicated. Five industry experts discuss the industry, trends, and how these challenges are being solved.</td>
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<td>FPGA vendors striving to make their devices more SoC- and ASIC-like collaborate with EDA companies to seamlessly integrate their tools, leading to benefits new capabilities in ESL synthesis, IP integration and re-use, and higher-level tools for software/hardware co-design.</td>
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<td>Internet of Things, wearables, and smart analog designs are seen as extremely complex due to their mixed-signal aspect. Some myths about mixed-signal designs make the process seem harder than it is, but ARM and Cadence dispel these myths.</td>
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**Introducing Design-for-Yield (DFY) and high sigma analysis**

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Slimmer and more flexible than the current Mini PCI Express (mPCIe)/Mini-SATA (mSATA) standard, M.2 does not introduce new signaling systems but rather allows for increased data throughput via multi-lane PCI Express (PCIe), and backward compatibility via SATA and USB signals. While driven by the demand for high-speed, high-capacity storage in ultrabooks, tablets and portable devices, M.2’s space-efficient form factor, backward compatibility, and flexibility mean it will have an impact on the embedded sector as well.

The unique needs and requirements of embedded customers make the adoption of M.2 a more complicated decision in this space than on the consumer side, but understanding the background of the technology, its specifications, and benefits can help embedded OEMs and system designers make the right choices now and prepare for the future.

mPCIe/mSATA

The current generation of small form factor expansion modules for both storage and general peripherals uses a common 30 mm x 50.95 mm mPCIe card form factor (Figure 1). Designed originally for the notebook market as an evolution of MiniPCI, mPCIe is a physical and electrical specification for expansion cards allowing Wi-Fi, Wireless Wide Area Network (WWAN), and other add-on functionality via a miniaturized PCIe connector. mPCIe’s widespread adoption in consumer applications, small form factor and its use of the familiar PCIe bus meant it naturally became a convenient and space-efficient way to add functionality to industrial and embedded systems.

As demand for SSDs in notebooks and mobile devices grew, in 2009, the mSATA format was introduced as a small form factor for storage, utilizing the same physical form factor and connector as mPCIe with a miniaturized SATA interface. While physically similar to mPCIe in both form factor and connector, mSATA cards are electrically different from mPCIe and require mSATA host support to function. Being based on the tried and true SATA storage protocol, mSATA made it easy for manufacturers to implement small form factor storage and it was rapidly adopted in the client space. These same factors have made mSATA attractive for embedded system storage and today it is one of the most popular small form factor SSD formats in both consumer and industrial markets.

mSATA bottlenecks

As the client and enterprise markets pursue higher capacity SSDs and higher throughputs to match, the performance bottleneck for top-end SSDs has become the SATA protocol which is limited to 600 MpBps. With increased capacities on SSDs, speeds go up as well and even the 600 MBps offered by SATA III is not enough for high-performance applications. At the same time, the mPCIe form factor on which mSATA was based physically limited how much flash could be put on one mSATA card.

Developed by the PCI-SIG consortium in response to SSD’s increasing demands on data throughput, M.2, formerly known as Next Generation Form Factor (NGFF) is a new specification for expansion modules in systems with space limitations.
The potential of M.2

Driven by client SSD performance needs, M.2 was developed as a forward-looking small form factor to resolve the issues mSATA was running into with flash storage in mind. With a thinner z-height and smaller footprint with less wasted board area, M.2 is more space efficient than mSATA. M.2 modules can be a range of lengths from 42 mm up to 110 mm and in either single- or double-sided versions. The flexibility of this physical specification allows for space-efficient M.2 add-on cards and M.2 SSDs with higher NAND capacities than mSATA would allow.

To address the bandwidth needs of performance SSDs, multi-lane PCIe was chosen as a high-end storage connectivity option. SATA III is currently limited to 600 MBps speeds and a single lane while PCI Express scales up to four lanes with M.2. At current PCI Express 2.0 speeds of 500 MBps a lane that means 2 GBps speeds are potentially possible with four-lane M.2 SSDs or even more with the new PCI Express 3.0. At the same time, M.2 still supports SATA as well as USB. This backward compatibility with existing signals eases migration to M.2 as it simplifies implementation of first-generation M.2 SSDs (running SATA) and peripheral cards such as Wi-Fi, GPS, and WWAN.

The physical interface

The M.2 specification defines three sockets for expansion modules. Socket 1 is for Wi-Fi, Socket 2 is for SATA or PCIe x2 SSD as well as general expansion cards, and Socket 3 is for SATA or high-speed PCIe x4 SSDs. The female socket connectors physically limit which M.2 cards can be installed. The M.2 cards themselves have connectors notched or “keyed” to their respective functionality (Figure 2, page 30). PCIe x2 SSDs can be keyed to fit both Socket 2 and Socket 3 connectors but will run at PCIe x2 speeds.

The host controller interface

To take full advantage of M.2’s multi-lane PCIe speed rather than running SATA over an M.2 physical interface, a new storage interface protocol is needed. As an industry standard, Advanced Host Controller Interface (AHCI) enjoys wide support at the operating system and controller level but is tied to SATA and its performance limitations. To get around this, client and enterprise SSD manufacturers so far have created custom drivers to unlock the bandwidth potential of multi-lane PCIe, but for the industrial market this is unfeasible from a cost and compatibility standpoint.

With the aim of allowing high-speed access to solid-state storage with PCIe over a standard protocol, a working group of more than 80 companies has developed NVM Express (NVMe). Whereas AHCI was designed in the era of rotating media and associated high latencies, NVMe has been optimized for the random access nature of SSDs and today’s multicore processors. A streamlined storage stack allows for higher throughput, lower latencies, better Input/Output Operations Per Second (IOPS), and lower power consumption as better performance allows the storage device to spend more time at idle.

NVMe’s benefits, open specification, and industry support indicate it will likely...
become the client storage protocol of the future, but adoption is taking time even in the client space. As a completely new storage protocol, NVMe is not compatible with AHCI and requires support at the system and software levels. As a standard for efficient access to SSDs, NVMe allows for non-proprietary solid-state storage that runs at native PCIe speeds, but until that sea change happens SATA/AHCI will continue to offer the optimal combination of reliability, performance, and compatibility for embedded applications.

**M.2 in the embedded space**

M.2’s strength as a small form factor lies not just in its potential for the next generation of high-performance SSDs, but also in its backward compatibility. While supporting high-performance SSDs over multi-lane PCIe, M.2 also supports SATA, USB, and single-lane PCIe. As NVMe awaits adoption in the marketplace, SATA-based first-generation M.2 storage cards and M.2 peripheral cards can allow space-constrained systems to benefit from the smaller and more flexible form factor with the reliability and compatibility of SATA.

For general embedded applications, mSATA and mPCIe are not going anywhere soon. Industrial applications have modest performance needs, emphasizing reliability and consistency instead. Even for performance-driven systems, the near-term value proposition is tenuous as the full performance benefits of M.2 SSDs require either NVMe support or proprietary drivers to realize native PCIe speeds. It will take time for the storage environment to support NVMe before embedded applications will be able to enjoy this level of performance, so current-generation M.2 SSDs may be a hard sell over mSATA modules in the embedded space. Meanwhile, mPCIe currently offers more than enough bandwidth for general embedded peripherals such as graphics cards or Wi-Fi modules.

**The embedded future of M.2**

The immediate benefits of M.2 in terms of size and capacity and the potential benefits in power consumption and performance with NVMe mean embedded OEMs and system designers need to be aware of this emerging format, but until the M.2 ecosystem matures, its current impact on the embedded and industrial market will be limited to the most space-constrained applications. Following more widespread adoption of the M.2 physical interface and NVMe host controller interface support, M.2 will affect performance-sensitive embedded applications next, but the reliability and robustness requirements of most industrial embedded systems mean mSATA/mPCIe will remain the small form factor of choice in the majority of industrial solutions for years to come.

C.C. Wu is Vice President of Innodisk and Director of Innodisk’s Embedded Flash Division.

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This Innodisk M.2 expansion module is keyed for Socket 2 and expands SATA connectivity with Hardware RAID.

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Controlling touch for high-performance devices, wearables

The Cypress TrueTouch capacitive touchscreen controller family offers single-touch, two-finger touch, and full multi-touch capabilities for screen sizes from 1.5" to 10.1". Cypress parts include a very high signal-to-noise ratio, waterproofing capabilities, fast refresh and scan rates, and low power consumption. The Cypress TrueTouch capacitive touchscreen controller was selected by Qualcomm for their Toq smartwatch product.

Prototype sensors for DIY and more

PIXELTEQ has announced a multispectral sensor development board for OEM optimal sensor prototyping. The board showcases the PixelSensor wavelength-selective photodiode arrays that help implement precision multispectral measurement in smaller devices. The board is targeted for a wide range of biomedical, industrial, and scientific applications. It even includes a tie-in to DIY apps – designers can program application-specific functions using the Arduino Integrated Development Environment (IDE). The kit also contains a cross-platform Graphical User Interface (GUI) to configure measurement settings of each spectral band, trigger external functions, communicate with other devices, and display/log data.

Lightweight, versatile Internet of Things/mobile database

The ITTIA DB SQL product is a lightweight embedded database targeting embedded systems, mobile devices, and other Internet of Things (IoT) appliances that require non-stop access to data. Weighing as little as 150 KB, the embedded database is expandable with enterprise features such as C/C++, TCP/IP, Open Database Connectivity (ODBC), Java Database Connectivity (JDBC), ADO.NET, Advanced Encryption Standard (AES), and more. The database also runs on a number of popular embedded processor architectures and operating systems, as well as custom platforms.
Take A Look At The x86 DIY Gizmo Development Board’s First Year

By GizmoSphere

It’s been described as hugely powerful. Extremely flexible. Blindingly fast.

It is the first x86 development board to be fully open source, end-to-end: hardware, software, and even bootloader.

Its compatibility with Windows 8 and previous versions of the OS, including Windows 7 and XP, makes Gizmo a practical PC replacement.

Since its official introduction to the world last year at a technical conference in Santa Clara, California, the x86 DIY Gizmo development board has caught the attention of developers globally.

From humble beginnings GizmoSphere has grown to include five key partners – AMD Embedded, Sage Electronic Engineering, Timesys, TMT, and Viosoft – and a dedicated community of developers via our website, Facebook page, Twitter account, and YouTube Channel.

Our support page boasts fully open-source design files and key downloads, including the board support packages SageBIOS™ BSP and Timesys BSP for Gizmo.

Our distributor, SemiconductorStore.com, notes a steady upward trend in sales of the Gizmo Explorer Kit as word about this versatile development board powered by the AMD Embedded G-Series APU continues to spread.

We’ve certainly expanded into many areas, and we’re poised for further growth through the rest of 2014.

What’s more, we’ve seen members of the growing GizmoSphere community, including university students, launch a number of exciting projects. Here’s a sampling of what developers are creating with their Gizmo boards:

> Fewer Potholes, Safer Roads: A team of students at Boston University selected Gizmo for their senior project: a vehicle mounted pothole detection system they’re creating to provide an automated, economical road repair solution. Their AutoScan prototype incorporates the Gizmo development board paired with an infrared depth sensing camera. AutoScan can be mounted under city vehicles to detect potholes automatically and access scheduling software for timely repairs.

> Go, Go Robot: An engineering student at Tecnico Lisboa in Portugal uses the Gizmo board to control a robot he built. With Gizmo and a keyboard, he controls the robot’s direction and speed.

> Secure, Self-Managed Cloud Infrastructure: An entrepreneur has developed a new database appliance, creating the means for a scalable, self-managed cloud infrastructure that can be accessed securely from any device, including mobile devices. The database appliance incorporates 8 Gizmo boards working as micro-servers operating in parallel. This multi-Gizmo system appears on the network as a single logical database server.

GizmoSphere is tearing down barriers in x86 open source computing by breaking new ground in the do-it-yourself market … and beyond. With attractive features and valuable downloads, GizmoSphere is steadily gaining a dedicated following.

Where will your bold initiative lead you? Share your progress with us at GizmoSphere.org. We’d love to showcase your project for the entire community to see.

Join GizmoSphere today and start building your dream project with the x86 Gizmo Explorer Kit!

www.gizmosphere.org

www.embedded-computing.com
By Google

Google Self-driving Car on City Streets

Self-driving cars take a lot of software, sensors, and other systems to be able to function autonomously. Google has been testing their self-driving car on the streets of Mountain View, CA and demonstrates its object, pedestrian, and cyclist sensing and avoidance capabilities.

http://opsy.st/ECDMay14GoogleVideo

By Morgan Advanced Materials

Heat Flow: A New Web-based Heat Transfer Calculator

A tool was recently launched that allows users to simulate heat transfer scenarios. Users can create and manage material databases and calculate based on international standard ASTM C680 formulas for heat loss and surface temperature estimates. The tool is available for most browsers and operating systems in addition to iTunes and Google Play for smartphones and tablets.


By Dave Hunt

PiPhone – A Raspberry Pi-based Smartphone

The iPhone 6 will probably be out later this year, but what about a Raspberry PiPhone? It’s touchscreen, a Sim900 GSM/GPRS module to make calls, and a LiPo battery to make it wireless… it may not be your main smartphone anytime soon, but it’s a pretty neat project. Creator Dave Hunt’s write up on the PiPhone:

http://opsy.st/ECDMay14PiPhone
http://opsy.st/ECDMay14PiPhoneVideo

By David Finch, Newark element14

LED There be Light: A Quick Overview of Switch-Mode Power Supply Design Options

Lifetime, form factor, packaging, a range of colors – from the outside it would appear as though LED lighting has everything going for it. But for design engineers, as usual, there’s a lot more to the story. Driving multiple high-power LEDs in switch mode is no trivial task for a non-experienced power supply engineer, but there are several options available to get the job done.


By John Hoeschele, Anaren


With the growth in wirelessly linked sensors that are linked to our smartphones and tablets, consumers and businesses alike will soon get a wide variety of notices delivered directly to their “inbox.” Bluetooth connectivity will help our mobile devices become passive receivers of all sorts of sensor data.

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