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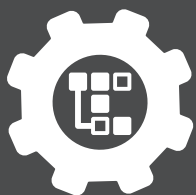
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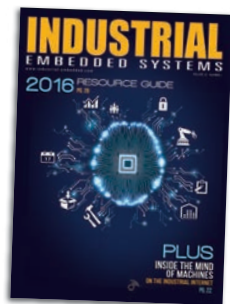
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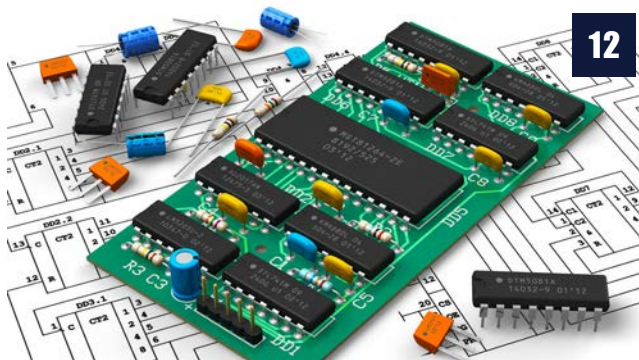


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By Brandon Lewis, Technology Editor



Predixions and precision for the Industrial Internet

The Internet of Things, Industrial Internet, or Industry 4.0 – call it what you will, but all of these terms can be summed up simply as “The use of networked technology to increase profits in a data-driven economy.” While it’s clear that the IoT of Fitbits and Nest thermostats doesn’t translate completely into that of wind turbines and jet engines, the concept of capturing information to influence future business outcomes remains constant.

Last year at the IoT Solutions World Congress in Barcelona, Colin Parris, Vice President of GE Software Research keynoted on the above notion, citing Apple, Amazon, and Google as examples of how data can be transformed over time to move from demographic data to psychographic data (or profiles of individual consumers) in order to drive sales. Then Parris turned his attention to applying these models in the context of the larger industrial market, doing so by introducing what the company calls “Digital Twins.”

Joining the cyber and physical in IIoT

Digital twins are a manifestation of the cyber-physical world of IIoT that create a virtual representation of individual physical systems deployed in the field. These engineering models are designed collaboratively by software architects, materials scientists, and hardware designers to create precise digital replicas of individual, real-world assets. These replicas are then continuously tuned and updated based on the history of and events experienced by a particular system, which is paired with its twin by serial number.

For instance, the digital twin of a wind turbine would account not only for the system’s total hours of operation, operating conditions, and limitations of the various components that make up the actual machine, but also use that information to project into the future for system optimization. If there are adverse weather conditions on the horizon, the digital twin can be used to simulate how the turbine’s gear box, controller, generator, and yaw drive must be set to maximize energy production without risking damage to system components at certain wind speeds. Digital twin models can also be used to deliver meticulous data about exactly what components require inspection, and when specifically. The ability to pinpoint the service of a jet engine, locomotive, or any industrial system where downtime equals lost revenue, in turn also means maximized revenue. This goes beyond the realm of predictive maintenance and into precision maintenance.

All of the data regarding repairs, environmental conditions, lifetime performance, etc. is repeatedly realized in updated

iterations of the digital twin, much like your personal profile on iTunes or Amazon continuously evolves over time. However, these capabilities are not the most intriguing possibilities enabled by a digital twin.

Analytics at the next level

Consider the IIoT at its most valuable, where, as Parris puts it, networked industrial machines publish content that is of interest to other networked industrial machines. Going back to the wind turbine example, a newer turbine in a wind farm may detect anomalies that it has never experienced before or is unfamiliar with. These could be related to performance, environmental conditions, or perhaps even a potential security vulnerability that the new machine is ill-equipped to handle. In this scenario, the new turbine would be able to query other nearby turbines for information about a particular anomaly – their historical analytics, as well as system updates – and adjust its settings and behavior accordingly. However, because the new turbine is unique from the other turbines it has requested data from – operating with its own components at various stages of their lifecycle, perhaps in a different orientation, and so on – its digital twin would use artificial intelligence and machine learning algorithms to compensate for status discrepancies included in the recommendations acquired from the new turbine’s counterparts.

This offers the possibility for two services on the Industrial Internet. First, historical data from industrial devices can be published for use by other systems, perhaps even ones in different market domains that serve different end purposes. Second, because of the possibility that relevant data could be of use to dissimilar systems, there will be a need to translate that data into various appropriate formats.

The platform that enables this data exchange marketplace is GE Predix, a cloud platform-as-a-service (PaaS) software offering that is not unlike the app stores for mobile devices that we’ve grown so accustomed to. Here, a collection of analytics and runtimes are available from GE and other third-parties with systems deployed across a variety of industrial markets, and exposed to the community through a set of APIs. Paired with an industrial-grade operating system, Predix is a prosumer tool for the Internet of Things, something GE is all too familiar with.

This is what the data-driven economy looks like on the Industrial Internet. For more information on Predix, or to register for a free trial, visit www.predix.io. **IES**



Maximizing investment in your legacy hardware platform

Even if you aren't planning to develop a brand new product, there are a number of options to help you make the most of your investment in your current embedded product line. Legacy products based on older hardware platforms can become obsolete or use end-of-life components. Customers are also continually looking for new features and better performance, but often don't want to invest in new hardware.

These are ongoing challenges for any product manufacturer, but are particularly highlighted in embedded systems where product lifetimes are typically much longer than in consumer markets.

The following looks at three of the most popular options to help you address these issues.

1. Firmware optimization

Optimizing your existing firmware can provide better performance and new features while still retaining the investment in your current hardware platform. This will not only remove (or at least delay) the need for a new hardware design, but also provides an opportunity to add new features, fix existing issues, and enhance reliability.

Sometimes it can be as simple as using more modern development tools with improved binary code generation, but optimizing embedded firmware is often a task where using a fresh pair of eyes can yield benefits, particularly if the engineers concerned have experience with this type of work and know the sort of pitfalls to watch out for. A company's own engineers are sometimes too close to the current design to be able to take an objective view of what is required to make the system run better, and using a third party can frequently be the best way to improve performance and reliability.

2. Firmware refactoring

Firmware refactoring is often overlooked as a means of improving the maintainability of legacy code, but an effective refactoring exercise can greatly improve the quality of older code and reduce the time to add new features. It can also help reduce the maintenance burden on the original code authors who are often now more senior and would be better employed on new design work.

Many successful products are based on a legacy codebase, and the longer they run and the more successful they are, the less engineers want to carry out a major redesign on them. This

leads to the firmware being a mixture of old and new code, often with different coding styles and varying levels of comments and documentation.

Adding new features, particularly non-trivial ones, can result in a lot of time being spent reviewing the current code and understanding what it does, and ultimately means that adding new feature is a complex and painful business.

Carrying out a detailed refactoring exercise can help unify the legacy codebase and make it more maintainable. A fresh pair of eyes can often identify bugs or weaknesses in the code and address them before they reach the customer.

Finally, it is important to ensure that the refactored code still does exactly what it is supposed to do, so a suite of regression tests that can be run before and after is also essential. The end result is then a codebase that is once again fit for purpose and can be used as the basis for future development for years to come.

3. Firmware migration

Sometimes the previous options are simply not sufficient, and you have to look at moving to a new hardware platform to get higher performance, lower cost, and lower power. Although this inevitably requires investment in a new hardware design, the results can be significant and very cost effective.

A typical firmware migration project not only requires an understanding of the product requirements, but also experience of the new hardware and firmware environments. The old and new firmware may run on different operating systems and/or types of processors, and using experienced engineers to carry out this porting work can help dramatically reduce the risks and amount of work required.

The migration may also be combined with a refactoring exercise as described previously so that a lot of the previous investment in developing the legacy system can be retained, but re-written so that the end result is much more efficient and offers higher performance while still being maintainable. **IES**

Ian Smith is Managing Director of Abelon Systems.

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'C' lands on FPGAs to make embedded multicore computing a reality

By Rory Dear, Technical Contributor

Through intense innovation and development, the primary face of embedded computing has changed constantly throughout the decades, but it's only relatively recently that parallel processing by means of multiple processor cores has even been possible. Some have argued that the single-purpose nature of embedded computers rendered multicore processing unattractive, and it's true that even today there exists a multitude of legacy applications where single-core performance remains king – a result of developers not designing for multicore. Given the predominantly asymmetric nature of processing tasks within an embedded system, multicore processing permits lower clock rates and consequently an overall reduction in power consumption – a factor more critical in embedded than ever before.

Those in the technology world have a natural desire to avoid duplication of effort and reinventing the wheel whenever possible. To this end, even form factors that have existed for decades, such as the ubiquitous PC/104, remain strong, as legacy users always seek an upgrade path that provides the least effort. The changes in availability of electronic components aren't generally controllable by the system integrator, but the mechanics of a solution are. The industry's continuation of one of the original embedded form factors offers innumerable legacy PC/104 projects an easy upgrade path, but there's a problem.

The peripheral bus of the original PC/104 is ISA. PCI was later drafted into the PC/104 family to offer a higher speed bus – PCI/104 – as well as PC/104-Plus, which provides both PCI and ISA. Embedded developers still use PCI to integrate (what today we'd think of as) low-bandwidth peripheral functions, but if PC/104 is to survive as a form factor,

an even higher-speed peripheral bus needs to become available and, perhaps even more importantly, standardized.

A potential standard solution has emerged as part of a \$100 million industry-wide EU research and development project into "embedded multicore systems for mixed criticality," namely, EMC². The objective of the EMC² (embedded multicore systems for mixed-criticality applications in dynamic and changeable real-time environments) concept was to kill two birds with one stone. Introducing the high-speed PCI Express (PCIe) expansion bus has permitted integration with the latest bandwidth-hungry peripheral functionality, such as video streams, while retaining the PC/104 form factor and facilitating multiple cores and processors. This opens the door to revitalizing creaking legacy applications or developing entirely new ones. The stack-through PCIe interface also allows multiple processor modules to be stacked, in itself multiplying the available cores and/or processors and saving cost and space compared to the customary backplane solution.

"Introducing the high-speed PCI Express expansion bus has permitted integration with the latest bandwidth-hungry peripheral functionality, such as video streams, while retaining the PC/104 form factor and facilitating multiple cores and processors. This opens the door to revitalizing creaking legacy applications or developing entirely new ones."

Programming for mixed criticality, power, and performance across multiple cores

One of the biggest challenges is to attain reliability across multiple independent processing cores to achieve safety-critical status. Embedded solutions are relied upon more than ever to undertake such tasks, and the requirements of proving that safety criticality are more stringent than ever before.

Analogous to the benefits of splitting asynchronous processing tasks over multiple cores, the trend to siphon specific processing threads into disparate hardware elements designed to execute tasks, such as FPGAs, is prevalent today. With the explosion in their popularity, ever-increasing complexity, and an entirely new language to code them with, a skills and resource vacuum has quickly ensued.

In combination with expensive tools, availability and restrictive costs involved with expert VHDL programmers have held back the universal deployment of FPGAs. Many system developers are still shying away from the technology and undertaking invariably heavy mathematical and algorithm-based processing in a generic processor instead, at the expense of power consumption and heat dissipation requirements, amongst others. The other hurdle is few offer a commercially viable route to integrate FPGA fabric into an off-the-shelf system. PC/104 was one of the few, as it provided an optimum commercial platform since designing a new PCB to include the FPGA circuitry simply wasn't viable.

Xilinx seized the opportunity by commercializing an All-Programmable system-on-chip (SoC) solution, the Zynq SoC with SDSoc development environment (Figure 1).

The Zynq SoC combines the software programmability of an ARM processor with the hardware programmability of an FPGA. The ARM processor satisfies more traditional processing threads while the FPGA manages those heavily mathematical functions expediently and with minimal power consumption.

While the concept was first conceived by Dr. Ian Page of Oxford University more than 20 years ago, the SDSoC development tools allow FPGA fabric programming in more traditional C/C++, allowing the power of FPGAs to be leveraged by a far wider audience than ever before. This quiet revolution effectively allows any developer, down to those even just starting their coding journeys, to leverage the massive potential of FPGAs.

Page, FIEE, CEng of Oxford University, remarks, "The core of my hardware compilation or computing without computers approach was actually developed starting in 1990, although it was only in the mid '90s that it was given a C-like syntax as Handel-C. Prior to that, Handel was cast in an abstract syntax form. This was very deliberate so that the programmer or meta-programmer could write proofs and transformations of the Handel programs. This allowed things like the automatic generation of heterogeneous parallel implementations, which were provably correct with respect to the original software.

"Although it is not the most parallel example, one particular transformation was the processor introduction transformation," Page continues. "This took in the software program you were interested in, created a processor design specifically to support that program, then compiled the program – partially or completely – onto the processor, and then implemented the whole thing in an FPGA. It was a bit like asking ARM to create an application-specific variant of one of their processors just for you, and then getting it back from them five minutes later."

With few exceptions, an embedded system has requirements for I/O. If these requirements are merely slow speed, then USB could suffice. However, with

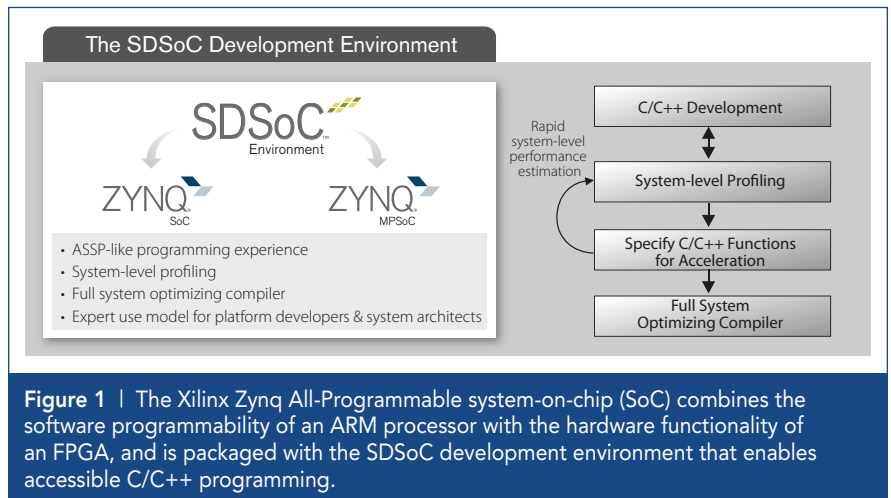


Figure 1 | The Xilinx Zynq All-Programmable system-on-chip (SoC) combines the software programmability of an ARM processor with the hardware functionality of an FPGA, and is packaged with the SDSoC development environment that enables accessible C/C++ programming.



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today's applications demanding integration of high-speed cameras or a high-speed ADC/DAC, an FPGA is required. The Zynq offers the ARM processor for USB and the FPGA to satisfy the high-speed needs. The SDSoC development environment enables analytics to determine by which processing element each function is most prudently executed to achieve optimal performance and power consumption.

Mark Jensen, director of corporate software strategy at Xilinx asserts, "The SDSoC development environment provides a familiar embedded C/C++ application development experience including an easy-to-use Eclipse IDE and a comprehensive design environment for heterogeneous Zynq All Programmable SoC and MPSoC deployment. Complete with the industry's first C/C++ full-system optimizing compiler, SDSoC delivers system-level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming. It also enables end-user and third-party platform developers to rapidly define, integrate, and verify system-level solutions and enable their end customers with a customized programming environment."

Production-ready implementation on PC/104

So how can this progress be translated into a commercially viable embedded solution for customers? One that offers these advantages, but without becoming so specific that few applications end up falling within its scope? Progress has been steady for years, and integrating FPGA fabric into embedded was a critical step.[1] The answer lies in combining the single-board PC/104 with the performance scalability of the system-on-module (SOM) design methodology to gain the advantages of both off-the-shelf SBCs and custom boards. Enter the EMC2 range from Sundance Multiprocessor Technology.

The EMC2 range offers a PC/104 format carrier board with integrated PCIe expansion and SOM interface that provides the flexibility and scalability

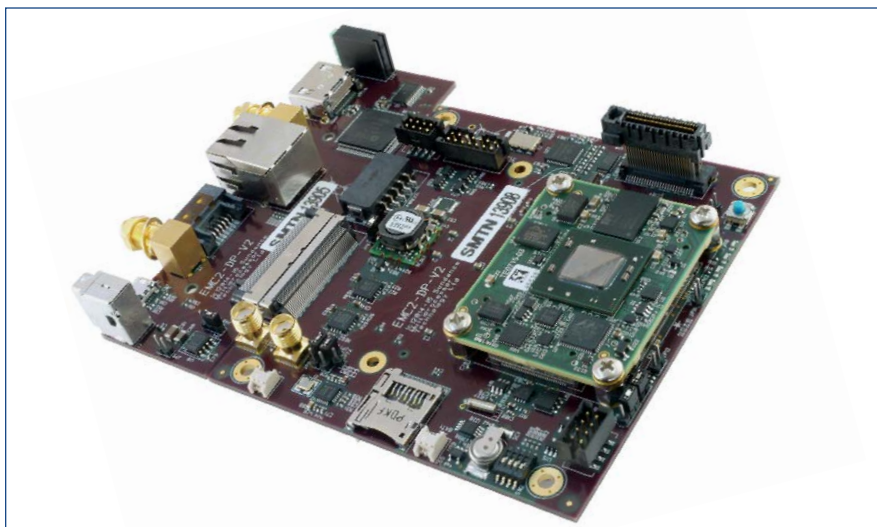


Figure 2 | The EMC2-Z7030 from Sundance Multiprocessor Technology is a PC/104 compatible system on module (SOM) that includes a Xilinx Zynq system-on-chip (SoC) with integrated dual ARM Cortex-A9 cores and a Kintex-7 FPGA.

necessary to encompass a plethora of potential embedded applications. The latest offering, the EMC2-Z7030, features the Xilinx Zynq SoC with integrated dual-core ARM Cortex-A9 processor combined with Kintex-7 FPGA technology (Figure 2). This combination offers an exponential performance increase, up to a factor of 100, over a typical FPGA SoC, whereas the power consumption remains the same. For example, on-the-fly video processing can be achieved by migrating a C program on the ARM processor to FPGA fabric.[2]

Flemming Christensen, managing director of Sundance Multiprocessor Technology Ltd., states, "The combination of Sundance's EMC2 boards and the Xilinx SDSoC development environment is another significant step forward for embedded systems design, enabling systems engineers to take advantage of the Zynq SoC's combination of a popular ARM Cortex-A9 CPU and the flexible and fast I/O associated with FPGA technology."

The EMC2-Z7030 is highly flexible in that it allows the core processor and FPGA combination to be leveraged as a stand-alone system, yet can also be utilized as a peripheral card where an x86 CPU module can be employed to vastly extend general-purpose processing capability.

Continually seeking commercial viability

Achieving commercially viable platforms around FPGAs invariably involves squeezing into the smallest FPGA fabric one possibly can. With the flexibility of the EMC2-Z7030, designers can develop and optimize their platform on a large and fast Zynq SoC to expedite development time, then scale down for production – or even maintain a scalable product range in the production phase if sub-models of their solution with varying complexity levels are required. The concept is far from new, but the newfound affordability drives this technology from niche into mainstream embedded computing. All that's needed to truly stake FPGA's claim over traditional single-core embedded solutions is FPGA SoCs that cost \$10, rather than \$100. **IES**

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Industrial Embedded Technology for Our Interconnected World

How to preserve signal-chain integrity when interfacing microcontrollers with DACs

By Rahul Prakash and Kunal Gandhi

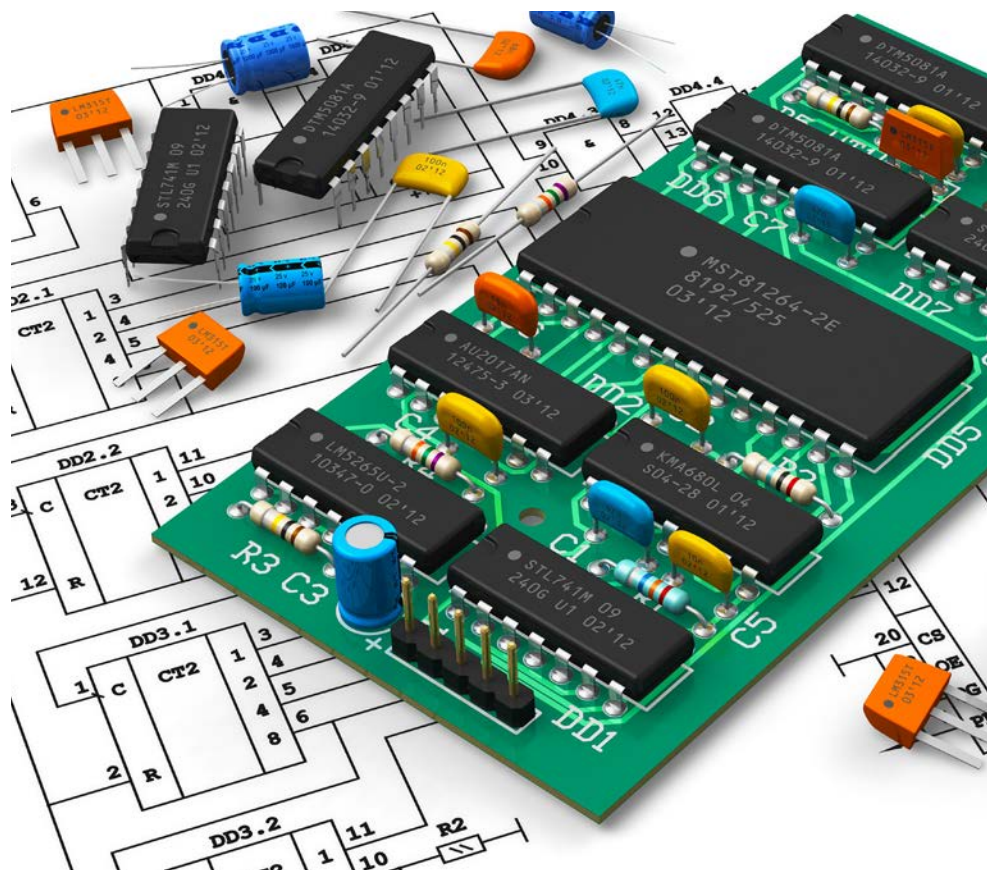
A microcontroller is one of the most power-hungry components in an industrial system. As the Industry 4.0 standard becomes more popular, microcontrollers are taking on more and more of a computing burden. As a consequence, we are seeing an explosive increase in microcontroller power consumption.

One way to manage power is to reduce the supply voltage. A decade ago, industrial control systems used 5 V microcontrollers. Now, with more processing capability inside the microcontroller, 3.3 V microcontrollers are gaining in popularity because this increased processing power coupled with lower supply voltage can lead to increased power savings.

On a high level, this shift in power supply seems like an easy solution to the power dissipation problem. However, microcontrollers are tightly coupled with all of the other components that they control. System architects have to ensure that all components are compatible with the logic-level interfacing requirement while not compromising the integrity of the signal chain's precision. In addition to this requirement, the system must be power efficient. The following discussion will highlight some of the challenges of interfacing microcontrollers with precision digital-to-analog converters (DACs) and how to address them.

Theory

There are multiple power-supply domains for typical non-isolated industrial systems (Figure 1). The microcontroller is powered by a high-capacity power supply capable of delivering hundreds of milliamperes of current.



Precision components such as DACs require a clean power supply that need not provide high current.

The requirement of the application mandates the DAC's power supply voltage level. For example, many precision applications require a 5 V output voltage range. This means that the power supply must be adequate to support this output range. Thus, in Figure 1, VDD-DAC must be > 5 V. For the lowest power dissipation, the lowest power supply must supply the microcontroller. Most common microcontrollers can operate with a 3 V power supply. Hence, VDDM can be as low as 3 V.

This power supply requirement places an unusual constraint on DACs. The DAC must be able to accept the input digital signal that toggles between 0 V and 3 V while itself being powered by a 5 V supply. Every precision DAC has a specification that relates to this condition, typically listed under the logic inputs section of the characteristics table (Figure 2).

The specification of importance in this case is V_{INH} (input high voltage). According to the data sheet, the DAC7311 is specified to accept input digital signals from $0.7 \times AVDD$ to $AVDD$ for $2.7 \text{ V} \leq AVDD \leq 5.5 \text{ V}$. Using the power supply requirement from Figure 1, the input digital signal must be $\geq 3.5 \text{ V}$ (0.7×5) to use this DAC. This places a lower limit on the microcontroller power supply: 3.5 V. But to reduce the power dissipation in the microcontroller, it is imperative to use the lowest possible power

“A decade ago, industrial control systems used 5 V microcontrollers. Now, with more processing capability inside the microcontroller, 3.3 V microcontrollers are gaining in popularity because this increased processing power coupled with lower supply voltage can lead to increased power savings.”

supply – for example, 3 V. This discrepancy is a common problem for system architects.

Solutions

There are three solutions to this problem.

Use a level shifter

A level shifter converts digital signals from one logic level to another. Using a level shifter between the microcontroller and the DAC (Figure 3) is the simplest workaround. But because each digital input signal needs a dedicated level shifter, this solution increases total board size and cost, particularly for DACs with multiple digital input pins like the DAC8568. The level shifter must be functional at the required communication speed between the microcontroller and the DAC.

Choose a DAC with an integrated level shifter

Some DACs have the level shifter integrated, with a separate power supply pin called the IOVDD (Figure 4). The package size of the DAC increases slightly with the additional pin, thereby increasing the board area. This solution also requires isolating the IOVDD power supply for power-isolated systems, including additional power isolators.

Choose a DAC with a transistor-transistor logic (TTL)-enabled interface

Some DACs have an interface that accepts lower levels of V_{INH} . For example,

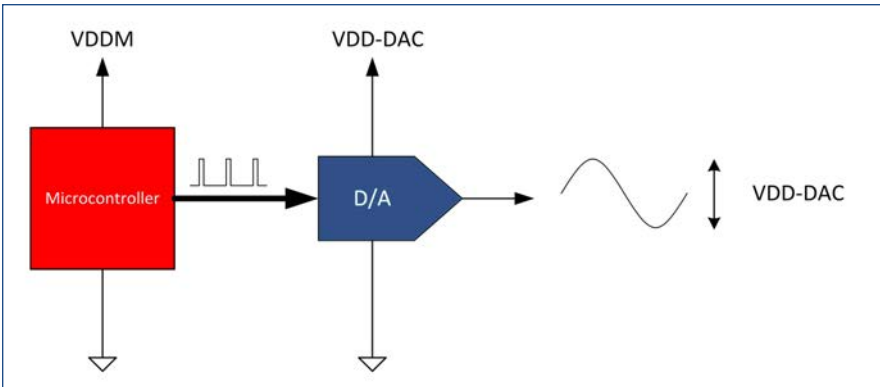


Figure 1 | Example of a non-isolated system

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS ⁽⁶⁾					
Input current				±1	μA
V_{INL} , Input low voltage	$AV_{DD} = 2.7\text{ V to }5.5\text{ V}$			$0.3 \times AV_{DD}$	V
	$AV_{DD} = 2.0\text{ V to }2.7\text{ V}$			$0.1 \times AV_{DD}$	V
V_{INH} , Input high voltage	$AV_{DD} = 2.7\text{ V to }5.5\text{ V}$	$0.7 \times AV_{DD}$			V
	$AV_{DD} = 2.0\text{ V to }2.7\text{ V}$	$0.9 \times AV_{DD}$			V

Figure 2 | Logic input levels of a single-channel, low-power DAC.

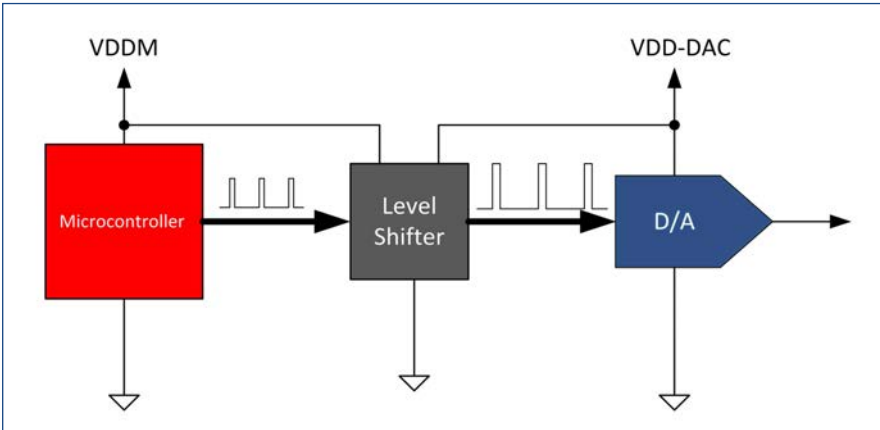


Figure 3 | Using a level shifter to interface 5 V DAC with 3.3 V microcontroller.

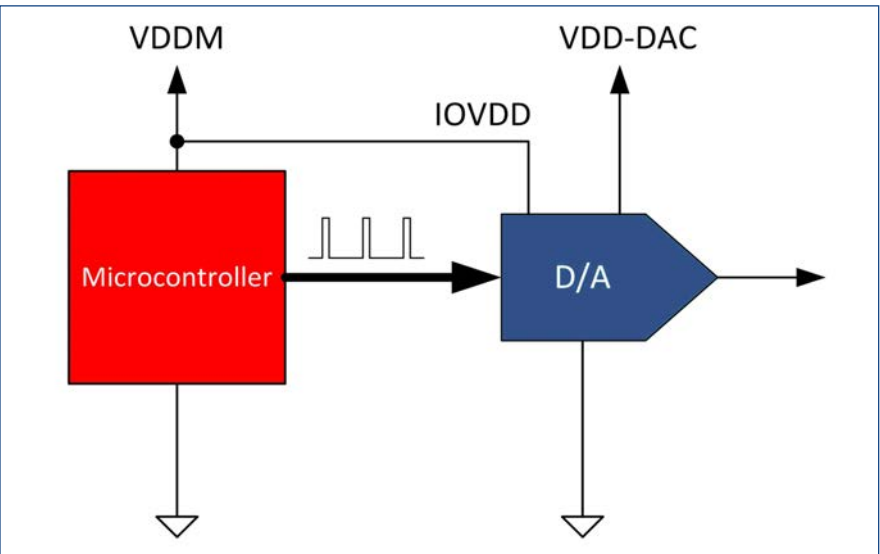


Figure 4 | DACs with an integrated level shifter.

the DAC8562T (Figure 5) data sheet specifies that it can accept input digital signals from 2.1 V to AVDD for 2.7 V ≤ AVDD ≤ 5.5 V. Thus, you can use this DAC in systems such as Figure 1 with VDDM = 3 V and VDD-DAC = 5 V.

Priorities

There are three key priorities while designing a system with a DAC that has a TTL-enabled interface.

Power dissipation

By using a TTL-enabled logic interface, the microcontroller can now run at the lower 3 V supply voltage. However, based on the idle voltage of the input digital signal to the DAC, there can be significant leakage current that flows through the power supply of the DAC. The typical value for this leakage current is usually specified in the power requirements section of the characteristics table (Figure 6).

The DAC power supply of 5 V coupled with the pin-idling voltage of 3 V causes a significant increase in the device's current consumption. The majority of the

leakage current flows through the I/O cells, as shown in Figure 7. This is evident from the table in Figure 5. In order to reduce this leakage current, we recommend keeping all digital input signals (except level-sensitive signals) idling at logic low or 0 V as opposed to logic high or 3 V.

DAC's DC accuracy

DC accuracy is a key point that is often overlooked while interfacing a microcontroller and a precision DAC with TTL logic. Figure 8 shows a simplified block diagram of a precision DAC. The parasitic resistor, RPAR, on the supply (VDD) and ground represents the pin and metal resistances inside the chip. In most precision DACs with a single supply and ground pin (for example, the DAC8560), the analog and I/O power supplies are shared internally.

Typically, the power supply lines inside the chip are directly connected to the supply pin; however, this is not always possible on very small packages. In those cases, the analog power supply is tapped from the closest point on the power supply rail. Thus, the analog power supply to the DAC output buffer incurs parasitic resistance to the supply pin.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS⁽²⁾					
Input-pin leakage current		-1	±0.1	1	μA
Logic input LOW voltage V _{IL}		0		0.8	V
Logic input HIGH voltage V _{IH}		2.1		AV _{DD}	V
Pin capacitance				3	pF

Figure 5 | Logic input levels of the dual-channel, low-power DAC.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS⁽⁵⁾					
Power supply current (I _{DD})	AV _{DD} = 3.6 V to 5.5 V, normal mode, internal reference off, Digital inputs at V _{DD} or GND		0.25	0.5	mA
	AV _{DD} = 3.6 V to 5.5 V, normal mode, internal reference off, Digital inputs at TTL level			4	
	AV _{DD} = 3.6 V to 5.5 V, normal mode, internal reference on, Digital inputs at VDD or GND		0.9	1.6	
	AV _{DD} = 3.6 V to 5.5 V, normal mode, internal reference on, Digital inputs at TTL level			5	
	AV _{DD} = 3.6 V to 5.5 V, power-down modes, Digital inputs at VDD or GND		0.55	4	μA
	AV _{DD} = 2.7 V to 3.6 V, normal mode, internal reference off, Digital inputs at VDD or GND		0.2	0.4	mA
	AV _{DD} = 2.7 V to 3.6 V, normal mode, internal reference off, Digital inputs at TTL level			.08	
	AV _{DD} = 2.7 V to 3.6 V, normal mode, internal reference on, Digital inputs at VDD or GND		0.73	1.4	
	AV _{DD} = 2.7 V to 3.6 V, normal mode, internal reference on, Digital inputs at TTL level			1.8	
	AV _{DD} = 2.7 V to 3.6 V, power-down modes, Digital inputs at VDD or GND		0.35	3	μA

Figure 6 | Power requirements of the dual-channel, low-power DAC.

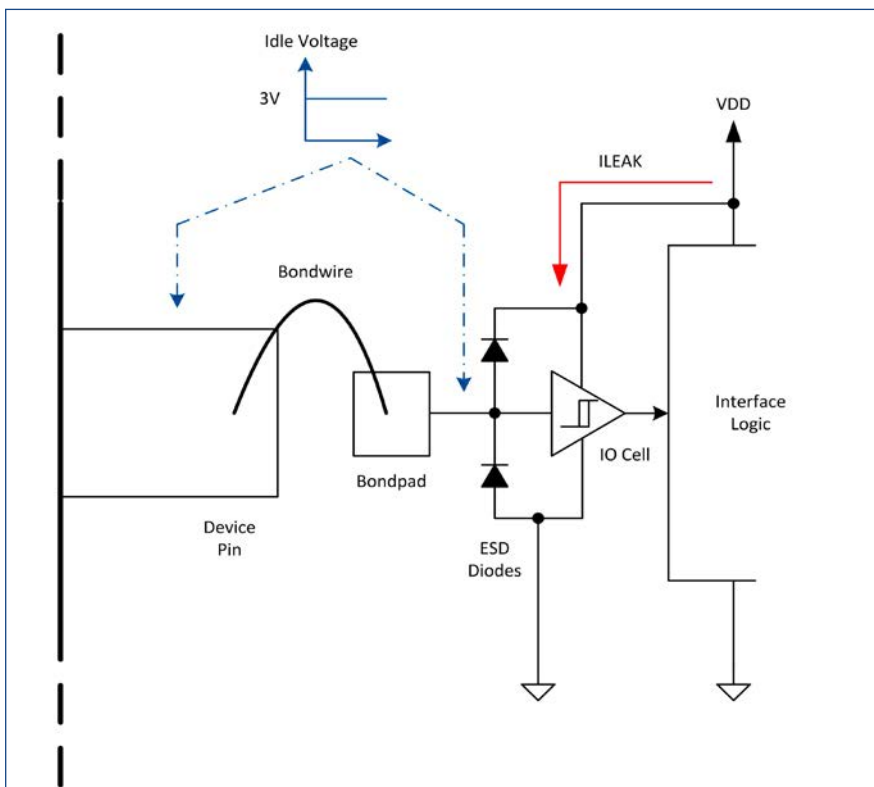


Figure 7 | Typical I/O cells.

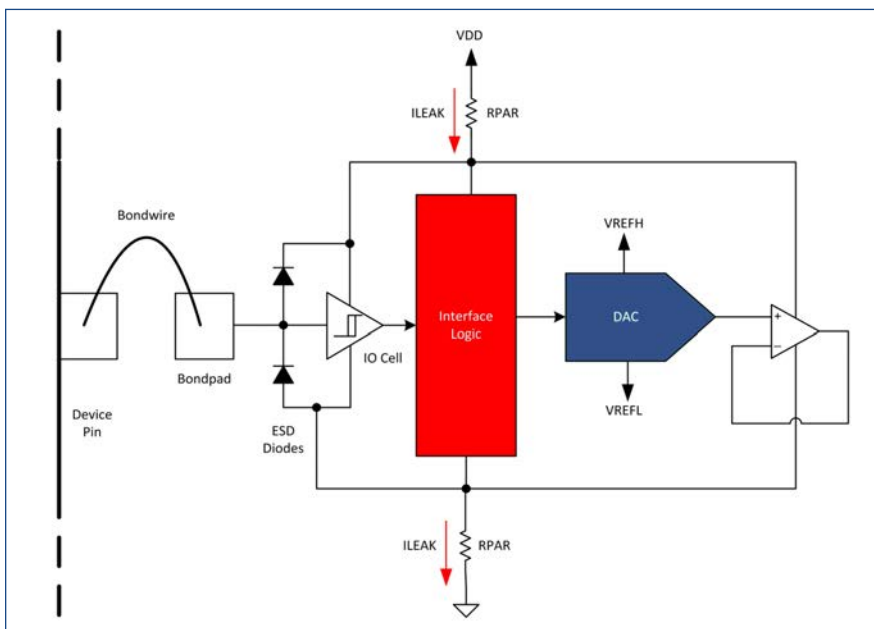


Figure 8 | Simplified DAC block diagram.

The leakage current discussed in section (a) causes IR drop across the parasitic resistance on the power and ground rails, reducing the headroom and foot room for the DAC output buffer and affecting DAC DC specifications such as offset and zero-code error. To reduce this impact, we recommend keeping all digital input signals (except level-sensitive signals) idling at logic low or 0 V, as opposed to logic high or 3 V.

Monotonicity and INL

For precision DACs, monotonicity and integral non-linearity (INL) are guaranteed for all of the codes. Following the example in Figure 8, the magnitude of ILEAK depends on the number of signals idling at logic high. The ILEAK is largest when all of the signals are idling at logic high. In between subsequent writes to the DAC, if the different

numbers of input signals are idling at logic high or low, the magnitude of ILEAK will vary from code to code.

This can cause changes in the headroom and foot room for the DAC output buffer and affect code-to-code linearity or even non-monotonic behavior of the DAC output in the worst case. We recommend keeping all digital inputs at the same I/O levels before and after writing to the DAC.

Conclusion

Preserving precision in a signal chain is often considered a part of signal-chain conditioning. However, interfacing the microcontroller and precision components in order to maintain precision in the signal chain also requires special care. This article discussed the issues associated with interfacing two different I/O levels between the microcontroller and precision DACs, along with some techniques to reduce the impact of interfacing to the precision signal chain.

For more information, download these datasheets: DAC7311, DAC8562T, DAC8560. **IES**

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Industrial motion control: Software creates better value and performance than hardware

By Dipesh Mukerji

Embedded OEMs – especially those whose products have complex human-machine interfaces (HMIs), manage many degrees of motion, and require hard real-time operation – have traditionally relied on field programmable gate arrays (FPGAs) and digital signal processors (DSPs) to meet the precision and performance requirements of machine vision and motion control applications. Today, that hardware-centric model is undergoing intense scrutiny as OEMs face increasing market pressures to cut costs, improve quality, and differentiate their products. By adopting a software-based control (soft-control) architecture, OEMs have an opportunity to do all three. They can differentiate their products and improve their competitiveness by significantly increasing yields/throughputs and shortening time-to-market. They can also reduce their bill-of-materials (BOM) costs and shrink compute footprints while simplifying and streamlining development, usability, and training.

In the relentlessly changing world of technology, several important advances are converging to prompt a rethink of traditional machine vision and motion control systems architectures. The major trends supporting this disruption include:

1. Increasingly powerful x86 processor technologies
2. Renewed commitment to commercial off-the-shelf (COTS) hardware and software
3. Advances in, and availability of, COTS-based fieldbuses
4. Convergence of components in system design
5. The advent of the Internet of Things (IoT) and Industry 4.0 touch-centered usability and motion sensing technologies

Although there are several competing approaches for capitalizing on these trends, a software-based control architecture has emerged as the leader.

By utilizing hard real-time symmetric multiprocessing (SMP) support available on today's x86-based multicore architectures and tight integration with the Microsoft Windows environment, OEMs can leverage versatile soft-control architectures to move control logic from specialized hardware components into software. For example, C/C++ source code logic that traditionally has been compiled and run on DSPs or FPGAs for programmable logic controllers (PLCs), motion control, and machine vision systems can be ported to target a real-time operating system (RTOS) or real-time extension to Microsoft Windows. The result is a hard real-time, SMP-enabled application that runs directly on x86, eliminating the need for an FPGA or DSP to perform the logic.

The following describes how the use of soft control architectures like control architectures based on multicore x86 hardware, such as the KINGSTAR Soft Motion Platform and IntervalZero RTX64 real-time extension for Windows, can help OEMs improve yields and throughput, shrink compute footprint, and significantly reduce costs for both themselves and their customers (Figure 1).

Soft-control architecture driving motion control and machine vision

Unlike traditional motion controllers that must incorporate a hardware microcomputer, FPGA, or DSP to provide features such as proportional-integral-derivative (PID) compensation, soft motion relies exclusively on a software-only engine that runs directly

on the cores of a host PC to handle real-time processing. This replaces the previous solution of running on a PCI board that plugs into a PC, which is expensive because it leaves the PC idle while the PCI board does the work.

A motion control software solution solves many of the challenges inherent in the traditional hardware approach, including vendor lock-in, flexibility, and cost. The best soft-control architectures have the ability to completely replace industrial motion control and machine vision hardware with a low-cost, Windows-based machine automation platform, as well as replace proprietary I/O and cabling with low-cost commodity parts like network interface cards (NICs) and CAT5 cables by taking advantage of standards like EtherCAT.

With a software-based motion control solution like the KINGSTAR Soft Motion Platform, EtherCAT can be used to transmit and receive data over a network, and a real-time extension like IntervalZero's RTX64 can turn Windows into a real-time control system. Using EtherCAT to transmit and receive all of the data over a network, as many axes can be controlled as needed and scaling up the axis count becomes very straightforward with the use of standard CAT5 cables, which are inexpensive and available in any length required. With EtherCAT, amplifiers can be mounted very close to the motors, and the digital nature of the signals eliminates analog cables entirely, as those outputs become part of an Ethernet packet. This allows the encoder, the halls, and the motor power cables to be as short as possible – a few feet long at most – which dramatically reduces costs. In addition, all of the cables, now much shorter, are identical. The cables simply connect a motor to an amplifier, which also greatly lowers cost and minimizes the chance of error. With this system in place, the control logic

software itself can be written. Run as an integrated platform, these components can accomplish everything that a DSP solution can provide and more.

Software versus hardware:

A performance comparison

Motion control software delivers equal or better performance than comparable hardware. Intel processors available today can do the exact same calculations as DSP chips and at the very same update rates, with motion profiles and PID calculations being just two examples. Furthermore, because the solution is software based it can be changed easily, so if a more complicated control scheme is needed for a particular axis, it can just be programmed in. One would just leave all of the standard axes to run as normal, but take over control of any axes that require more logic: Change servo gains on the fly; electronically gear any axis to any other. With software, you gain agility and save time.

With EtherCAT as many axes as needed can be added to a design, and single-core Intel processors have been used to control 100 axes with an update rate of 500 μ s, representing an order of magnitude improvement over DSP solutions. This ability is so powerful that in some cases motion control engineers have attempted to execute two control programs on a single-core Intel processor-based equipment as two separate machines after realizing it's possible to run multiple programs on a single EtherCAT network with one PC controlling each. If needed, however, a separate core can be dedicated for each program in more demanding applications.

Software versus hardware:

A cost comparison

As detailed in Figure 2, the cost of an 8-axis software-based motion control system is 44 percent of the cost of a similar DSP solution. If an additional axis needs to be added to the system, the cost of the DSP solution goes up by \$1,500 because an additional board must be added to the PC; with a soft motion solution, additional axes can be included at no additional cost.

Businesses succeed when they produce quality products at lower cost and faster time-to-market than their competitors.

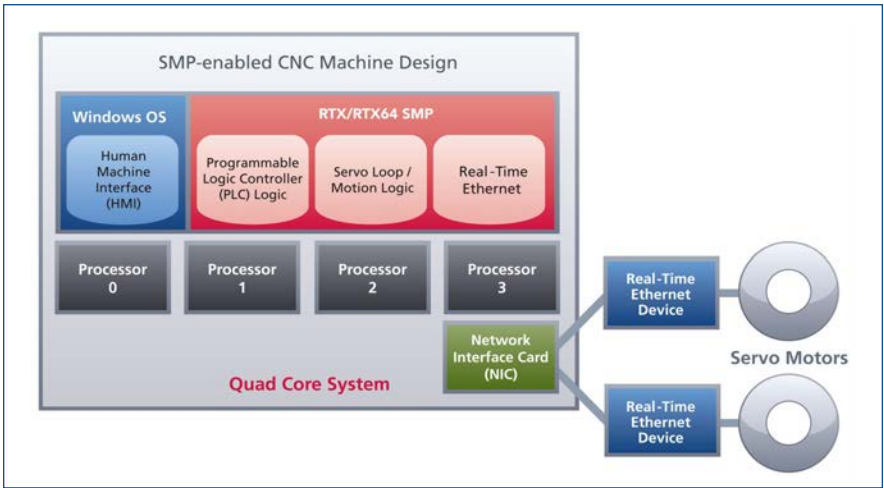


Figure 1 | The soft motion control architecture depicted here illustrates how the symmetric multiprocessing (SMP) capabilities of modern multicore x86 processors can be combined with Microsoft Windows and the IntervalZero RTX64 real-time extension to reduce costs and improve performance in control applications.

Figure 2a

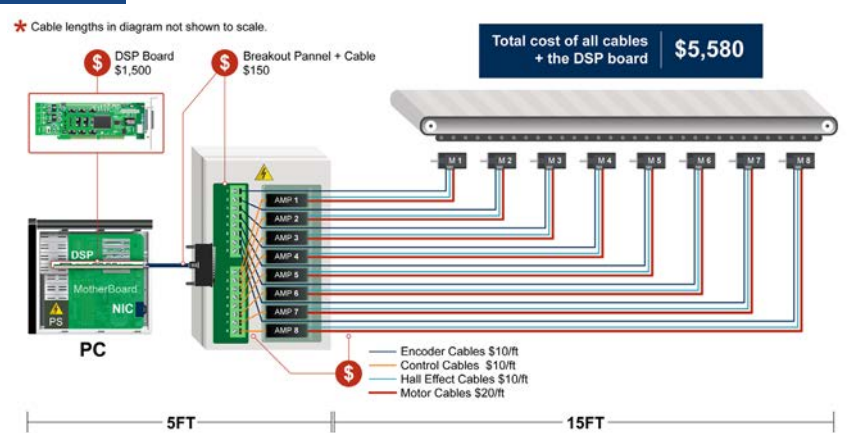


Figure 2b

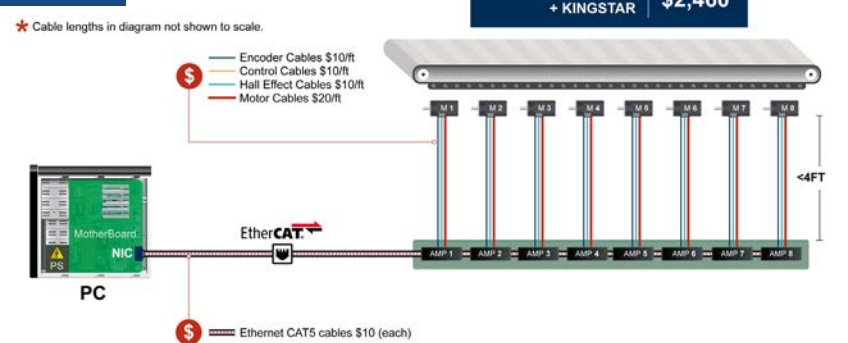


Figure 2a | Traditional hardware-centric control architectures require multiple components that significantly drive up costs, as seen in this 8-axis control system architecture. **Figure 2b** | Using soft-motion control technology running on an off-the-shelf x86 processor, the same 8-axis system architecture costs 44 percent of the hardware-centric implementation.

A software approach to machine control like KINGSTAR enables exactly that. With equal or better performance than traditional hardware solutions at less than half the cost, soft motion control is the clear choice for real business results. **IES**

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Industrial Internet through the wire with EtherCAT Technology Group

Interview with Martin Rostan, Executive Director, EtherCAT Technology Group

With all the fuss around wireless connectivity for the Internet of Things (IoT), it's sometimes easy to forget that the backbone of industrial systems is built on wired fieldbus technologies. While some of those legacy fieldbus technologies are starting to give way, EtherCAT, the "Ethernet Fieldbus" is not only continuing to succeed in industrial markets, but also preparing for integration with wider Industry 4.0 technologies and deployments. Martin Rostan, Executive Director of the EtherCAT Technology Group, explains.



What will the role of fieldbuses and Industrial Ethernet be as Industry 4.0 takes hold?

ROSTAN: The core of Industry 4.0 is communication. There are certain communication levels where wireless Ethernet provides sufficient determinism, bandwidth, and reliability, but when it comes to process data communication, hard real-time capabilities with short cycle times are required. This can

only be provided by fieldbuses and certain industrial Ethernet technologies.

Remind us about EtherCAT technology and how its topology helps separate it from other Industrial Ethernet protocols in terms of performance, cost, and safety.

ROSTAN: EtherCAT is characterized by its unique functional principle: Instead of sending one frame to each node and

receiving a response from each node in every cycle, EtherCAT sends just one frame through all the nodes. Each node extracts its data from that frame on the fly and can insert data into the very same frame as well. So all of them share one frame and one overhead, and as a result, we optimize the bandwidth utilization and get the best possible performance out of a standard Ethernet frame. This makes EtherCAT

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Solid State Drives 101: Everything You Ever Wanted to Know

By Steve Larrivee, Cactus Technologies

Solid-state drives (SSDs) are no longer the drives of the future — they're the drives of the present. If you haven't noticed, they are no longer cost prohibitive, and their performance and stability make them must-have components for a host of applications.

In this white paper, you'll learn about the different types of SSDs, the characteristics of each type, and most importantly, which one is best for your application, along with how it should be implemented.

Link: <http://embedded-computing.com/white-papers/white-101-everything-ever-wanted-know/>



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by far the fastest industrial Ethernet technology and the only one that supports hard real-time without any special chip in the master – which makes every embedded μ C-Board with an Ethernet port an EtherCAT master by hardware. Since nodes can have multiple ports, they can support any topology without using switches, which further reduces costs. And since EtherCAT requires no IT expertise, it is very simple to use. We call it the Ethernet Fieldbus, which not only mirrors ease of use, but also mirrors the low costs. Last but not least, the Safety over EtherCAT protocol allows one to cover functional safety applications with the same bus system as well.

Recently, the EtherCAT Technology Group announced a partnership with the OPC Foundation to help facilitate interoperable, continuous communications through all layers of industrial networks. Can you provide some background on the work there, and whether it will require any significant changes to EtherCAT technology?

ROSTAN: With OPC, we are working on interface specifications that will enable EtherCAT systems to publish process data to any Industry 4.0 capable entity, including but not limited to cloud services. Furthermore, such entities can also be granted access to all parameters and settings within the system, which makes the system fully remote manageable. This will enable smooth and seamless integration of EtherCAT-based systems within any digital factory environment.

As mentioned, the core of both Industrial IoT (IIoT) and Industry 4.0 is communication: reliable, fast, real-time, and deterministic communication is required at the controls level. This is exactly what EtherCAT is all about, so there is no need for any fundamental change since EtherCAT already meets these requirements. We may have to add certain IIoT and Industry 4.0 interfaces, and perhaps also data description methodologies once they are fully defined and stabilized, but the EtherCAT core technology itself is completely stable and has been since 2003. In fact, we consider this a major advantage of EtherCAT: while most competing technologies have versioning issues, members of the EtherCAT Technology Group can rely on

a technology where features are added, but the version has never changed. This is one of the reasons EtherCAT has the best adoption rate and the widest product range in the industry.

Given the strength of EtherCAT, is there an end to fieldbus technology in sight?

ROSTAN: Yes and no. Yes, since most new control architectures are now implementing modern Ethernet-based technologies such as EtherCAT; it's easy to implement and use, it's incredibly fast, it provides many features that legacy bus technologies cannot support, and, of course, it's a very good fit for embedded systems.

And no, since EtherCAT is a fieldbus technology. The legacy bus technologies will remain in place for a long time, too. **IES**

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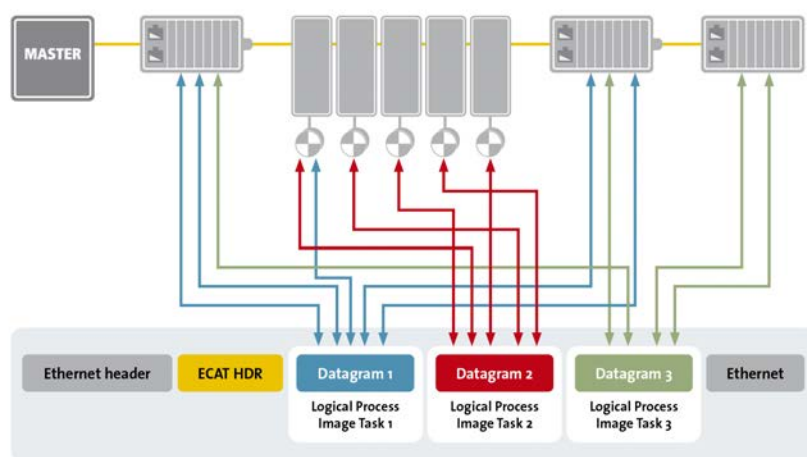


Figure 1 | A fundamental principle of EtherCAT is its ability to insert process data on the fly.

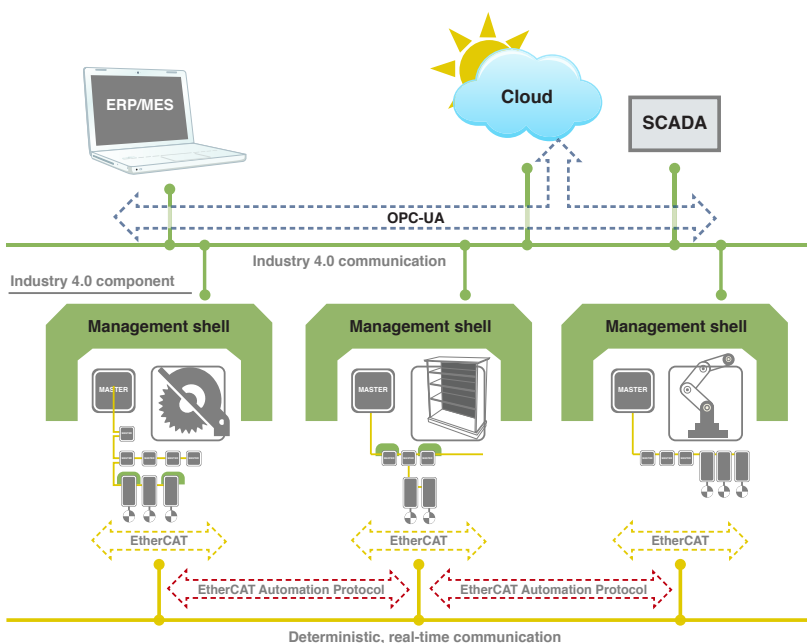


Figure 2 | A recent Memorandum of Understanding (MOU) between the EtherCAT Technology Group and OPC Foundation aims to define an interface based on EtherCAT that maps existing devices and machines into an Industry 4.0 conformant methodology.

Leveraging embedded industry standards for flexible IoT gateway designs

By Dan Demers

Market research firm VDC emphasized in a recent study that Internet of Things (IoT) gateways are the essential link between heterogeneous local sensor networks and enterprise applications. The following case study explores the challenges of implementing such a solution, and how MyOmega Systems Technologies was able to develop a uniquely flexible and secure IoT gateway based on industry-standard hardware modules and embedded design expertise.

A recent survey that records the status of the implementation of IoT or Industry 4.0 applications points out that it takes considerable effort and time to turn ideas into reality.[1] Only 3 percent of respondents were able to fully implement their Industry 4.0 application and only 12 percent have implemented their first partial solution. Furthermore, 85 percent are still in the early stages, ranging from the evaluation and planning to the first pilots. The mass implementation stage is therefore still to come. However, in four years' time, up to 50 billion devices are expected to be connected via the IoT.

Initial IoT projects are often hampered by all kinds of issues. There are clouds, but no cloud solution for the specific application; there are many appropriate services that can be used in isolation, but they are often not secure; sensors and machines come with connectivity, but the infrastructure is mixed and an "integrated solution" is different for each company; and, finally, one large challenge is the gateway design.

In this challenging environment, MyOmega System Technologies is faced with delivering industrial customers



high-performance, rugged gateway solutions that have extended security, flexible programming modules, and expanded connectivity options versus standard, off-the-shelf gateways. Not only must these platforms be able to interface the field and process levels of complex systems, but they must also be engendered with the capacity to manage hundreds or thousands of sensor nodes across transmission distances ranging into the thousands of meters.

The IoT applications that MyOmega supports can be extremely diverse. For example, smart farming applications can require a 3000-meter wireless communication link between the IoT gateway and the sensors in the field. Logistics applications designed to measure the fill levels of kanban containers via image recognition executed on a gateway can be composed of up to 3,000 bins connected per individual gateway node.

These examples show the diverse tasks performed by IoT gateway platforms, not the least of which is security. Because of the computational overhead of security applications, most of these functions must be offloaded from resource-constrained edge devices to more powerful, centralized gateway nodes. Standard box PC gateway solutions typically only support a few common interfaces via extension cards for communication with the edge, limiting MyOmega's ability to deliver a platform capable of communicating with the widest possible range of systems. Therefore, the company elected to develop its own IoT gateway based on the principles of flexibility and security.

A standards-based approach to full-featured flexibility

The result is the MYNXG Gateway, a hexagonal industrial networking platform that provides middleware and protocol support for IoT applications (Figure 1). The system can be equipped with eight antennas (LTE, HSPA, 2x WLAN) and six radio modules. Additionally, the MYNXG Gateway supports a mid-range radio solution for the 868 MHz and 2.4 GHz bands based on connectivity standards such as IEEE 802.15.4, 6LoWPAN, and CoAP to enable wireless communications over distances of up to 3 km.

MYNXG is an example of how industry-standard hardware platforms can significantly shorten the time from concept to production-ready solution. Leveraging Congatec's Embedded Design & Manufacturing (EDM) services, MyOmega was able to quickly specify the design of a carrier board to bring out the hardware interfaces required by MYNXG gateway deployments, and utilize the off-the-shelf, Intel Atom-based Conga-QA4 Qseven computer-on-module (COM) as the system's processing element.

In addition to the time-to-market savings of this modular approach, the Qseven COM architecture allows processor modules to be swapped out based on the requirements of different industrial applications, or in the event that component or performance upgrades are needed down the line. Partnering with Congatec's EDM team also allowed MyOmega to leverage thermal, signal integrity, and validation expertise from the embedded industry to reduce their time-to-market with the MYNXG Gateway by 60 percent while also ensuring the platform isn't hampered by transmission capabilities.

A familiar gateway to new applications

IoT, Industry 4.0, and clouds are the latest focus in the industrial sector, and many new applications are being developed to take advantage of these changes in technology. Gateways that provide secure, reliable communications and device management capabilities are essential to the success of these applications, as they bridge the technology gap between sensor devices and back-end

business intelligence systems. But this is not reinventing the wheel; embedded solutions have been addressing the requirements of industrial IoT gateways for years, just using a different moniker. And they've been doing so as modular standards, available off the shelf. **IES**

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Figure 1 | The MyOmega Systems MYNXG Gateway is a flexible, industry standards-based platform that offers broad wireless support and secure communications rooted in BitLocker encryption.

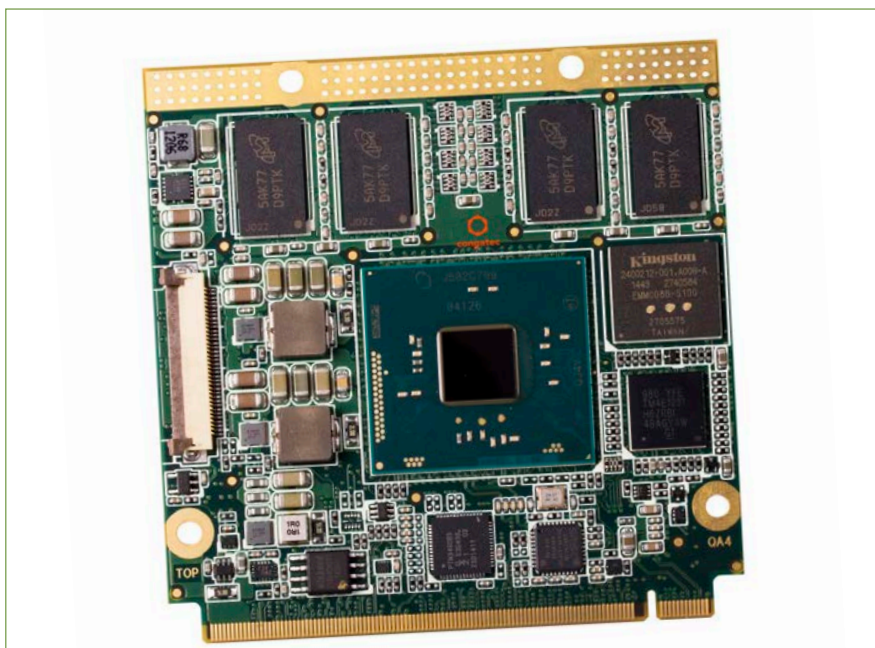


Figure 2 | The Congatec Conga-QA4 Qseven module based on Intel Atom processors provides a modular approach to Industrial IoT gateway design.

Inside the mind of machines: AI modeling scales security, analytics on the Industrial Internet

By Brandon Lewis, Technology Editor

The advent of the Industrial Internet has raised the bar for security analysts and data scientists, a workforce whose number is quickly being dwarfed by the amount of connected machines. Now, machine learning and artificial intelligence professionals are teaming with traditional embedded vendors to help suppress the rising tide of cyber threats and Big Data.

On their website, cybersecurity firm Norse Corporation generates a detailed, real-time map of cyber attacks occurring around the world, including the attack origin, attack type, and attack target (Figure 1). Hundreds of attacks are registered in any given minute, which, while disconcerting, pales in comparison with the number of systems being connected to the Industrial Internet.

This brief exercise demonstrates a couple of things: 1) the quantity and speed of cyber threats that can be used to attack vulnerable, safety-critical industrial systems; and 2) the growing need for data scientists and security analysts¹, as well as tools and technologies to support them as the Internet of Things (IoT) expands. According to information from the U.S. Bureau of Labor Statistics, 82,900 information security analysts were employed in 2014, a figure projected to grow by 18 percent through 2024². However, as the number of connected devices grows into the billions, will roughly 100,000 security professionals be sufficient to offset the majority of cyber attacks targeted at connected industry?

Consider this question in the context of a single analyst reviewing security logs of 1,000 connected machines at random.



Assume that 95 percent of the logs ingested by the operator's security information and event management (SIEM) system conform to normal operation, while the remaining 5 percent of logs are suspicious (containing evidence of potential intrusions or violations). This equates to a total of 50 potential security threats in the entire collection, but also implies that the analyst will investigate 20 logs on average before encountering an actual threat, and need to repeat this log-checking process 50 times before encountering all threats (again, on average). If one of the 50 potential threats includes sophisticated malware such as Stuxnet or Duqu designed to commandeer the operation of cyber-physical industrial control systems or wipe hard drives, the analyst may not be able to intervene in time to protect millions of dollars worth of equipment or IP. Meanwhile, events continue to occur for all devices connected to the network.

The lesson here on the state of today's cyber defense work force should be clear to operators of safety-critical infrastructure, the security industry, and the IoT at large. But the prior examples also prompt a secondary realization that the signature-based methodologies used by firewalls to authenticate packets crossing the network, as well as by local antivirus software used to prevent malware from launching on a device, are no longer sufficient security technologies by themselves in today's cyber-physical world. Both Stuxnet and Duqu leveraged stolen or abused keys to gain access to target systems, and with digital signature libraries constantly in flux, it is difficult, if not impossible, for signature-based security systems and the analysts that rely on them to consistently mitigate threats.

To augment security teams, players in the Industrial Internet need to permit security professionals to quickly evaluate potential threats by embedding an "engineer, or at

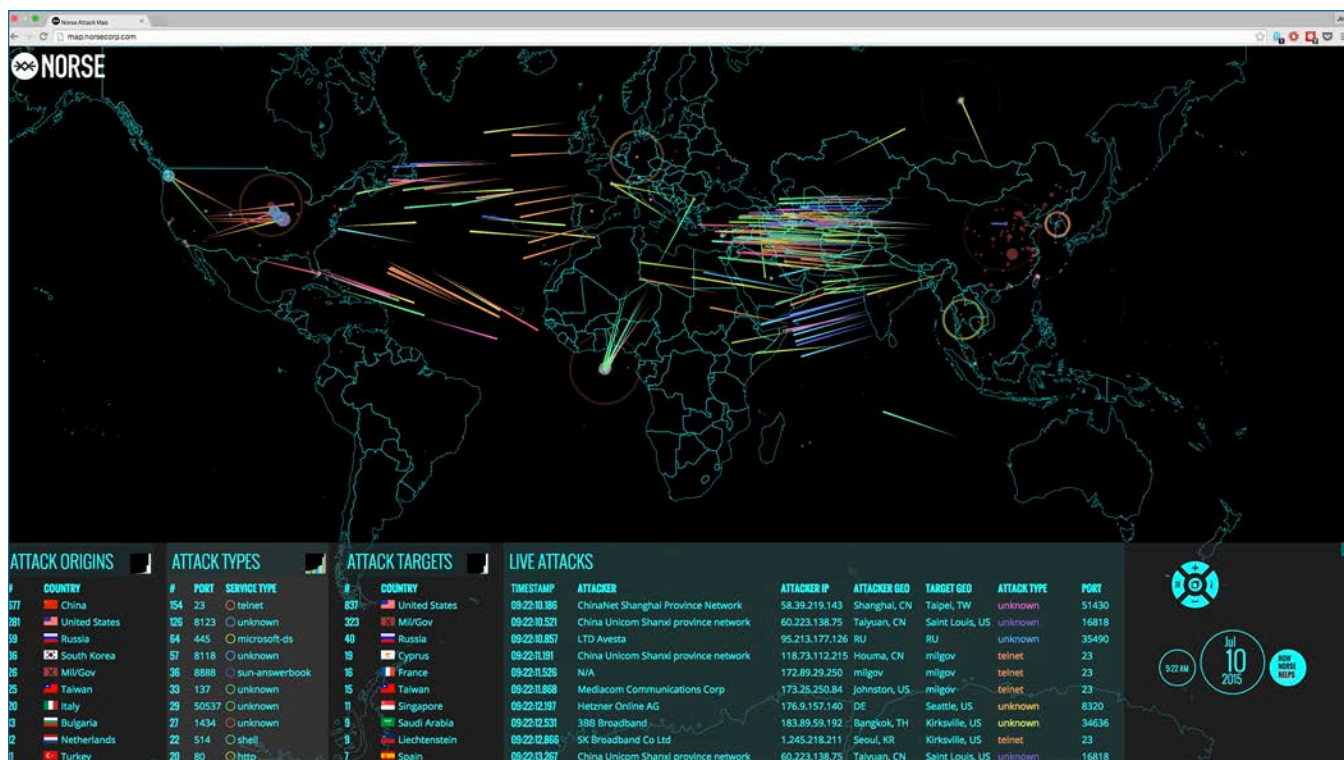


Figure 1 | Norse Corporation produces a real-time map of worldwide cyber attacks, which calculates hundreds per minute.

least that level of intelligence, in every machine,” says Amir Husain, Founder and CEO of SparkCognition.

“Embed a brain [into the system] that is the equivalent of a high-end mechanical engineer that can monitor the system,” Husain says. “If you visualize it that way, it’s no longer about what virus, whether it’s called Stuxnet, whether it’s called Flame, or whether it’s called a third name, the point is that you are monitoring the symptoms and the entire system out of band. Regardless of how the threat got in, you’re out of band of the IT network and you’re looking at the typical behavior of the system and saying, ‘Hey, the level of vibration or the speed at which this motor is running or the harmonics just don’t look good, and I’m predicting that this device will fail imminently. The gradient of that remaining, useful life curve is so sharp that this cannot be just normal wear and tear.’

“We’re talking about embedding a brain, a specialist’s brain, with every system and having the ability to evolve that brain to the custom needs of every individual device. When we talk about dynamically

evolving models of behavior and having the capabilities for these models to learn and adapt to the specific asset over time, that’s really what we’re talking about.”

Genetic competition feeds intelligent machines

Founded in 2013, SparkCognition is an artificial intelligence (AI) and machine learning firm that develops algorithms and decision-making models that automate the creation of cognitive, intelligent systems. Based on technology whereby structured,

Probability of detection of first security threat against the number of items

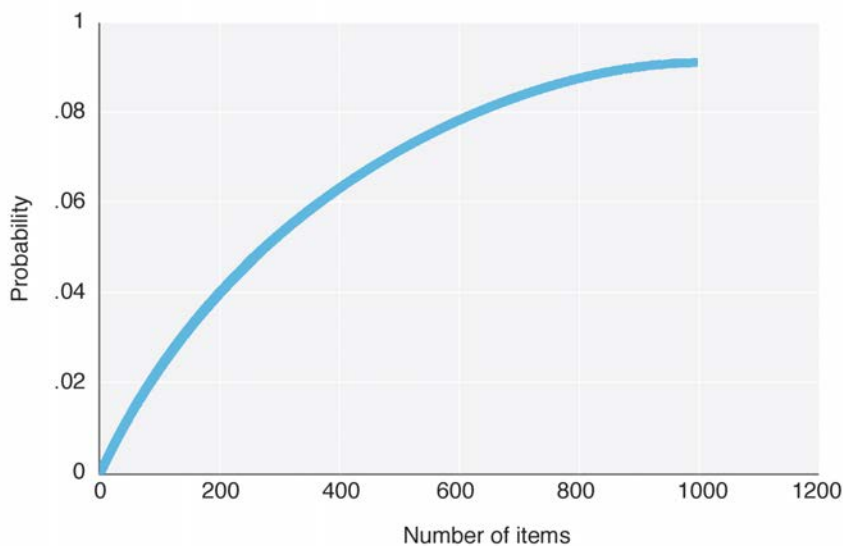


Figure 2 | Assuming that five percent of security logs contain actual threats, security analysts are forced to manually review as many logs as possible to increase the probability of detecting said threats.

semi-structured, and unstructured data is acquired and mined (see Sidebar 1), SparkCognition's SparkSecure platform layers cognitive intelligence into traditional security solutions to permit the detection of zero-day attacks (signature-less threats), monitoring of threat behavior to predict potential future attacks, and efficiency scaling of security teams by analyzing and sorting log data before prioritizing those records for analyst review. These capabilities can be brought down to the individual system level, which is made possible by elastic machine learning models generated through a process known as ensembling.

Given the various schools of thought in the AI community around model creation – including neural networks, Bayesian statistics, hidden Markov models (HMMs), natural language processing, and support vector machines (SVMs) – *ensembling* provides a multi-disciplinary approach to cognitive modeling that combines various machine learning techniques in somewhat of an automated genetic competition to produce the best result for a given machine serving a specific purpose. This strategy enables the best possible solution for cognitive systems (which have

traditionally been limited to learning in a brittle if/then/else-type fashion), and also allows model development to occur at speeds exponentially faster than possible if built by human engineers. To describe the ensembling process, Husain imagines four engineers in a room working to solve a complex problem.

"Let's say you come from an electrical engineering background and I come from a software engineering background and Nick comes from a mechanical engineering background and John comes from a structural engineering background," he says. "We have a problem that we collectively put our minds to and we all bring our perspectives to it.

"Often what happens is that it's not that one person is absolutely right and three others are absolutely wrong, but that there's some mixture of value that can be put together to create something that's composite, that's better than any one idea alone," he continues. "SparkCognition uses automated algorithms to create models using different techniques, as, for example, you might want to model something as an HMM in a deep neural network and through a Bayesian

filter, and have all of this on an SVM. Ensembling, which is the combination of various different solutions, is a form of competition, and usually we employ genetic techniques to induce competition between auto-assembled and auto-created models. It's about taking every tool at your disposal and having an automated way to apply all those tools to learn from the application as to what was effective and what was not, and then creating a composite solution that solves the problem in the best way possible.

To accelerate the development of precision models for cognitive machines, SparkCognition maintains an active network of systems in order to collect data of relevance to the industries it serves, which can then be used to augment device data gathered from a system itself. For example, security information gathered since the company's inception can be used to supplement data from a newly deployed machine, thus accelerating return on investment (ROI) as the algorithm and model development process does not have to start from scratch. For industrial customers, trained models can be operational in a timeframe spanning hours to a few days.

Structured data ingress for cognitive and intelligent systems

An often overlooked challenge in the worlds of Big Data and the Industrial Internet is the collection of data from sensor devices themselves in a manner that is ingestible by cloud/IT backends. For example, inputs could include structured (binary), semi-structured (part binary, part text), or unstructured (text-heavy) data, making it difficult for other machines, and even cognitively intelligent platforms, to interpret.

To ensure unified data capture across a diverse range of connected devices for its SparkSecure and SparkPredict (for data analytics and predictive maintenance) offerings, SparkCognition has partnered with National Instruments (NI), creator of the technical data management streaming (TDMS) file format. Unlike other file formats such as ASCII and XML that emphasize application planning, software architecture, or system design and leave storage decisions to the organizational processes of operators, TDMS was initially architected for storing test and measurement data in a highly structured, scalable, streamable, and exchangeable way that prevents information silos from occurring on isolated machines. According to Jamie Smith, Director of Embedded Systems at National Instruments, this "open, documented standard to efficiently organize and analyze data" is critical to data acquisition systems, as well as the prognostics and machine learning systems they feed.

"TDMS provides both binary and metadata to document the data set for additional analysis and provide efficient storage and transport across the

network," Smith says. "The TDMS file format is used to organize and analyze engineering design data, test data, and analog operational data. Companies are using this format in conjunction with our technical data analysis tool DIAdem and InsightCM Enterprise to improve overall quality, reduce maintenance cost, and increase uptime."

TDMS files are hierarchically structured into three distinct classifications: File, Group, and Channel. This model allows for descriptive information to be included in the file along with other data, so that data sets can be easily documented and scaled as application or system requirements evolve.

"This data format is used with several machine learning and prognostics offerings, including NI's machine learning tool kit, Watchdog Agent (whose prognostics were developed in collaboration with the Center for Intelligent Maintenance Systems), SparkCognition's prognostics tools, and has been integrated into IBM's Bluemix as part of the Industrial Internet Consortium Predictive Maintenance Testbed hosted by National Instruments," he continues. "Because all of these tools can ingest TDMS, you can separate data acquisition from your analytics choices to allow flexibility when choosing an analytics tools offering."

For more information, access a TDMS white paper at www.ni.com/white-paper/3727/en.

Artificial Intelligence:

May the disruption commence

However, getting trained models operational is only part of the job, as the model generated for a particular system is only as good as the data available to it at the time of its creation. Actual intelligence requires the ability to account for new logs and sensor data generated by the system (as well as human input received) well after initial model deployment and into the future. For this purpose, SparkCognition's "Cognitive Fingerprinting" algorithms are used to analyze diverse data sets and recognize patterns forming in real time, for example by predicting a change in system state. A partnership with IBM also facilitates integration with the Watson platform so that Watson can provide remediation responses in the event of a system anomaly.

Considering these capabilities, in addition to working relationships with embedded data acquisition vendors like National Instruments that aid in unified data ingress, the end-to-end nature of emerging AI ecosystems such as SparkCognition's suggests that systems are in a position to operate completely autonomously, with minimal need for human intervention. But, how realistic is that today? Husain explains.

"SparkSecure, out of the box, is able to act entirely autonomously," he says. "SparkSecure can be deployed in an environment where it can sense an attack, it can determine the likelihood of this being a real attack versus a false positive, and then can take action, which includes things like making a change to a firewall, disabling a user account, killing a service, and so on. But the reality is that, for non-technical reasons, most of our customers elect to have these actions vetted by an incident response professional before they are implemented.

"This is new technology. Think about the self-driving car. Google has already shown that the self-driving car can do better than most human drivers, but there is a reticence and a nervousness around simply going ahead and

implementing that as a technology that's common," Husain continues. "[AI and machine learning] are similar. These systems work really, really, really well in their current form, and SparkSecure already augments human security professionals and allows one person to look at more data than they could ever have looked at on their own, and it proposes the actions as well. But when it comes to actually making the change, our customers are at the point where they want that human validation, which I completely

understand. But, ultimately, at some point in the future, can such a system be autonomous? Of course." **IES**

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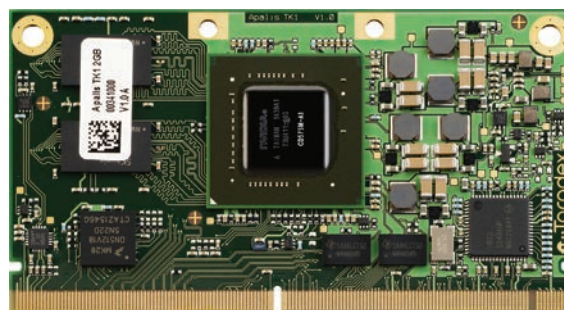
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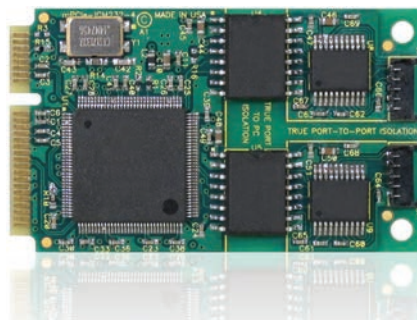
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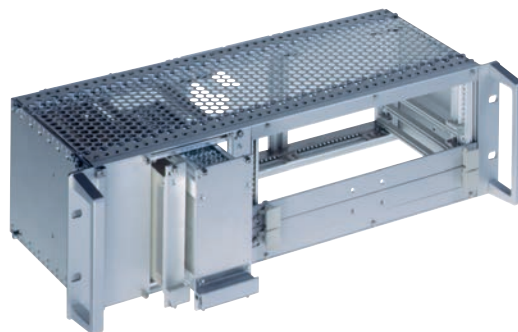
Intermas – Modular Assembly Systems

Intermas develops, manufactures and markets components and modules for the packaging of electronics:

Cabinets, housings, subracks, cassettes and an extensive range of accessories for the 19" rack systems. The electronic enclosure systems are used in the fields of PCI, VME/VME64x, cPCI, IEEE, and communication applications with state-of-the-art EMI and RFI-shielded protection.

Intermas offers wiring connectors and cable interface housings in accordance with IEC 60 603-2/ DIN 41 612, bus bars, 19" cross flow fans, power supplies, and euroboard covers. Intermas has extensive product range of more than 10,000 separate components and more than 30 years of experience.

**Go to www.intermas-us.com
for our new catalog.**



FEATURES

- > 19" subracks and housings with flexible internal layout in various 3U and 6U sizes
- > EMI and RFI-shielded protection using stable stainless steel contact springs ensuring permanent and reliable bonding
- > CompactPCI modules with integrated bus board and power supply
- > InterRail® product line to meet tough physical demands and vibration-proof used for railway engineering, traffic engineering, and power station engineering
- > Connectors and wiring accessories
- > Customizations available

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Industrial Hardware

BayCat (VL-EPM-31)

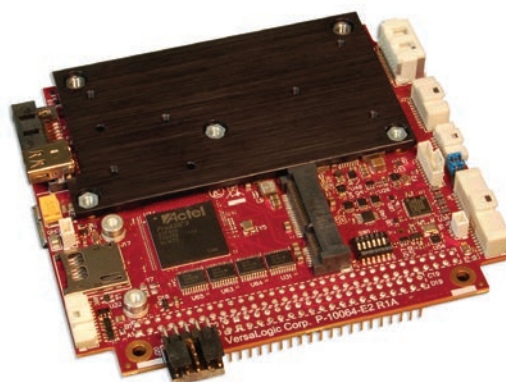
PC/104-Plus "Bay Trail" Embedded Computer

BayCat is a rugged new PC/104-Plus™ single board computer (SBC) with on-board Trusted Platform Module (TPM) for enhanced security. BayCat combines high performance, low power consumption, and backwards compatibility with systems using PC/104-Plus ISA or PCI expansion. Built for extreme environments, the BayCat is designed and tested for industrial temperature (-40° to +85°C) operation and meets MIL-STD-202G specifications to withstand high impact and vibration. Latching connectors and fanless operation provide additional benefits in harsh environments.

BayCat is available in single-, dual-, and quad-core processor options to meet a variety of price/performance/application requirements. BayCat features a Mini PCIe socket with plug-in Wi-Fi modems, GPS receivers, and other mini cards such as MIL-STD-1553, Ethernet, and Analog. For stacking expansion using industry-standard add-on boards, the BayCat supports PC/104-Plus expansion.

The BayCat's on-board TPM security chip can lock out unauthorized hardware and software access providing a secure processing environment for applications in applications that require hardware-level security functions. Additional security is provided through built-in AES (Advanced Encryption Standard) instructions.

The BayCat is backed by VersaLogic's 5-year warranty and product life extension programs that can continue delivery well past the year 2025.



FEATURES

- > -40°C to +85°C operation
- > TPM hardware security
- > Fanless Operation; Latching connectors
- > PC/104 Format: 4.3 x 3.8" (108 x 96 mm)
- > One, two, and four-core models
- > Up to 8 GB RAM; VGA and DisplayPort video outputs
- > ISA, PCI and SPI expansion

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VersaLogic Corporation
<http://www.versalogic.com/0316-IES-BayCat>

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in [linkedin.com/company/versalogic-corporation](https://www.linkedin.com/company/versalogic-corporation)

☎ 503-747-2261
🐦 @versalogic



cPCI, PXI, VME, Custom Packaging Solutions

VME and VME64x, CompactPCI, or PXI chassis are available in many configurations from 1U to 12U, 2 to 21 slots, with many power options up to 1,200 watts. Dual hot-swap is available in AC or DC versions. We have in-house design, manufacturing capabilities, and in-process controls. All Vector chassis and backplanes are manufactured in the USA and are available with custom modifications and the shortest lead times in the industry.

Series 2370 chassis offer the lowest profile per slot. Cards are inserted horizontally from the front, and 80mm rear I/O backplane slot configuration is also available. Chassis are available from 1U, 2 slots up to 7U, 12 slots for VME, CompactPCI, or PXI. All chassis are IEEE 1101.10/11 compliant with hot-swap, plug-in AC or DC power options.

Our Series 400 enclosures feature side-filtered air intake and rear exhaust for up to 21 vertical cards. Options include hot-swap, plug-in AC or DC power, and system voltage/temperature monitor. Embedded power supplies are available up to 1,200 watts.

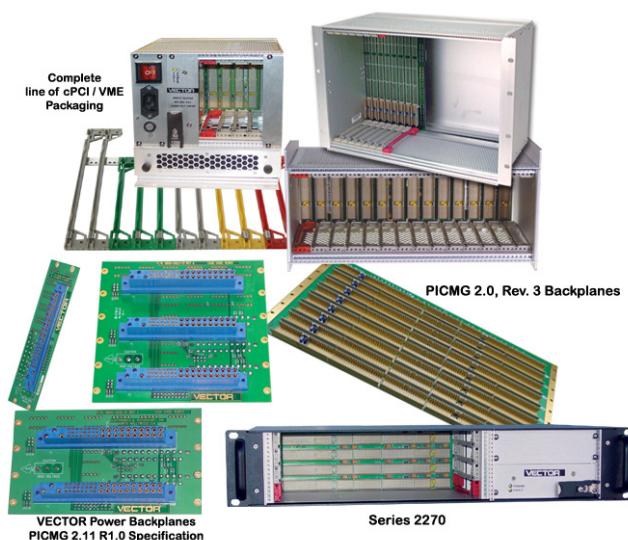
Series 790 is MIL-STD-461D/E compliant and certified, economical, and lighter weight than most enclosures available today. It is available in 3U, 4U, and 5U models up to 7 horizontal slots.

All Vector chassis are available for custom modification in the shortest time frame. Many factory paint colors are available and can be specified with Federal Standard or RAL numbers.

For more detailed product information,
please visit **www.vectorelect.com**

or call

1-800-423-5659 and discuss your application
with a Vector representative.



FEATURES

- > Made in the USA
- > Most rack accessories ship from stock
- > Modified 'standards' and customization are our specialty
- > Card sizes from 3U x 160mm to 9U x 400mm
- > System monitoring option (CMM)
- > AC or DC power input
- > Power options up to 1,200 watts

industrial.embedded-computing.com/p371649

Vector Electronics & Technology, Inc.
www.vectorelect.com

✉ inquire@vectorelect.com
☎ 800-423-5659

Fox (VL-EPM-19)

Rugged PC/104-Plus Embedded Computer

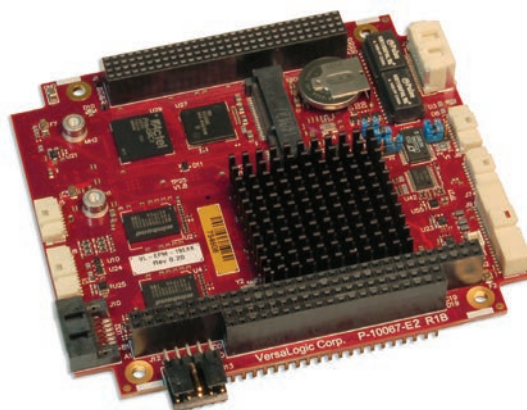
Fox is a rugged new PC/104-Plus™ single board computer (SBC). It features the compactness of the PC/104 form-factor, and the compatibility of the classic PC/104-Plus expansion interface – with ISA and PCI bus expansion. It also features extensive I/O capabilities, low power consumption, and fanless operation over the full industrial temperature range.

The Fox is a full-featured SBC for low power embedded environments that require passive cooling. It delivers mid-range performance and lower power draw along with industry-standard PC/104-Plus compatibility.

The Fox leverages DMP's Vortex86DX2 System on Chip. It offers full industrial temperature (-40° to +85°C) operation, and low power requirements (5.3 Watts). It provides I/O expansion through the PC/104-Plus stackable bus (PCI + ISA), as well as a Mini PCIe socket, MicroSD socket, and a SPI/SPX interface.

Designed and tested to withstand extreme temperatures, high-impact, and vibration, Fox features no moving parts and soldered-on RAM. This single board computer is an ideal choice for applications that require a rugged, high reliability computer.

The Fox is backed by VersaLogic's 5-year warranty and product life extension programs that can continue delivery well past the year 2025.



FEATURES

- > -40° to +85°C Operating Temperature
- > Soldered-on RAM (up to 1 GB)
- > Fanless Operation; High shock and vibrate
- > DMP Vortex86DX2 32-bit Processor
- > VGA and LVDS video outputs
- > Mini PCIe/mSATA socket
- > PC/104-Plus expansion; SPI/SPX Expansion

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🐦 @versalogic



Intelligent IoT Gateway Starter Kit

ADLINK's Intelligent IoT Gateway Starter Kit provides a complete IoT connection solution for reduced development time and quick deployment for every application environment. The starter kit combines ADLINK's MXE-202i intelligent IoT gateway based on Intel® Atom™ E3826 processors, ADLINK's EdgePro IoT device & sensor management application, one light sensor and corresponding siren output, Modbus TCP module and accessories, all utilizing industrial open standard protocols with security functions powered by the Intel® IoT Gateway. The starter kit simplifies device-cloud connection, accelerates IoT application development and speeds deployment for a wide variety of application environments, such as industrial automation, smart buildings, smart parking systems and agriculture.

The ADLINK EdgePro runs on the Intel® IoT Gateway, integrating the Wind River Intelligent Device Platform® (IDP) XT and McAfee® Embedded Control to provide complete, pre-validated communication and security. EdgePro enables device and sensor management via plug-in(s) for field protocols including ZigBee (Home Automation Profile) and the commonly adopted fieldbus Modbus TCP for industrial automation. Interaction across devices/sensors is accomplished by an Event Execution Engine, and a web-based dashboard allows remote monitoring of status and actuator control with RESTful web-service APIs. EdgePro enables simple configuration of reliable and secure connectivity with Amazon and Windows Azure Cloud.



FEATURES

- > Provides a complete IoT connection solution for accelerated IoT application development
- > Equipped with MXE-202i dual-core Intel® Atom™ SoC processor E3826 IoT Gateway on Wind River® IDP XT 2.0
- > Preloaded ADLINK EdgePro IoT device & sensor management application
- > Easy configuration with user-friendly administrator interface and dashboards
- > Includes light sensor, siren output, Modbus TCP module and accessories
- > MXE-202i: shock tolerance up to 100 G and optional extended -20°C to 70°C operating temp

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ADLINK Technology

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ELMA

Your Solution Partner

Industrial Internet/IoT

NetSys-5401 Industrial Cisco Router

The **NetSys-5401** is optimized for mobile and embedded networks that require IP routing and services. Featuring Cisco's 5915 Embedded Services Router the flexible, compact system provides highly secure data, voice, and video communications to stationary and mobile network nodes across wired and wireless links. The system offers high performance with five Fast Ethernet interfaces (two routed and three switched), and a rich Cisco IOS Software feature set for customers deploying bandwidth-intensive applications in embedded networks in industrial, public safety, transportation, defense, and energy markets. Cisco's on board hardware encryption provides scalable video, voice, and data services for mobile and embedded outdoor networks. Optional Advanced Enterprise package provides protocol support for Cisco's Mobile Ready Net features including mobile ad hoc networking and radio aware routing.



FEATURES

- > Five 10/100 Fast Ethernet ports (two routed and three switched)
- > Cisco IOS-Managed Embedded Services Router (ESR) including Cisco advanced encryption and mobile routing protocols
- > Cisco 5915 Advanced Enterprise IOS including support for mobile ad hoc networking and radio aware routing (optional)
- > 512 MB DRAM and 256MB flash memory
- > Fanless SWaP optimized rugged construction

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Elma Electronic Inc.

<http://www.elma.com/en/products/systems-solutions/application-ready-platforms/product-pages/cisco-routers/netsys-nts-54e-01-compact-embedded-services-router-detail/>

✉ sales@elma.com ☎ 510-656-3400 @elma_electronic
 in <https://www.linkedin.com/company/elma-electronic>



Industrial Internet/IoT

TANK-860-QGW

QTS Gateway is an operating system designed specifically for IEI IPCs and fully inheriting the QNAP NAS operating system (QTS), breaking through the stereotype of IPCs not having operating systems and saving unnecessary costs for installing servers and computers. "TANK-860-QGW is the best way to get into cloud applications, especially in the aspect of operating system. With QNAP's years of software experience and the built-in Virtualization Station, users can seamlessly migrate their current operating platform to the virtual machine (VM) in QTS Gateway, and directly connect to the cloud through various apps in QTS Gateway. Therefore, the three main goals of industrial IoT (IIOT) – remote monitoring, preventive maintenance and asset management can easily be achieved," said Don Yu, Director of IEI.

QTS Gateway not only allows easy monitoring of computer activity through its visualized interface, it also allows the use of many free application programs, making it multifunctional while challenging the values of traditional IPCs. The TANK-860-QGW is installed with an iRIS-2400 module so that it can utilize the IoT concept to perform remote control, including power management/control, remote KVM monitoring or sending alarm and warning information through e-mail or SMS.



FEATURES

- > Intel® HM86 Chipset + 4th gen Intel® Core™ CPU
- > Ruggedized and Wide Temp support: -20°C ~ 60°C
- > Great Flexibility of expansion slots:
 - 2-slot: 2 x PCIe by 16, 1x PCIe Mini slot
 - 4-slot: 2 x PCIe by 16, 2 x PCI, 2 x PCIe Mini slot
 - 6-slot: 1 x PCIe by 16, 2 x PCIe by 4, 3 x PCI, 2 x PCIe Mini slot
- > IPMI function for remote control management
- > Three independent video outputs (DP, VGA, DVI-I) support high resolution
- > 2 x 2.5" SATA HDD bay design fulfills high storage demand
- > Remote visualization system and remote device manager
- > Integrated cloud management
- > RAID-0 and RAID-1 support for automatic backup
- > Multiple OS Support: Windows/Linux/UNIX

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ATP DRAM and NAND Flash Products

ATP Industrial Grade DRAM Products

ATP DRAM Modules are designed for high-performance, mission-critical applications such as Industrial PC and Networking/Telecom, where high levels of technical support, operating consistency, and wide operating temperature ranges are required. Built with high quality IC components and 100% tested, the ATP DRAM module family includes a full spectrum of form factors including VLP, ULP, UDIMM, RDIMM, SODIMM, and MINI-DIMM, as well as multiple generations of DRAM technologies.

ATP has a long history of providing long-term support and addressing specific requirements of OEM customers.

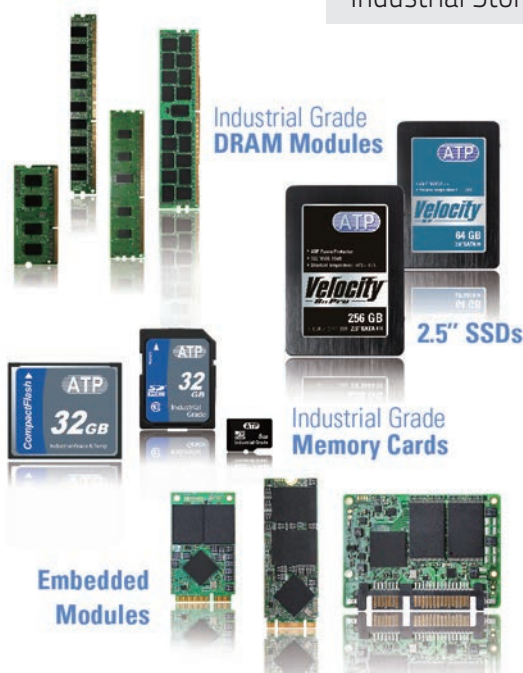
The new ATP Manufacturing, Testing and Validation facility offers enhanced manufacturing quality and TDBI/ATE testing capabilities on all DRAM product lines.

ATP Industrial Grade NAND Flash Products

Flash Product Line Summary: Memory Cards (microSD/SD), **Embedded Modules** (SATA, USB, eUSB), and **HDD Replacement SSD** (2.5" SATAII/III).

ATP Industrial Grade NAND Flash Products are designed for high-performance, mission-critical applications such as Automotive, Healthcare, Networking/Telecom, Military, etc., where high levels of durability, operating consistency, and wide operating temperature ranges are required. All ATP Industrial Grade NAND Flash products implement ECC and wear-leveling algorithms to maximize NAND Flash component utilization and long-term data integrity. The product line is also built using SLC (Single Level Cell)-type NAND Flash components, which are specified to at least 20 times greater the rating for program/erase cycles (lifetime) compared to commercial and consumer level MLC-type NAND Flash.

ATP is a true manufacturer with over twenty years of experience in the production of NAND Flash memory solutions and DRAM memory modules. ATP offers in-house design, testing and product tuning, as well as extensive supply chain support with controlled/fixed BOMs and long product life cycles.



FEATURES

ATP Industrial-Grade DRAM Products

- › JEDEC compliant
- › Extensive support on DDR4, DDR3, DDR2, DDR1, and PC133 SDRAM generation memory modules
- › Industrial Grade temperature range (-40°C to 85°C)
- › Conformal coating for environmentally rugged applications
- › Long-term supply chain commitment upon module qualification
- › ATP patented TDBI System – the next generation test during burn-in
- › Extra 30µ" thickness golden finger

ATP Industrial-Grade Flash Products

- › SLC NAND Flash Components
- › ATP patented PowerProtector Technology – Data integrity during a sudden power down
- › SMART/SD Life Monitor Technology – Flash health status feedback to host
- › Integrated Secure Erase Technology
- › Industrial Grade temperature range (-40°C to 85°C)
- › Supply chain road maps by BOM upon product qualification
- › Onboard AES Encryption (SSD Products)

New SATA III Products

- 2.5" SSD SII Pro
- 2.5" SSD MV
- M.2 2260/2242
- CFast
- mSATA
- SlimSATA

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The New IoT Has Arrived

Drop in LoRa® Technology Modules Deliver Long-Range, Low-Power Cloud Connectivity

The RN2483 and RN2903 are revolutionary end-node solutions that enable extremely long-range (up to 15 km), bidirectional communication with years of battery life for Internet of Things (IoT), Machine-to-Machine (M2M), smart city and industrial applications.

The RN2483 is a fully certified LoRa® technology modem for the European 433/868 MHz bands, and the RN2903 modem is for the 915 MHz North American band. Both modems come with the LoRaWAN™ Class A protocol stack, so they can easily connect with the rapidly expanding

infrastructure driven by the LoRa Alliance to create Low-Power Wide-Area Networks (LPWANs), both as privately managed scalable deployments or telecom-operated public networks with nationwide coverage. Due to the long range of LoRa technology, these modems are able to operate without repeaters, reducing the total cost of ownership.

Additionally, both the RN2483 and RN2903 are fully certified, which saves significant certification costs and reduces time to market.

The New IoT Has Arrived
Drop in LoRa® Technology Modules Deliver Long-Range, Low-Power Cloud Connectivity

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Modern Embedded Systems Programming

Embedded software developers are independently re-discovering patterns for building concurrent software that is safer, more responsive and easier to understand than naked threads of a Real-Time Operating System (RTOS). These best practices universally favor non-blocking, asynchronous, event-driven, encapsulated state machines instead of naked, blocking RTOS threads.

While these concepts can be implemented manually on top of the “free threading” approach, a better way is to use an active object (actor) framework, which inherently supports and automatically enforces the best practices of concurrent programming.

The QP™ family of active object frameworks from Quantum Leaps provides a lightweight, reusable architecture designed specifically for deeply embedded systems. The QP family consists of QP/C, QP/C++, and QP-nano frameworks, which are all strictly quality controlled and thoroughly documented. The frameworks are licensed as GPL open source as well as commercially.

The behavior of active objects is specified in QP by means of hierarchical state machines (UML statecharts). The frameworks support manual coding of UML state machines in C or C++ as well as fully automatic code generation by means of the free QM™ graphical modeling tool.

All QP frameworks contain a selection of built-in real-time kernels and can run on bare-metal microcontrollers, completely replacing a conventional RTOS. Native QP ports and ready- to-use examples are provided for major CPU families, such as ARM Cortex-M. QP/C and QP/C++ frameworks can also be used with many traditional RTOSes and desktop OSes (such as Windows and Linux).

Welcome to the 21st century!



FEATURES

- › Reusable architecture based on active objects (actors), which is safer and easier to understand than “free-threading” with a traditional RTOS
- › Simple-to-use coding techniques for hierarchical state machines (UML statecharts), with which to implement the behavior of active objects
- › Free QM modeling tool for drawing UML statecharts and automatic code generation based on QP frameworks
- › Efficient and thread-safe event-driven mechanisms for active objects to communicate, such as direct event passing and publish-subscribe
- › Selection of built-in RTOS kernels to run the QP applications, such as the cooperative QV kernel, the preemptive non-blocking QK kernel, and the preemptive blocking QXK kernel
- › Compliant with MISRA-C:2004 (QP/C and QP-nano) and MISRA-C++:2008 (QP/C++)
- › Book “Practical UML Statecharts in C/C++” with detailed design study of the QP framework, application notes, articles, user manuals, and blog

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Colibri iMX7

The newest member of Toradex's popular Colibri System on Module (SOM) product line is based on the NXP® i.MX 7 series applications processors. The Colibri iMX7 offers an outstanding performance/power ratio, advanced security features, and a heterogeneous multicore architecture based on ARM® Cortex-A7 and Cortex-M4 cores, which make the platform a perfect fit for products targeting the rapidly growing IoT market.

The additional Cortex-M4 core is tailored for real-time applications. This unique heterogeneous multicore architecture allows to separate critical tasks from UI or communication related applications. The i.MX 7 processor also includes additional security features such as secure boot, cryptographic acceleration and tamper detection, which are of high value for today's connected applications.

The Colibri iMX7 SOMs are an extension to the small form factor Toradex embedded computing SOMs and customized Single Board Computers (SBC), which are deployed in a variety of industries such as industrial automation, medical, automotive, robotics and more.

The new Colibri iMX7 is priced starting at 49 USD (@1K units) and is available for sale on the Toradex website.

For more information, please visit <https://www.toradex.com/colibri-imx7>



FEATURES

- > NXP i.MX 7 series applications processors
- > 1/2x ARM Cortex-A7 up to 1GHz plus Cortex-M4 at 200MHz
- > Up to 512MB RAM and 512MB on-board SLC NAND Flash
- > Asymmetric heterogeneous multicore processing architecture
- > Low power/high efficiency CPU with advanced security features
- > Connectivity: Ethernet, USB, CAN, SPI, I2C, UART, PWM, etc.
- > Multimedia: RGB Display, Camera Interface, Touch, Audio, PWM, GPIO, etc.

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Toradex

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Industrial Temperature iPac-9X25

Designed and manufactured in the USA, the iPac-9X25 is a Web-enabled microcontroller with the ability to run an embedded server and to display the current monitored or logged data. The Web connection is available via two 10/100-Base-T Ethernet ports or 802.11 wireless Wi-Fi networking when using the proper Linux modules and adapters. This micro-controller has all connectors brought out as headers on the board and has the same footprint of a standard PC/104 module at 3.77" x 3.54". The iPac-9X25 is perfectly suited for Industrial Temperature Embedded Data Acquisition and Control applications.

Pricing for Qty 1 is \$198.



FEATURES

- > Atmel AT91SAM9x25 400 MHz Processor
- > 128MB DDR2 RAM, 4GB eMMC, 16MB Serial Data Flash, Micro SD
- > 20 General Purpose Digital I/O lines, 16 SPI I/O Expander Based Digital I/O, and 8 High Drive Digital Outputs
- > 2x USB 2.0 (High-Speed) Host Port, 1x USB 2.0 (Full-Speed) Host Port, 1x USB 2.0 (High-Speed) Device Port, 1x CAN Bus
- > 3x RS232, 1x RS232/422/485, 2x 10/100 Ethernet
- > Up to 7 channels of 10 bit A/D, Up to 4 16-bit PWMs
- > Industrial operating range of -40C to +85C

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EMAC, Inc.

www.emacinc.com/products/pc_compatible_sbcs/IPAC-9X25

✉ info@emacinc.com

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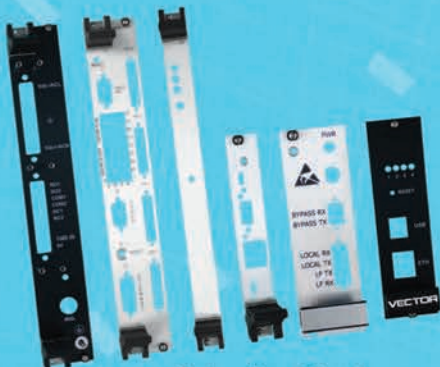
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Chassis and Rack Accessories



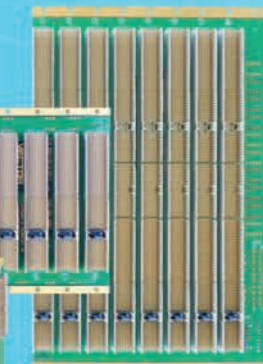
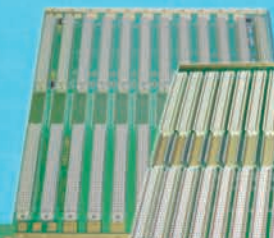
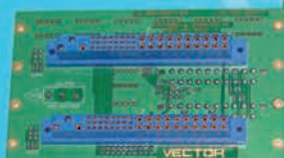
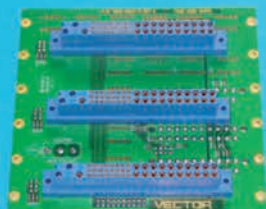
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devices, fully tested and certified.
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VECTOR Power Backplanes
PICMG 2.11 R1.0 Specification



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