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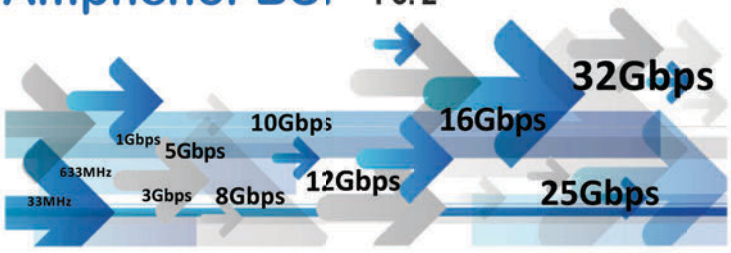

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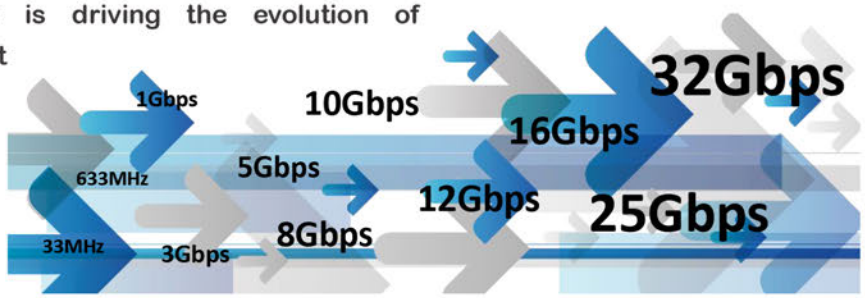

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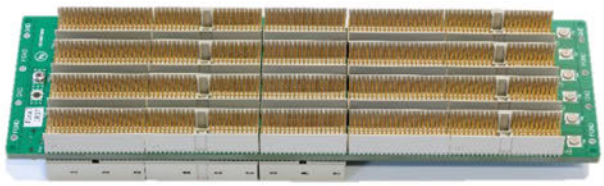

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FALL 2018

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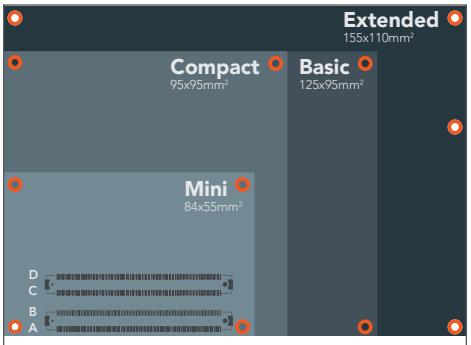

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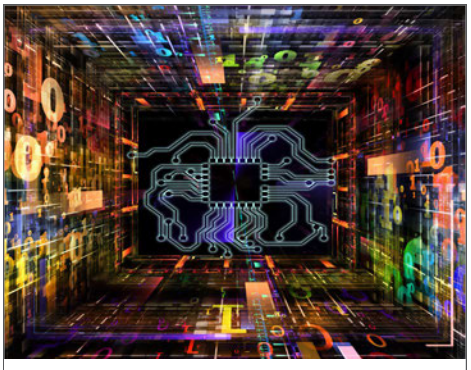

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On the cover

The PICMG Systems & Technology 2019 Application Guide covers PICMG standards and their role in growing the COM market, the IIoT, the sensors domain, and MicroTCA.

The Application Guide also highlights some of the industry's top products, in the categories of COM Express, CompactPCI, MicroTCA, and OSs and tools, especially in the military/aerospace and test/measurement arenas.

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Collaboration enables innovation

By Jessica Isquith, President of PICMG

jess@picmg.org

"In the long history of humankind (and animal kind, too) those who learned to collaborate and improvise most effectively have prevailed." – Charles Darwin

PICMG has begun several exciting new initiatives during the past year, within an atmosphere of strong collaboration that will only help in the success of each. The rapid adoption of industrial IoT (IIoT) and growing requirements in the Computer on Module (COM) market have led to the formation of multiple new committees, groups, and alliances within PICMG and the industry at large – collaboration in action.

This issue contains four contributed articles with key market and technical updates on many of our key initiatives. First, I provide an overview (page 8) of the COM market, the PICMG family of specifications (including an introduction to two new initiatives), and a status update on our IIoT programs. Often, while reviewing reports and articles in preparation for presentations, reports, and meetings, I try to find contradictions among the many publications. In the past few years, however, I've found two areas of undeniable growth with no studies to the contrary: the COMs market and the IIoT market.

Doug Sandy, PICMG CTO, has been leading IIoT initiatives related to the sensor domain, which until now has suffered from a lack of standardization. His latest article addresses the challenges we expect to face developing two new open specifications to facilitate the deployment of IIoT. These challenges include security, data modeling, synchronization, and required memory footprint. You can find his article, "Tackling the challenges of industrial IoT" in this issue on page 20.

Christian Eder of congatec is the chairperson of the new PICMG COM initiative. In his article, "COM Express is heading towards 'server-on-module'" (read it on page 12), he provides an in-depth explanation of COM Express Rev. 3, which was ratified in mid-2017.

IN THE PAST FEW YEARS, HOWEVER, I'VE FOUND TWO AREAS OF UNDENIABLE GROWTH WITH NO STUDIES TO THE CONTRARY: THE COMS MARKET AND THE IIOT MARKET.

The High-Speed MicroTCA committee has made a number of breakthroughs towards establishing a 40G specification. Justin Moll is leading these efforts and provides a detailed update on MicroTCA applications and future innovations on page 16. He reports that this phase of work is expected to be completed and prepared for review within the next two quarters. In December, DESY will be hosting the seventh annual MicroTCA workshop for Industry and Research in Hamburg. For more information please email us at info@picmg.org.

University outreach

In 2019 we plan to launch a university outreach program and an academic membership level. As PICMG enters its 26th year, we want to support and encourage young engineers' interest in embedded computing and facilitate their understanding of the value of Open Standards. Many of our members already have active alliances and programs with universities. Our goal is to help the next generation of engineers get involved with PICMG standards so that they will be prepared to specify them upon their entry into industry. Excellent examples of successful university/industry relationships include Extreme Engineering, NEXCOM, and SECO.

Show presence in 2018 and 2019

For the first time in several years, PICMG sponsored three key industry events in 2018. First up was Embedded Tech Trends, where we launched our IIoT initiatives. At embedded world, we showcased over 20 members' products, while more than 40 PICMG members exhibited at the largest annual embedded computing event in the world. We also exhibited at the Sensors Expo, where Doug Sandy presented an update of our IIoT initiatives along with a CNC-based proof of concept. This major sensors event will be expanded next year to include an Embedded Pavilion. We will have a presence at each of these events in 2019 as well, so please contact us if you would like to attend and/or actively participate.

PICMG is growing!

As with all organizations, some members leave and new ones join. I am pleased to share that we have gained more than a dozen new members in the past two years! In 2018 we welcomed TQ-Systems GmbH, Honeywell Inc., Core Source Technologies, Dynetics, Inc., North Atlantic Industries, and Vectology, Inc.

We have also witnessed the introduction of hundreds of new products based upon PICMG standards and encourage all members to present their products on our website. I hope you enjoy this application guide. Please do not hesitate to contact me regarding any PICMG initiatives or specifications at jess@picmg.org.

Bringing IoT to the sensor domain: Sensors Expo recap

By Justin Moll, Vice President of Marketing at PICMG

justin@picmg.org

Sensors Expo was held in San Jose from June 26 to 28, 2018. It was great to see a trade show with growing attendance and enthusiasm. Regardless of the type of sensor vendor on display, the trend to connect sensor technologies was widespread. Featured were wireless innovations, an embedded system area, a university showcase, and even clever end solutions such as the sensor-laden mattress, which we all admired longingly after being on our feet all day.

From an embedded computing perspective, there seemed to be two pressing needs in the sensors market: First, a way to connect legacy sensors so that they can be used in modern and future systems. Second, for those IP-enabled sensors that are "connected," the question becomes how they will interoperate with devices from other vendors. Of course there are a wealth of great proprietary, closed sensor solutions. However, they would face serious challenges in connecting with other devices on the factory floor or other IIoT [industrial Internet of Things] applications. This is where PICMG's new IIoT specification concept comes in.

The PICMG approach is to create a metadata model – a master schema, if you will – of all types of individual companies' data models to work with other devices. This metadata model will allow all types of sensors – those that measure pressure, temperature, color, proximity, etc. – to interface in a well-known language of the IT room. The models will also include multipoint sensors, controllers, and some specialty function devices. PICMG has a working agreement with DMTF [the Distributed Management Task Force, an industry-standards organization] and will use its Redfish API.

PICMG had a proof-of-concept demo at the Expo showing a basic machine with three 8-bit servo controllers that adjusted the machine's X, Y, and Z axes. Each controller used the PICMG data model providing basic PUT and GET commands based upon RESTful interfaces. By showing an IIoT implementation over an established and well-known IT format, visitors were able to imagine a connected approach using their own product/solution. Sensor companies understood that it was advantageous for them to be an active participant to ensure their schema approach is incorporated into the PICMG metadata model.

IIoT sensors present themselves as intelligent, managed devices over the factory network using the common metadata model. Using RESTful application programming interfaces, sensors may be monitored and controlled using standard IT methodologies. For sensors and actuators that must respond in real time, it may be necessary to place a controller close to devices in order to monitor the devices locally. This arrangement reduces the latency and improves determinism over having the devices remotely controlled through the factory control center. These local IIoT controllers would present the connected sensor data models to the upstream control center. They would also introduce programmable "listener" functions that implement local policies when sensor events occur. The listener functions may also be directly implemented in sensors and actuators.

Legacy sensors can be addressed as well with connections to the IIoT control center. Initially, programmable logic controllers (PLCs) can be connected over their existing interfaces and be managed through legacy software. As an intermediate step to full IIoT functionality, the PLC can later be replaced by an IIoT control gateway. This device "translates" the sensor's native protocols to a RESTful data interface using the common metadata model. This approach allows the same sensors to be used while the control architecture is migrated to IIoT technologies.

PICMG is planning a specification for a small (postage-stamp-sized) interface so that legacy sensors can be connected and interface with other IIoT devices. At a later stage, the older sensors can be replaced with fully IIoT-enabled sensors.

PICMG is known in the industrial automation world mainly for hardware specifications such as cPCI Serial, COM Express, and CompactPCI. However, the specification development organization is also well versed in software/firmware. For the TCA [Telecom Computing Architecture] designs, PICMG developed the Hardware Platform Management spec that enabled system performance monitoring, predictive maintenance, software upgrades in live systems, event logging, and more. Leveraging its expertise in software/firmware specifications – combined with the vast implementation of PICMG-based hardware from its member companies – PICMG believes that it is in a strong position for a true plug-and-play IIoT specification.

If you are interested in participating in the IIoT Advisory Board and/or becoming a member, contact PICMG at info@picmg.org for more details. A white paper on the PICMG IIoT vision is posted on www.picmg.org.

***Justin Moll** is vice president of marketing for PICMG.*

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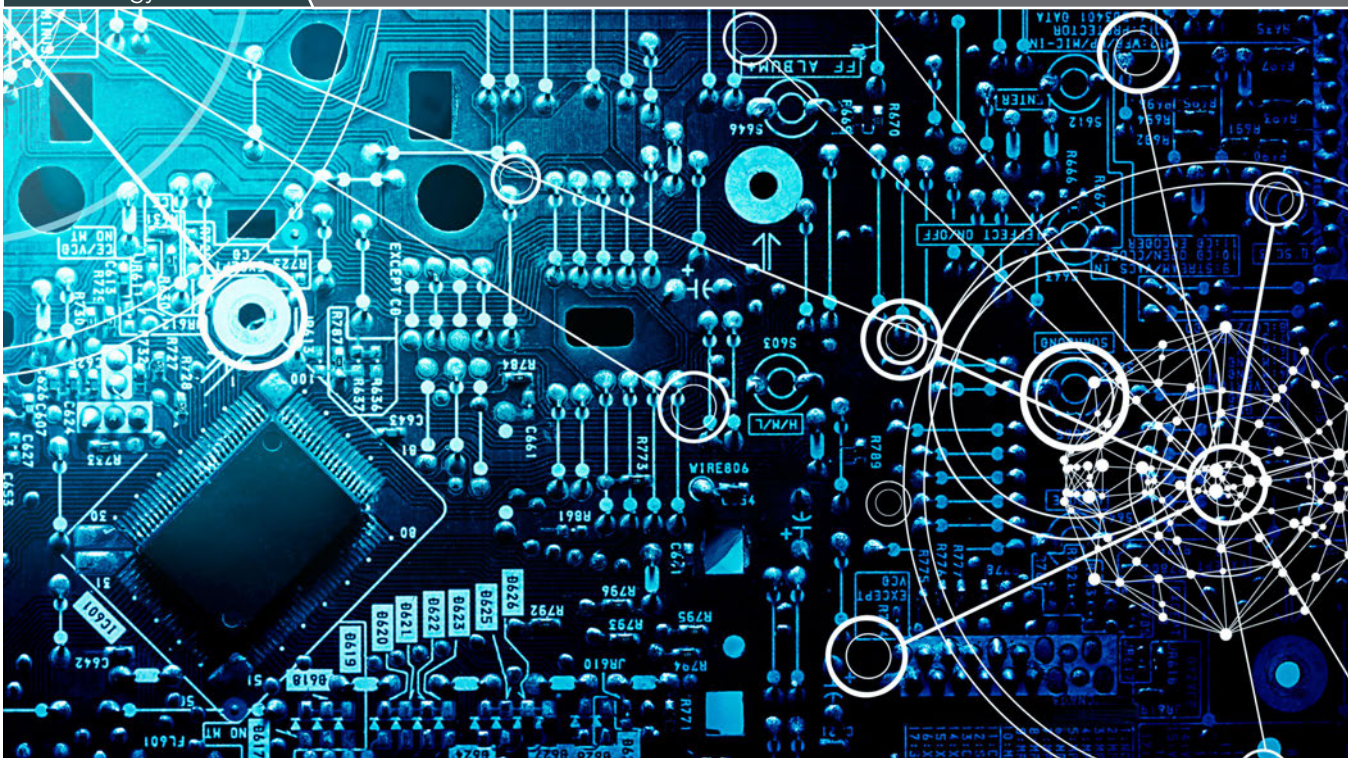

COM and IIoT market growth aligns with PICMG initiatives

By Jessica Isquith, President of PICMG

The Computer on Module (COM) market is expected to grow significantly over the next five-plus years, according to multiple market research studies. Within the COM market, COM Express is the recognized leader, with its strongest areas of growth being IIoT [industrial Internet of Things] and adoption in rugged environments, including drones, military, and transportation.

Several recent studies show that the largest area of IIoT investment and growth has been in smart factories.[1,2] Research in this area reveals that two of the major factors impeding rapid adoption of IIoT are a lack of standardization and a large legacy install base. This is particularly true of the sensor domain, which is currently made up of a combination of legacy and smart or IT-enabled sensors and actuators.

The McKinsey study states that the smart sensor market will reach over a trillion dollars: "… one of the largest sources of value from the adoption of the Internet of Things, potentially generating an economic impact of $1.2 trillion to $3.7 trillion per year. In the factories setting, value from the Internet of Things would arise chiefly from productivity improvements, including 10 to 20 percent energy savings and a 10 to 25 percent potential improvement in labor efficiency." (McKinsey, 2015.)[2]

Other studies support this growth: "We believe the Internet of Things opportunity for Industrials could amount to $2 trillion by 2020. The Internet of Things has the potential to impact everything from new product opportunities, to shop floor optimization, to factory worker efficiency gains that will power top-line and bottom-line gains." (Goldman Sachs[3])

PICMG IIoT strategy

With the lack of standards within the sensor domain, many companies and organizations are working together to provide solutions. Based upon our strong history and member companies' wealth of experience in industrial automation, system architecture, and cross-industry collaboration, PICMG has set forth a multiprong IIoT strategy.

At the heart of each initiative is the enabling of plug-and-play at the "last foot" of IIoT implementations. The concept of the last foot is analogous to the issues faced by the telecommunications industry in delivering services to the "last mile," which refers to

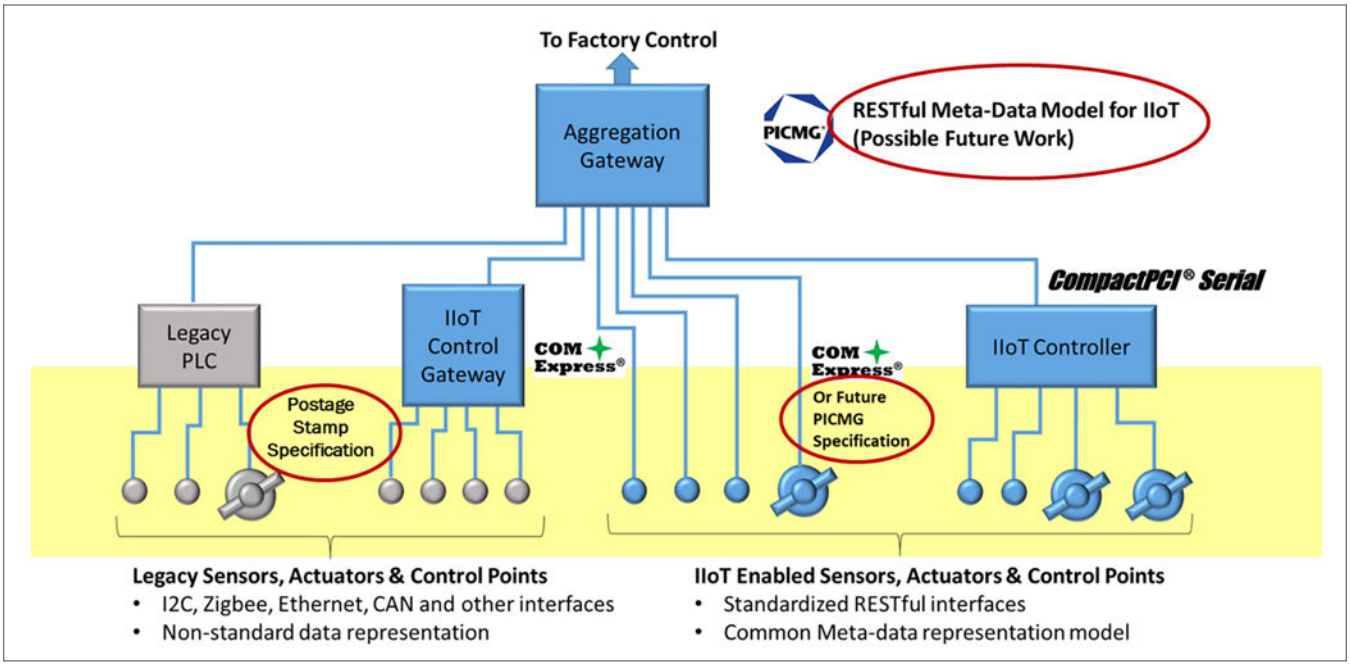

Figure 1 | Possible metadata model for IIoT sensors.

the portion of the telecommunications network chain that physically reaches the end users' premises. In the case of IIoT, the last foot is the sensor domain.

Core elements of PICMG's IIoT sensor domain strategy include:

- Postage-stamp form factor to convert of legacy sensors into smart sensors
- Network architecture and data models for the sensor domain
- IIoT developer kits

Over the past year, PICMG has taken many steps toward its vision of bringing standardization to that last foot. We established an Industry Advisory Board (IAB) – under the leadership of PICMG CTO Doug Sandy – that combines existing members (including new participants from member companies), outside experts, sensor manufacturers, and complementary associations, all to enhance the IIoT industry expertise.

In May, PICMG formed a partnership with the Distributed Management Task Force (DMTF), another industry-standards organization, to collaborate on IIoT efforts.[4] The DMTF creates open manageability standards spanning a range of emerging and traditional IT infrastructures, including cloud, virtualization, network, servers, and storage. Redfish is an open industry standard that specifies a RESTful interface based on the Open Data Protocol (OData) which uses HTTPS and JSON to transfer data. (Figure 1.)

The alliance between our organizations will help ensure the groups' standards are coordinated and aligned in the IIoT domain. It will advance collaboration between the two groups as PICMG specifies Redfish Application Programming Interface (API) resources to create a critical component of a new architecture and data model for the sensor domain. The work product from this partnership will include creating and maintaining Redfish extensions to support IIoT system deployments.

Our partnership signifies a key step in realizing a new IIoT infrastructure that addresses the sensor domain (smart and "not smart" sensors and actuators). To realize this goal, many technical challenges must be tackled, including security, data modeling, synchronization, and required memory footprint.

COM market surging

The COM market is also growing rapidly, which bodes well for PICMG technology. Market-research firm IHS forecasts an 8.6 percent combined annual growth rate (CAGR) for the COM Express market during the period 2015 to 2020, an impressive gain. Market-leading technologies are usually those that are well-established, and market volume tends to be stable rather than dynamic. Similar studies from Research and Markets paint even healthier growth prospects for COM Express, forecasting that the global COM market will grow at a CAGR of 17.97 percent during the period 2016 to 2020. Technavio's market study estimates that the global COM market stood at $543.98 million in 2017, with COM Express at more than 50 percent of the market. According to Technavio, it will increase to $818.25 million in 2022, growing at a CAGR of 8.51 percent during the period 2017 to 2022.[5]

This tremendous growth in the COMs market aligns well with current PICMG COM Express specifications as well as for two new initiatives that are underway. The first new initiative is an extension of COM Express (COM.0) for harsh environments, while the second is a new generation of COM Open Specifications.

COM Express has become ubiquitous in embedded applications and the most recognized PICMG standard. At recent events, from embedded world in Nuremberg to Computex in Taiwan, hundreds of COM Express products were on display. Though we are not privy to all available products, PICMG has distributed the specification to hundreds of manufacturers since its first release in 2005.

The COM Express standard – or family of standards, as it is sometimes described – is more than a dozen years old. (Figure 2.) It has emerged and endured as the most widely used small form factor for thousands of applications worldwide. The standard defines a family of COM single-board computers appropriate for a wide range of commercial and military/aerospace applications. The first two revisions of the standard were designed to accommodate modern high-performance chipsets and serial signaling protocols, including PCI Express Gen 3, SATA, USB 3.0, and high-resolution video interfaces. It is entirely open, with anyone permitted to build COM Express products without licenses or royalties.

COM Express = versatile

The ability to plug a COM Express module onto a carrier board reduces the time and cost to develop a product, as the user does not need to understand the often-complex details associated with high-speed signaling or the latest chipsets. The mezzanine capability is enabled by two standardized connectors mounted on the bottom of the board that can plug onto a board below it. All versions have these two connectors, although there are slight variations in pin assignment depending on the version. This layout means that the customer's product lifetime is lengthened, as newer COM Express modules can simply be plugged onto the carrier board, as they become available, to improve performance or lower cost.

Target applications often need to strike a careful balance between cost and performance, which leads to a variety of COM Express form factors and board sizes being defined in the standard. All of this flexibility is not without its challenges, however. Interfaces continue to evolve, especially video interfaces, as GPU and CPU chipset manufacturers change them or update them frequently.

COM Express Revision 2.0 Embedded Application Programming Interface (EAPI)

For the introduction of Revision 2.0 of the COM Express specification, PICMG developed a corresponding API. The EAPI specifies functions for industrial applications, which do not employ a common programming interface. In the past, the use of special features – such as a watchdog timer – required vendor-dependent software programming. This situation limited the free exchangeability of modules between different module vendors. With the release of the EAPI, this limitation has been removed.

The EAPI describes a common API to unify the software control for system information, watchdog timer, I^2C bus, flat-panel brightness control, and user storage area.

COM Express Revision 3.0

Revision 3.0 of COM Express – ratified in 2017 – provides for a new Type 7 connector and the addition of as many as four 10 Gigabit Ethernet (10 GbE) interfaces on the board. Previous revisions of the specification had been limited to a single Gigabit Ethernet interface. The higher-speed ports provide compatibility with new markets, such as data centers, where the high compute density of COM Express can result in increased rack utilization. The 10 GbE ports are also ideal for high-bandwidth video applications such as surveillance. The specification also increased the number of PCI Express lanes to 32 across the Type 7 connector, an improvement that brings a wealth of connectivity and interface options, including the support for GPGPUs.

The COM Express standard's new Type 7 pinout does away with all graphics support and replaces it with as many as four 10 GbE ports and an additional eight PCI Express (PCIe) ports, bringing the total PCIe support to as many as 32 PCIe lanes. The Type 7 pinout has been specifically tailored to leverage all the functions of low-power, headless server-grade systems-on-chip (SoCs). A Network Controller Sideband Interface (NC-SI) bus is also supported, enabling Intelligent Platform Management Interface (IPMI) Board Management Controller (BMC) support on the carrier board.

New PICMG COM specification kicks off

Earlier this year, PICMG launched another project: A new COM specification is under development that will be a parallel effort to existing COM Express efforts. The subcommittee will develop a next-generation COM standard and an accompanying Carrier Design Guide. This standard is intended to coexist with the existing standard, rather than as a replacement for COM.0. The new specification is expected to support two different module sizes – one for high-performance computing and the other for embedded computing. Initial plans include incorporating a new high-speed connector

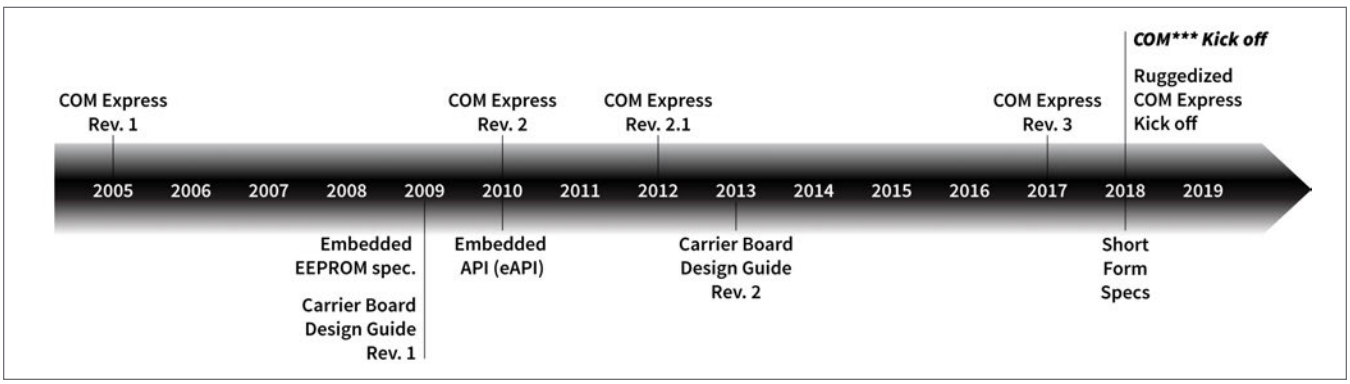

Figure 2 | COM roadmap and overview of current offerings.

able to support existing and future interfaces such as PCI Express Gen 4/5 and as fast as 100 Gb Ethernet. The specification will target medium- to high-performance server-class processors.

In all, 18 of PICMG's member companies have joined the group, which is being sponsored by Congatec, ADLINK, and Kontron.

Rugged COM Express shifts over to PICMG

Rugged COM Express began as an initiative within the VITA organization as an adjunct to the COM.0 PICMG specification. In the summer of 2018, VITA and PICMG agreed to transfer Rugged COM Express into the PICMG organization in order to complete the specification. PICMG and VITA have a rich history of successful collaboration as both organizations work together to meet industry needs. A key example of this is our Hardware Platform Management (HPM) specification.

The specification will define a ruggedized version of PICMG COM.0 for harsh and mission-critical environments. The goal of the specification is to describe a 100 percent mechanical-compatible housing around a COM Express module. The team is finalizing a solid aluminum-frame design that protects the electronics against environmental influences such as moisture, dust, vibration or EMC radiation, and operates in the extended temperature range of -40 °C to + 85 °C. Conductive cooling and a metal housing will be integral parts of the specification and serve as a clear differentiator to existing COM specifications. The committee will determine which COM Express versions will be supported.

This effort is sponsored by MEN Micro, nVENT, and Elma.

The need for open specifications to enable successful hybrid solutions, migration paths, and hardware/software interoperability are at the heart of PICMG's strategy; the drive for these solutions aligns with our nearly 25 years of success in providing answers to similar industry needs.

Looking ahead

PICMG will continue to work on resolving obstacles to enable successful IIoT implementation through the development of open specifications. Our COM family of specifications will continue to evolve to meet processor, I/O, environmental, and market-specific needs. To further aid adoption of COM Express, we developed short-form specs that are available for free. All PICMG associate and executive members are welcome to participate in the IIoT initiatives and COM subcommittees. For more information, please contact us at info@picmg.org. We look forward to hearing from you.

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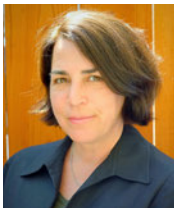

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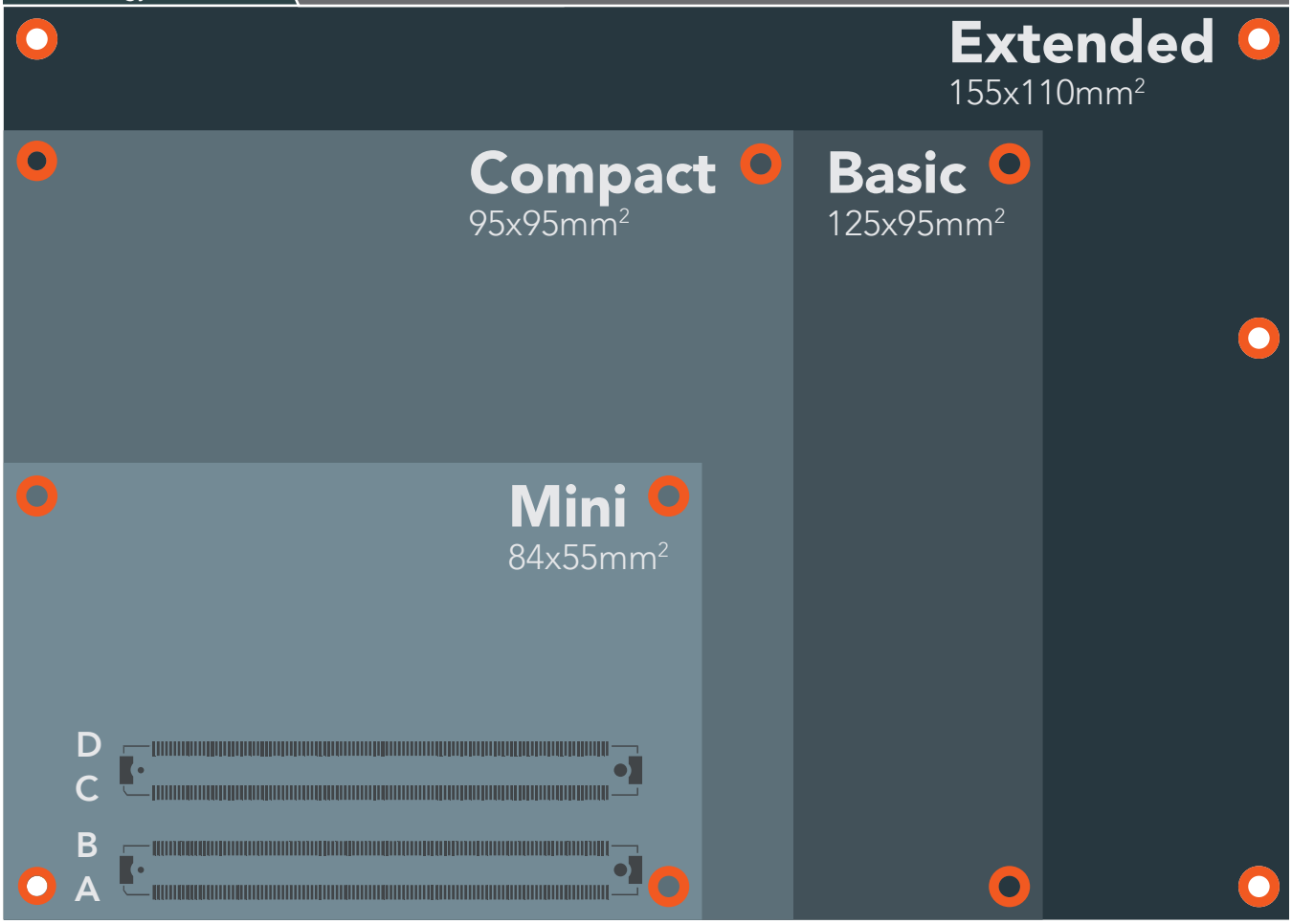

COM Express is heading towards "server-on-module"

By Christian Eder

With the newly revised (Version 3.0) iteration of the most successful computer-on-module (COM) standard, a new pinout type is added to extend the reach of COM Express to server type applications.

COM Express – a computer-on-module standard defined by the PICMG consortium (www.picmg.org) – saw the first version released in 2005, with updates in 2010 and 2012. The upcoming Revision 3.0 for the COM Express standard defines four different sizes and three pinouts.

The new Type 7, while not a replacement for the well-established Type 6 pinout, trades all audio and video interfaces for four 10G Ethernet ports and a total of 32 PCI Express lanes. These changes were applied in order to support enhanced micro servers and other server type applications that only allow for low power consumption but require high computing performance and communication throughput.

COM Express pinouts

The PICMG specification defines different pinout types in order to fulfill application-specific demands. The pinout Types 1, 3, 4, and 5 are considered to be "legacy" and are no longer used for new designs. Products featuring older pinout types are still available and refer to the revision 2.1 of the COM Express specification. (Table 1.) The Mini size was introduced with Rev. 2.1 and is only implemented for the single-connector pinout Type 10. The most popular pinout today is Type 6, which replaced the legacy Type 2 computing modules.

The Extended size definition of 110 x 155 mm² did not become relevant in the market in the past. With the new, server-oriented pinout Type 7 defined in the COM Express specification Rev. 3.0, this size might actually come into play as server type applications require more DRAM capacity and more robust CPU performance levels. COM Express supports a maximum of 137 W power consumption; the larger size adds real estate for more memory and allows for better heat transmission to support higher power consumption.

When comparing the new Type 7 pinout to the Type 6 pinout, it becomes clear that Type 7 is not a replacement for 6: Instead, it's a definition that clearly

Type	Rows	PCIe	SATA	LAN 1G/10G	USB 2.0/3.0	Display
10	AB	4	2	1/-	8/2	LVDS/eDP, DDI
6	AB/CD	24	4	1/-	8/4	VGA, LVDS, PEG, 3x DDI
7	AB/CD	32	2	1/4	4/4	

Table 1 | The PICMG specification defines different pinout types in order to fulfill application-specific demands.

targets headless server applications with low power consumption, high computing density and high I/O throughput. The new Type 7 definition removes all audio and video interfaces, the upper four USB 2.0, ExpressCard, and the upper two SATA ports, a move that releases 60 pins on the AB connector and another 42 pins on the CD connector. These 102 newly released pins, in combination with some previously reserved pins, have been used to add extra PCI Express lanes and four 10 GB Ethernet KR lanes with a complete set of NC-SI sideband signals.

At a maximum, Type 7 COM Express modules can provide a host of features:

- 4 x 10GBaseKR Ethernet with NC-SI
- 1 x 1GB Ethernet
- 32 x PCI Express 3.0 lanes
- 2 x SATA
- 8 x GPIO shared with SDIO
- 2 x serial shared with CAN
- LPC bus shared with eSPI
- SPI and I²C bus

10 GBit Ethernet

On top of the existing 1 GB Ethernet, COM Express Type 7 pinout defines up to four 10GBASE-KR ports with a maximum theoretical data performance of 10 GBit/s. 10GBASE-KR defines single backplane lanes (see IEEE 802.3/49) in order to avoid being tied to predefined physical interfaces.

The PHY that defines the physical transmission layer is not on the module but instead needs to be implemented on the carrier board. The carrier board implementation finally decides if the data is transmitted via copper or fiber cables. For even more flexibility, this might be implemented as exchangeable SFP+ modules [small-form-factor-pluggable].

It's also possible to combine the performance of multiple 10 GBit Ethernet signals: Four lanes of 10GBASE-KR can be bundled into one PHY for 40GBASE-KR4.

THE NEW TYPE 7, WHILE NOT A REPLACEMENT FOR THE WELL-ESTABLISHED TYPE 6 PINOUT, TRADES ALL AUDIO AND VIDEO INTERFACES FOR FOUR 10G ETHERNET PORTS AND A TOTAL OF 32 PCI EXPRESS LANES.

The feature set of the COM Express 10GBASE-KR interfaces also includes a software-defined pin for each of the four interfaces. This physical pin can be configured as input or output and is controlled by the corresponding Ethernet controller. A typical application for this is the implementation of a hardware-based precision timing protocol for enhanced real-time applications.

NC-SI Ethernet sideband signals

The network controller sideband interface (NC-SI) defines the protocol and electrical interface for connecting a baseboard management controller (BMC), which is used to enable out-of-band remote manageability. This interface was defined by DMTF (Distributed Management Task Force, Inc., see http://www.dmtf.org) and is fully implemented for COM Express Type 7 modules.

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NC-SI defines the connection between the network controller and the out-of-band management controller, which can be implemented on the carrier board. It supports the communication between the management controller and external management applications.

NCSI signals

- NCSI_CLK_IN : Clock Reference
- NCSI_RXD[0:1] : Receive Data (Network Controller to Baseboard Management Controller)
- NCSI_TXD[0:1] : Transmit Data (Baseboard Management Controller to Network Controller)
- NCSI_CRS_DV : Carrier Sense/Receive Data Valid to Network Controller
- NCSI_TX_EN : Transmit Enable
- NCSI_RX_ER : Receive Error
- NCSI_ARB_IN : Network Controller Hardware Arbitration Input
- NCSI_ARB_OUT : Network Controller Hardware Arbitration Output

Mass storage interface

The removal of two SATA ports looks confusing at first glance, since server applications are always hungry for a large amount of mass storage; however, current technology trends clearly show that SATA hard drives are being replaced by fast solid-state disks (SSDs). Since SSDs are much faster, the SATA interfaces therefore become a performance bottleneck and are being replaced by NVMe (NVM Express/Non-Volatile Memory Host Controller Interface Specification – NVMHCI, see www.nvmexpress.org), which uses the PCI Express interface for mass storage devices. That's clearly supported by Type 7, with the increased amount of PCIe lanes. (Table 2.)

Benefits of NVMe when compared to SATA

NVMe is the optimized PCI Express SSD Interface. This logical device interface has been defined from the ground up in order to take advantage of the low latency and the parallel internal structures of flash-based storage devices. The goal of NVMe is to release the full performance advantages of PCIe-based SSDs and standardize the PCIe interface for fast SSDs. The NVMe specification defines an optimized register interface, command set, and feature set for PCI Express-based SSDs. NVMe reduces the I/O overhead and brings various performance improvements including multiple long command queues, improved interrupt processing, and reduced latency.

For classical server applications, NVMe mass storage devices are available as standard-sized PCI Express expansion cards. For mobile and embedded applications, the M.2 form factor with up to four PCIe lanes is typically used.

Upcoming NVM technologies

Intel has already announced its intention to release Optane SSD products based on its brand-new 3D Xpoint technology, which was announced in 2016. This is a new technology based on phase change technology and promises to boost performance and endurance by 1,000 times compared to NAND flash technology. Based on the 3D stacking of the cells, the density of 3D Xpoint will be an improvement of 10 times over DRAM technology.

The promised performance and endurance of this new technology will be constrained by SATA, however; NVMe leaves much more headroom to gain the expected maximum performance levels.

Heat management and power consumption

The high density of computing performance required for data-center applications correlates directly with the power consumption. The direct impact: The energy cost that is not expected to decrease in the future. It's not just the computers power consumption, it's also the energy required to provide cooling, which goes into the total operating cost. The lower the computer´s power consumption, the lower the cost of cooling it down. Efficient cooling also increases the reliability and lifespan of the silicon. With the "turbo boost" features of current processors, a good cooling concept also allows for extra computing performance. Turbo boost allows overclocking the processors as long as they are kept cool enough.

In order to be highly thermally efficient, most COM Express products are equipped with embedded technologies borrowed from mobile and low-power applications. The COM Express specification defines a heat spreader as a thermal interface to the system housing. This flat surface easily integrates into server applications and allows for a quick technology upgrade without having to change the mechanical and/or electrical system architecture. Following the ever-changing roadmaps of the chip vendors is no longer a challenge.

The COM Express specification also defines an I²C bus that allows the connection of environmental sensors in order to connect multiple temperature sensors for enhanced system monitoring.

Interface	SATA3	PCIe 2.0		PCIe 3.0		PCIe 4.0	
Lanes		x2	x4	x2	x4	x2	x4
Max performance per direction	6 Gbit/sec	10 Gbit/sec	20 Gbit/sec	16 Gbit/sec	32 Gbit/sec	32 Gbit/sec	64 Gbit/sec

Table 2 | Performance comparison of SATA and PCI Express

Usable for Open Compute Project?
Some of the largest data center operators, i.e. Facebook and Google, are driving the Open Compute Project (http://www.opencompute.org) to make their server platforms more efficient, flexible, and scalable. This is one of many areas where COM Express might use its server-on-module capabilities to enhance telecom and data center applications.

Compatibility to Type 6 pinout
For headless applications it might be possible to use a Type 7 module with a Type 6 carrier board; such a combination will work if certain interfaces are not used by the carrier board.

Omitted interfaces
- SATA[2:3]
- AC97 / HDA Audio
- USB[4:7]
- EXCD[0:1]
- eDP / LVDS
- VGA
- DDI[0:2]

Going forward
COM Express is the most successful computer-on-module standard ever, but it's not the best at supporting the fast-growing area of edge computing servers. In this arena we find some requirements from the "classic" server markets combined with industrial requirements. It's clear that server processor technologies for low-power applications supporting a massive amount of interfaces (i.e., PCI Express Gen 4 or Gen 5, 100 GBit Ethernet, etc.) will need to become available within the next few years.

COM-HD (the name is not yet fixed; it might be changed by the PICMG workgroup) is the forward-looking next generation of COMs. It's the next standard on the COM roadmap, which started way back in 1999 with ETX, followed in 2005 by COM Express, and is about to be extended by COM-HD to ensure state-of-the-art computing modules for at least the next 10 years.

The task of PICMG's COM-HD workgroup is to define a standard that supports fifth-generation PCIe and 100 GB Ethernet while doubling the amount of interfaces. The max I/O performance of COM-HD will be about eight times that of the current COM Express Type 7, with 64 instead of 32 PCIe lanes, or four times throughput when comparing PCIe Gen 3 to Gen 5.

COM-HD will not replace COM Express. Instead, it will offer more choices for high-end edge computing.

Christian Eder *is director of marketing for congatec AG. He has been an active participant in the COM Express workgroups as the specification editor for COM Express 2.0, COM Express 2.1, COM Express Design Guide 2.0, Embedded EEPROM, Embedded EAPI, and now the COM Express 3.0 workgroup.*

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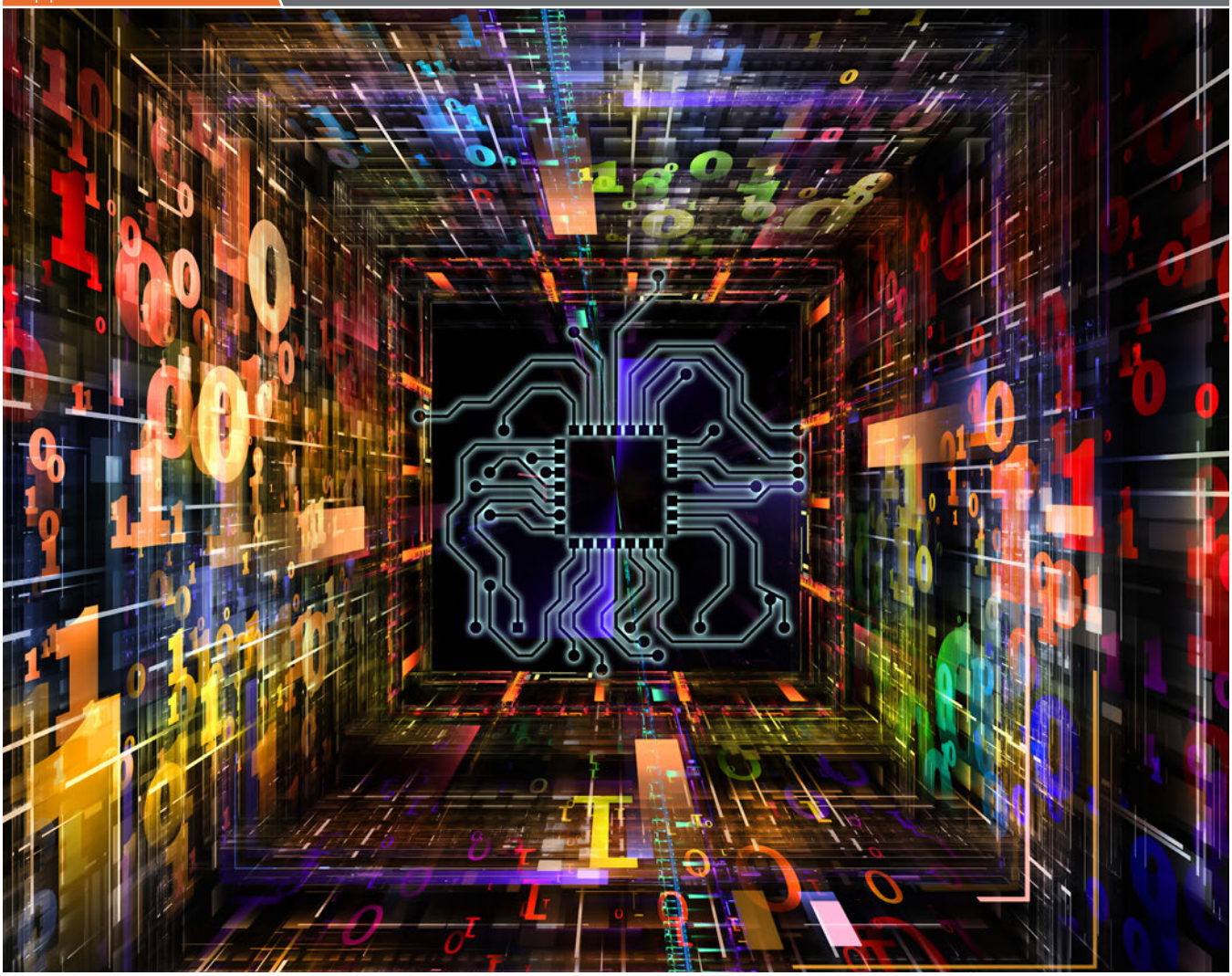

Military, aerospace, and physics applications drive new MicroTCA innovations

By Justin Moll

MicroTCA is a highly versatile backplane-based architecture that is utilized in a wide variety of applications. With a high-speed connector, compact size, hot-swappability, and 99.9999 percent achievable uptime, it's a powerful architecture. Particularly in military/aerospace and physics applications, end users are asking for solutions to make the architecture faster, handle more power, provide more I/O, and meet other demands of the environment. The MicroTCA/AMC vendors are stepping up to meet these requirements.

In the mil/aero market, there have been ruggedized solutions for MicroTCA for years. Although MicroTCA.2/.3 never gained mass adoption, vendors have been using best practices for rugged rackmount and air transport rack (ATR) designs. Handling more processing power is one of the common desires for the highest-end computing requirements. With the architecture's small size, MicroTCA at times has had limitations on using some of the powerful processors available in the market. However, new trends and innovations are changing the game. Organically, one of these issues continues to subside.

As processors become more compact and utilize less wattage, more options can be utilized in MicroTCA. In fact, there are several high-end AMCs that have been released recently (details are discussed below). The other game-changer is that vendors are utilizing more of the "tongues" of the connector to increase the power and I/O available. A typical AMC uses a single tongue with 21 pins that use about 4A each. By using a double-tongue, these pins can be used to power AMCs to over 160W theoretically, but more in the 110-120W range in practice. This opens up the AMCs to utilize processors such as the Intel

Xeon E5-2648L and FPGAs such as Xilinx's Virtex UltraScale XCVU190, with 1800 DSP slices. One example is VadaTech's AMC594 dual channel 8-bit ADC at 56 GSPS with the XCVU190 UltraScale FPGA and 16GB of 64-bit DDR4 memory. (Figure 1.)

One may wonder if this second tongue creates a custom, proprietary solution. It does not hamper interoperability; the use of the second tongue is allowed in the specification and the pitch between slots has enough space for it. Therefore, the backplane spacing is not affected. But, sometimes these solutions will be customized to squeeze out even more performance. For example, the AMC594 has a special high-speed connector in the Zone 3 (RTM) area that plugs into a proprietary second backplane.

These types of innovations are bringing in new design wins for MicroTCA. These include:

1. An unmanned airborne electronic warfare (EW) payload with a large U.S. defense prime, based on Xilinx Zynq UltraScale+ and Analog Devices AD9361. The customer started with standard commercial rackmount platforms for capability demonstrations and is now working with the vendor to create ruggedized deployable versions.
2. An avionics sensor system with a major U.S. aerospace company, initially using standard MTCA chassis and modules based on Xilinx RFSoC.

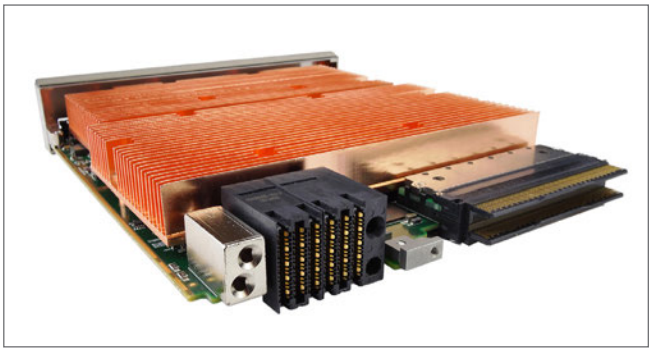

Figure 1 | A part of the MicroTCA.0 specification that is not well known is a second connector "tongue" of the AMC connector, which can be put to work to provide more power or I/O connectivity. (Photo courtesy of VadaTech.)

3. Naval countermeasures suite with a U.S. defense prime, using hardened MTCA (including ADC, DAC, and FPGA).
4. High-speed (56 Gsps) data-acquisition system capable of supporting up to four channels (I/Q, dual-modularity) for optical network development, with a European partner.

It's not just the military/aerospace market that is pushing performance; the physics labs are also driving new MicroTCA innovations.

High-energy physics

MicroTCA, particularly MicroTCA.4 for physics, is increasingly popular in various lab environments. While we often focus on the AMC boards, the chassis are also been designed to meet a wide range of application requirements. There are many chassis platforms for the double-module-sized AMC that are used in MicroTCA.4 for physics. They are typically 7U-9U tall and provide up to 12 AMCs with redundant MCH options.

However, sometimes the labs desire smaller enclosures with fewer slots. There are also several of these in the market, but the majority are side-to-side cooled. While efficient, this airflow path requires special cabinet arrangements to support the management of the cold intake and hot exhaust. nVent/Schroff developed a front-to-rear cooled version in a 3U size for the European Spallation Source (ESS) in Sweden. The chassis offers 6 AMC slots, 4 MicroRTMs, and an optional integrated JTAG switch module (JSM).

Ioxos has developed an IFC_1410 intelligent FMC carrier for MicroTCA.4 based on Kintex UltraScale and an IFC_1420 1.8 GHz 16-bit 10 channel ADC with 5 DAC channels to the RTM. They have also introduced an I/O and synchronization MicroRTM that interfaces with the FMC carrier. DESY [Deutsches Elektronen-Synchrotron, Hamburg] developed a new four-channel piezo driver to help labs have a general-purpose piezo actuator using high voltage and high current drive. It is used in high-energy physics applications for the synchronization and special diagnostics as well as the tuning of superconducting cavities. They have been successfully installed and commissioned at the European XFEL facility especially for master laser oscillator (MLO) synchronization, electro-optical bunch length diagnostics (EOD), or pump-probe experiments. [Note: DESY will have its annual MicroTCA Workshop December 5-6, 2018, at its newly completed MicroTCA Technology Lab.]

Other boards have been developed to upgrade the performance of existing MicroTCA/AMC systems. This group includes Concurrent's AM F5x/msd AMC based on an Intel Xeon E3-1500 v5 processor with PCIe Gen3 connectivity. Also available: An AM G6x/mds double module AMC with an optional MicroTCA.4 MicroTCA connector. It features a Xeon E3-1505M v6 processor and has direct attached storage capability. Pixus Technologies also upgraded its MicroTCA chassis to PCIe Gen3 and offers some configurations for 40GbE. Of course, there are many ongoing product upgrades in the industry for MicroTCA/AMC. (Figure 2.)

AMCs in AdvancedTCA

A fact that is often lost to those who are new to MicroTCA is that the AMCs were originally designed to be used inside carrier boards for AdvancedTCA designs. Although this design approach is not used as often, some AdvancedTCA applications would greatly benefit from the additional I/O, storage, and specialty board features of the AMCs. Alternatively, there are hybrid AdvancedTCA/AMC chassis that allow both types of boards to be plugged in a specialized chassis without requiring carriers.

Figure 2 | MicroTCA enclosures are being designed in various configurations to meet the market's evolving requirements. This 3U chassis (photo courtesy of nVent/Schroff) features a horizontal-mount configuration with front-to-rear cooling.

Next levels of performance

A current PICMG committee is getting closer to finalizing the specification for 40GbE MicroTCA/AMC systems. In short, the group has done detailed simulation studies proving even worst-case performance for 40GbE. The group recently has developed the specialty probe cards for testing the simulations using the full interconnect path of the hardware. When the final results are complete, the specification will be updated. Some members of this group plan to do a cursory review of PCIe Gen 4 speeds as well, although this is not the primary focus of the committee.

Achieving 100G speeds would almost certainly require a connector modification, but cursory review of simulation results suggest that short paths with very high-grade PCB material and backdrilling may be able to support small to medium-sized backplanes. As PICMG is member-driven and because to a large degree MicroTCA is customer-driven, the members, the labs, and the military/aerospace community would ideally drive next-generation efforts.

Versatile performer

MicroTCA and AMCs continue to hit new levels of performance with creative design solutions from PICMG member companies. The architecture remains a growing choice in the military/aerospace community with its SWaP advantages and vast array of options. Physics and a wealth of other applications – including banking, industrial, medical, test/measurement, communications, and more – continue to bring MicroTCA new applications and innovations. Particularly with creative use of underutilized perks of the specification, MicroTCA will continue to advance for many years to come.

Justin Moll *is vice president of marketing for PICMG.*

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Tackling the challenges of industrial IoT

By Doug Sandy

The Internet of Things (IoT) promises to transform the way that we deploy industrial applications by combining the best practices from the IT space with cloud-based analytics and machine learning.

New industrial IoT (IIoT) deployments will benefit from improved operational efficiencies due to the quantity and quality of the information available to optimize processes. Wider use of IT technologies such as common protocols and RESTful interfaces will also enable tighter integration between the various systems (e.g., factory floor, purchasing, and sales) and allow operators to tap into the large and growing pool of IT talent. New and emerging standards will control how all these technologies work together in harmony. With all these promising developments for IIoT, one critical area has remained relatively impervious to standardization: the sensor domain. Challenges such as security, synchronization, scaling, and lack of interoperability have in the past impeded progress. Now, however, with coordination between PICMG, the DMTF [Distributed Management Task Force], and other organizations, this situation is changing.

Plug-and-play architectures of the 1990s transformed our expectations of how new devices could be added to our computing systems. Prior to plug-and-play, adding a new peripheral device to a computer required manual configuration of the hardware and software. Now users expect that when a new device is plugged in, the computer will "automatically" detect the new hardware, configure it, and make it immediately available. This isn't automatic, of course, but rather a

well-defined process in which the software queries the hardware and the hardware reports its capabilities. However, adding new sensors and actuators in an industrial deployment still falls largely into the manual configuration category.

PICMG seeks to tackle the IIoT challenges and accelerate its deployment by providing two new open specifications. The first is an architecture and data model that leverages existing IT technologies and enables plug-and-play at the sensor domain, while the second is a postage stamp-sized form factor that allows existing sensors to be easily converted into "smart sensors" that play seamlessly within the larger IIoT-enabled facility. Read on to learn about some of the issues we expect to encounter, as well as some possible solutions. With the combined talent of our member companies, along with collaboration with other industry organizations, PICMG hopes to conquer the challenges and make these plans a reality in 2019.

Challenge #1: Security

The first challenge that we expect to encounter is that of network and data security. While security is important regardless of the application, it becomes even more critical when breaches of the network can potentially take over factory operations, stall transportation systems, or affect the stability of the power grid. Fortunately, there are some common-sense precautions and best practices that can already be applied.

First and foremost, security can be strengthened by applying the adage: If it doesn't need to be connected, don't connect it. Most of us realize that an internet-enabled thermostat or security camera in our home creates a potential target for hackers. After weighing the risks, we make an informed decision about whether or not the risks are offset by the convenience that Internet connectivity brings. For industrial applications, the calculus is different. Almost no amount of convenience could offset the potential risks associated with takeover of a "Smart Factory Control" application, for instance.

Industrial IoT deployments must firewall their mission-critical systems away from the outside world, allowing only monitoring (not control) through carefully secured access points. This "walled fortress" approach (Figure 1) is not unlike what telecommunications companies have successfully used for network management for years. Although the data network is open to all their customers for use, the management and control network is tightly secured. IIoT sensor specifications must provide appropriate security features for sensors living within the walled fortress environment of their facility.

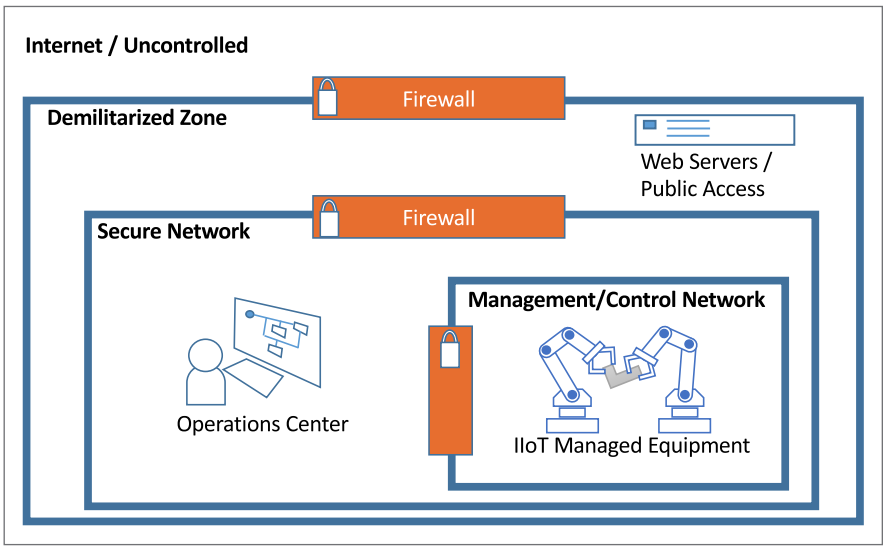


Figure 1 | Example implementation of the "walled fortress" security architecture for IIoT.

> INDUSTRIAL IOT DEPLOYMENTS MUST FIREWALL THEIR MISSION-CRITICAL SYSTEMS AWAY FROM THE OUTSIDE WORLD, ALLOWING ONLY MONITORING (NOT CONTROL) THROUGH CAREFULLY SECURED ACCESS POINTS.

At this point, you might be asking, "Is this even the Internet of Things, if the things are not connected to the internet?" This is a valid question and is probably technically true. Remember, though, that the business values associated with IIoT are largely centered around leveraging internet technology and the internet talent pool, not necessarily connecting an industrial application to the broader internet.

Challenge #2: Synchronization

The next challenge that we expect to face in standardizing sensor domain IIoT is that of synchronization. In other types of IoT, sensors work relatively autonomously from each other and the acceptable system response time to sensor events is often in the range of several seconds to many minutes. Neither is the case in industrial applications. Take, for example, a robotic arm that is responsible for welding: The motion of each joint must be carefully coordinated with the other joints in order to quickly and accurately accomplish its task. In practice, this means that the multiple motors must respond to the same stimulus (e.g., "start moving" command) within a very short and deterministic timeframe.

Three potential solutions exist for accomplishing this synchronization: sideband signals, network multicasting, and network time synchronization. The first and simplest

option connects all the devices that must be coordinated to another signal for the purpose of synchronization. This technique works well for situations where the devices are located in physical proximity to each other. The second, using UDP [user datagram protocol] multicast capabilities can eliminate some of the networking delays associated with multiple TCP/IP commands (one to each device) as it melds them into one command that is sent simultaneously to all the devices at once. The last option requires each sensor endpoint to maintain an accurate clock source, which they synchronize to a reference clock found on the network. When commands are sent to the sensor nodes, they can be coded to begin or end with respect to a specific network time. These possible solutions are shown in Figure 2. It is expected that IIoT specifications will support a variety of these options.

Challenge #3: Memory footprint

The third challenge associated with applying internet technologies to the sensor domain is the limited memory capacity of the microcontrollers that are otherwise ideal for this application. This problem stems from the fact that most higher-level internet management protocols are human-readable (think XML and JSON). While this is desirable for the people who develop and manage the IT infrastructure, the text-based approach is an extremely inefficient method for storing and conveying information. For instance, the 300+ words of this article's first two paragraphs would push the limits of data storage for most 8-bit microcontrollers.

While the first reaction to solve this problem might be to use a microcontroller that has more memory, this may adversely change the solution cost and make smart sensors cost-prohibitive. Augmenting the memory of an existing microcontroller using external devices such as flash memory may solve the problem but has similar drawbacks on cost.

An alternate solution (Figure 3) is to allow the sensor domain to transmit the data in a binary coded fashion. In this solution, data is stored and transmitted as a coded sequence of binary information, rather than human-readable text. This dramatically reduces the amount of memory required to store the sensor information and puts it well within reach of most 8-bit microcontrollers. The binary data is converted to human-readable text for use by the rest of the network. The translation occurs within an IoT gateway device and only works well if the data structures that are communicated at the sensor level closely match the human-readable version created by the gateway. Standardization in both of these domains is key.

Challenge #4: Data model

The final challenge to consider is that of the data model itself. This challenge is the most abstract and is probably new to those who are not familiar with IT management. Rather than dig into all the technical details, let's use a more familiar example: Computer plug-and-play.

When we plug a new piece of hardware into our computer, the computer software interrogates the new hardware to determine what it is and what its resource needs are. The hardware, in turn, responds with information that describes itself in a manner that the computer hardware understands. The information describing the hardware can be thought of as a "data model" – a description of the hardware, its needs, and capabilities.

In IT implementations, the data model also forms the interface by which the device behavior can be altered. By writing a modified data model (or portion thereof) back to the device, the device behavior is updated with the changes. For instance, a thermostat data model might contain a field that specifies the temperature setpoint at which the air-conditioning unit should turn on. Updating this field in the device's data would signal the thermostat to change the setpoint to the new value.

The real challenge with defining data models is providing flexibility to support today's and anticipated future devices without adding undue complexity. Since interoperability between vendors is essential, this activity can only happen within the context of a standards organization

Ongoing work

PICMG is moving forward with an aggressive schedule to advance IIoT. The PICMG approach encourages a firewalled, secure network architecture that supports a variety

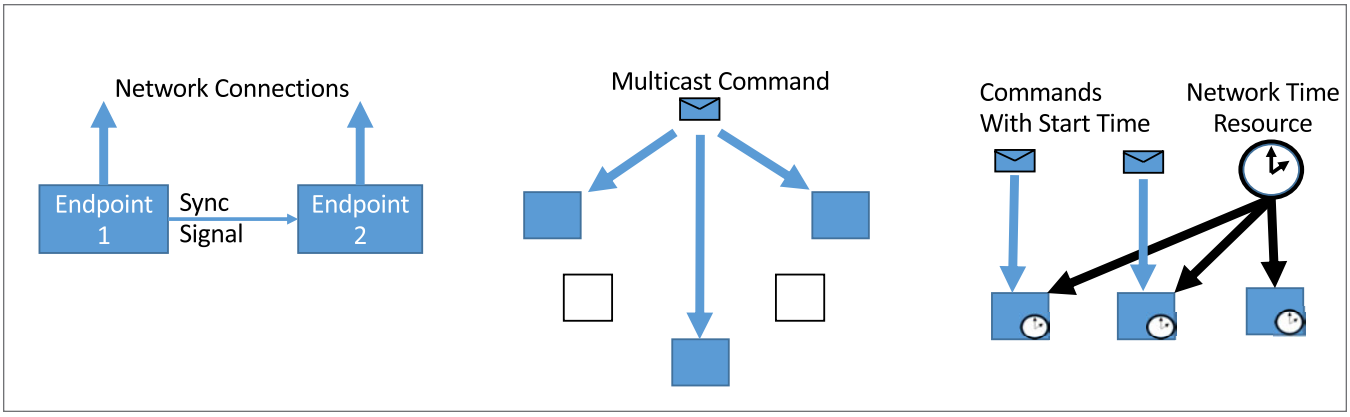


Figure 2 | Possible synchronization methods for IIoT.

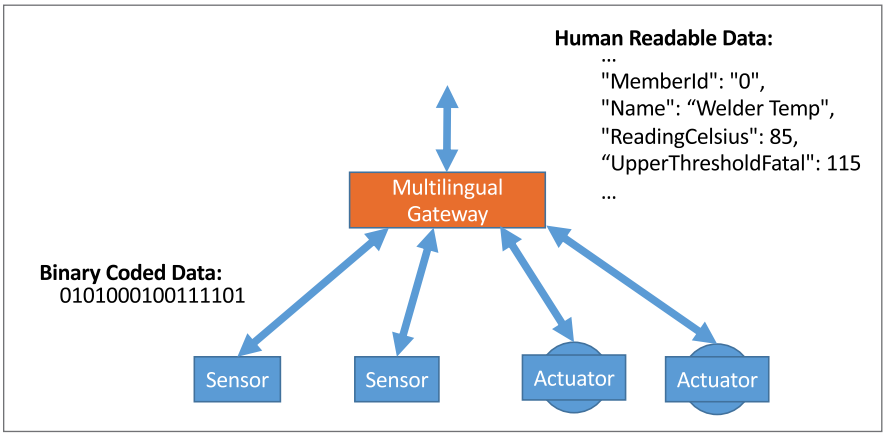
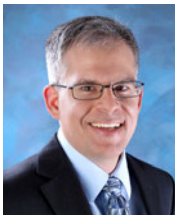


Figure 3 | Conversion of human-readable data representation to binary-coded representation.

of synchronization methods and a uniform data model that scales down to the sensor domain through binary encoding. Using well-established practices, the specifications will provide plug-and-play interoperability at the sensor domain to the "last foot" of the IIoT network. In March 2018, we formed an alliance with the DMTF in order to extend the Redfish management API to industrial applications. In June 2018 we demonstrated a proof-of-concept CNC machine using 8-bit microcontrollers and restful APIs at Sensor Expo, and we are currently poised to begin specification work on both the postage-stamp form factor and the IIoT data model efforts.

If you are interested in more information about PICMG, its IIoT activities, or how you can join in this work, please contact us (address to right). PICMG is committed to accelerating the deployment of IIoT. We hope that you will consider joining the team.



Doug Sandy *is the Vice President of Technology for PICMG, with over 24 years of industry experience in the embedded computing, industrial automation, telecommunications, and cloud computing spaces. Doug has worked as Technical Fellow, Chief Technology Officer, and Chief Architect for major corporations including Motorola, Emerson, and Artesyn Embedded Technologies. He now enjoys training the next generation of engineers at Arizona State University's Polytechnic Campus where he is a full-time educator and program coordinator for software-engineering capstone projects. Readers may reach Doug at doug@picmg.org.*

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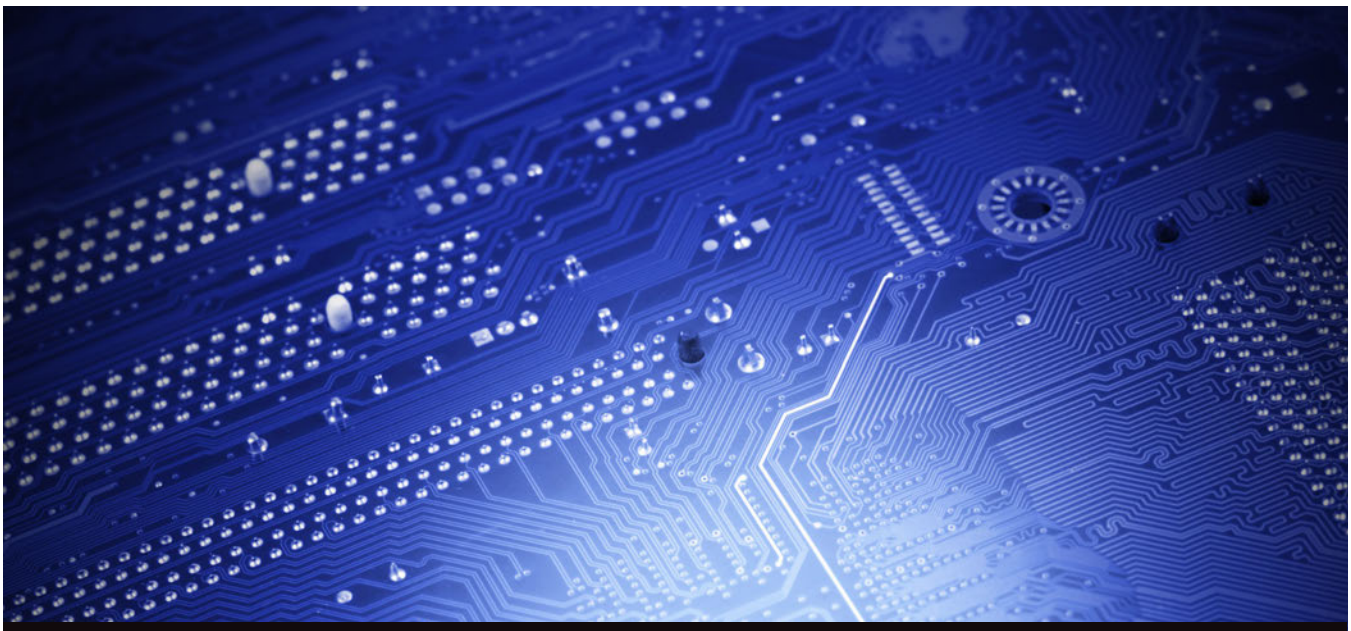

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PICMG is a nonprofit consortium of companies and organizations that collaboratively develop open standards for high-performance telecommunications, military, industrial, and general-purpose embedded computing applications.

Founded in 1994, the group has more than 250 member companies that specialize in a wide range of technical disciplines, including mechanical and thermal design, single-board computer design, very-high-speed signaling design and analysis, networking expertise, backplane and packaging design, power management, high-availability software, and comprehensive system management.

Key standards families developed by PICMG include CompactPCI, AdvancedTCA, MicroTCA, AdvancedMC, CompactPCI Serial, COM Express, SHB Express, and HPM (Hardware Platform Management). In its more than two decades of operation, PICMG has published over 50 specifications developed by participants from hundreds of companies. Work on standards across a wide range of markets, applications, and technologies continues as the boundaries of datacom, telecom, military and aerospace, industrial, man/machine interface applications, and deeply embedded computing continue to blur.

Equipment built to PICMG standards is used worldwide, with any company allowed to build or use equipment without restriction (although certain technologies used for some military applications may be subject to U.S. export restrictions governed by ITAR rules).

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PICMG adheres to a formal, multistep development process. Development work can be periodically be reviewed by all member companies, although work inside of a technical subcommittee is confidential to the members of that committee until that work is ready for broader review by other members. Until a specification or standards-related document is ratified by the entire membership, it is confidential to PICMG. After ratification, all documents are available to the general public.

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PICMG standards – because the organization has such a large number of contributing companies – reflect the extremely wide and deep technical capabilities of its members. By using well-understood and proven open standards, vendors can bring products to market quickly. Customers gain from the price and performance competition that results from many vendors operating in an open marketplace.

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OPEN MODULAR COMPUTING STANDARDS

There are nine distinct "families" of PICMG standards. Many have subsidiary specifications that are designed to add additional capability.

Please visit www.picmg.org/openstandards/ to learn more about each one.

- **Advanced TCA:** This high-performance modular standard, also called ATCA, was developed for critical central-office telecommunications applications and is also used for a wide range of commercial and military applications. It offers a complete management infrastructure so that high-availability systems with "six nines" reliability can be deployed.

- **CompactPCI:** A modular general-purpose computing system based on 3U and 6U Eurocard mechanical standards, it features hot-swap capability and can be either convection- or conduction-cooled. With hundreds of thousands of installations worldwide, this popular architecture is one of the most successful and popular standards in use today.

- **COM Express:** This small-form-factor (SFF) standard is designed for deeply embedded applications where space is at a premium but high performance is required. COM Express boards can be used as standalones or plugged onto an application-specific baseboard with I/O expansion.

- **MicroTCA:** Often called "AdvancedTCA's little brother," MicroTCA is a modular platform for building smaller and less-expensive systems that AdvancedTCA while retaining the high-availability architecture of AdvancedTCA. MicroTCA systems use AMC modules as their basic computing and I/O building blocks.

- **Advanced MC:** This standard defines a family of small, hot-swappable, and fully managed mezzanine cards that can be used to tailor I/O for large AdvancedTCA systems or used as the basis for building MicroTCA systems. They are commonly called "AMCs."

- **CompactPCI Serial:** This relatively new standard uses CompactPCI's mechanical structure but updates the system interconnects to include PCI Express, Ethernet, SATA, and USB. It offers 20 to 40 times the backplane bandwidth of CompactPCI and is ideal for new applications or upgrades to older systems.

- **SHB Express:** This upgrade to the PCI-ISA standard replaces parallel PCI interconnects with serial PCI Express lanes, improving performance and increasing compute power. A passive backplane is used, and standard desktop PCI Express cards can be used for I/O customization.

- **Hardware Platform Management:** Also known as "HPM," this software standard defines how to build fully managed, high-availability AdvancedTCA or MicroTCA systems. It is the first, and currently the only, open standard for system management.

- **PCI-ISA:** PICMG's first open standard, PCI-ISA is used to build rugged, reliable, and maintainable computers that are designed to replace desktop PCs in industrial-control communications or data-acquisition applications. The PCI-ISA standard moves all of the active circuitry normally found on a motherboard to an easily replaceable and upgradable plug-in card. While standard PC cards plug into other slots to customize a system, a PCI-ISA system uses a passive backplane consisting of connectors with no active components.

- **New standards and under development:** The cPCI Serial Space specification, a ruggedized version of CompactPCI Serial that specifically addresses the extreme environment requirements for outer space, was ratified in August 2017. In addition, PICMG is working with members and advisory board industry leaders to develop the elements for an IIoT [industrial Internet of Things] specification. New standards arise when members identify the need to create a new embedded computing standard for a particular market or application.

THE VALUE OF OPEN STANDARDS

What makes PICMG a leading standards organization?
PICMG has more than 250 member companies, all of which combine to bring an extremely wide and deep talent base to the table. Unlike some other consortia, PICMG is not controlled by one or a few companies: It is governed by the Executive Members that work together to ratify processes and procedures, elect officers, and approve budgets. PICMG maintains a "one company-one vote" policy, which means that no single company can dominate the standards-development process.

Over the last several decades, open standards have become increasingly important for a wide range of embedded and specialized computer applications, both big and small. While the definition of "open standard" can vary, for the embedded computer world it usually means a succinct definition of everything a vendor needs to know to build equipment and write software that will work with compatible products offered by other vendors.

In an organization like PICMG, all players, whether large or small, can take an important role. Participants have access to thought leaders in areas they or their company may lack expertise. They also can meet experts in a wide range of engineering disciplines.

PICMG also has an outstanding intellectual property (IP) policy that ensures that members must submit IP declarations throughout the standards-development process, where they can be accepted for use or rejected. To date, no PICMG standard or specification has required any user licenses or royalties. Moreover, anyone can build equipment in accordance with or use PICMG standards whether they are members or not. PICMG is truly an open organization. Dues are low: In fact, the cost of a yearly Executive membership has not changed in 20 years.

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JOINING PICMG

Why join PICMG?
By joining an organization like PICMG, anyone can play an important role. Participants have access to thought leaders in areas they or their company may lack expertise. They come to know experts in a wide range of engineering disciplines. The groups that develop these open standards do so because they are interested in getting something done in a finite amount of time; whenever possible, bureaucracy and politics are kept to a minimum. Members of these development groups have a common goal: To create standards that are widely used and that each company involved can make money from. Companies can specialize in their areas of expertise without needing to be good at everything. In addition to technical collaboration, business collaborations often evolve in a symbiotic way.

Companies that participate in standards development also have a very important advantage: They are already up to speed when the standard is released and can thus be first to market with compliant and leading-edge products.

In its 20-plus years of operation, PICMG has published almost 50 open industry specifications that encompass nine basic standards families developed by participants from hundreds of companies. The Consortium plans to continue its work across a wide range of technologies. Member companies of PICMG have some big plans for the next decade, as designers in the data communications, telecommunications, industrial, and military/aerospace arenas embed technology ever more deeply into specialized and everyday products.

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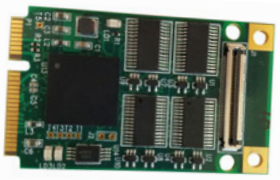

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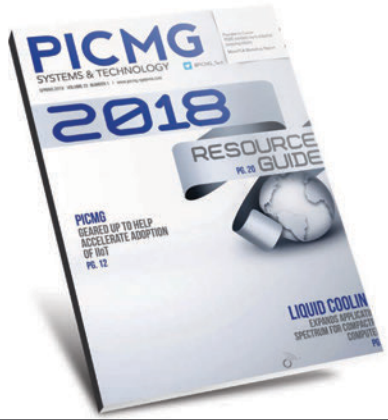

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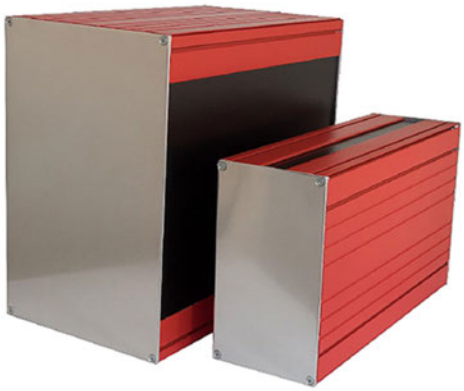

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An extensive EPICS ecosystem of open source tools, libraries and applications, is available to support the physics community in the development of distributed real-time platforms for precision instrumentation and accelerator control systems.

www.ioxos.ch/wp-content/uploads/2018/02/IFC_1420_SDS_A0.pdf
http://picmg.mil-embedded.com/p374804

Operating Systems and Tools

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http://bit.ly/2N4hp73
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Presented by Wind River

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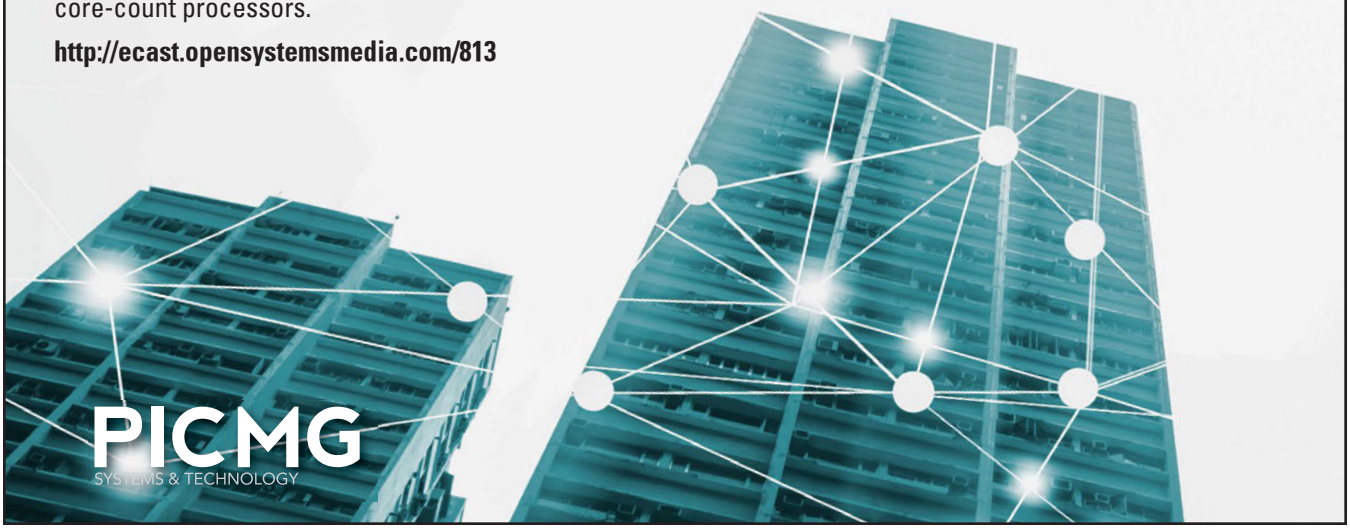

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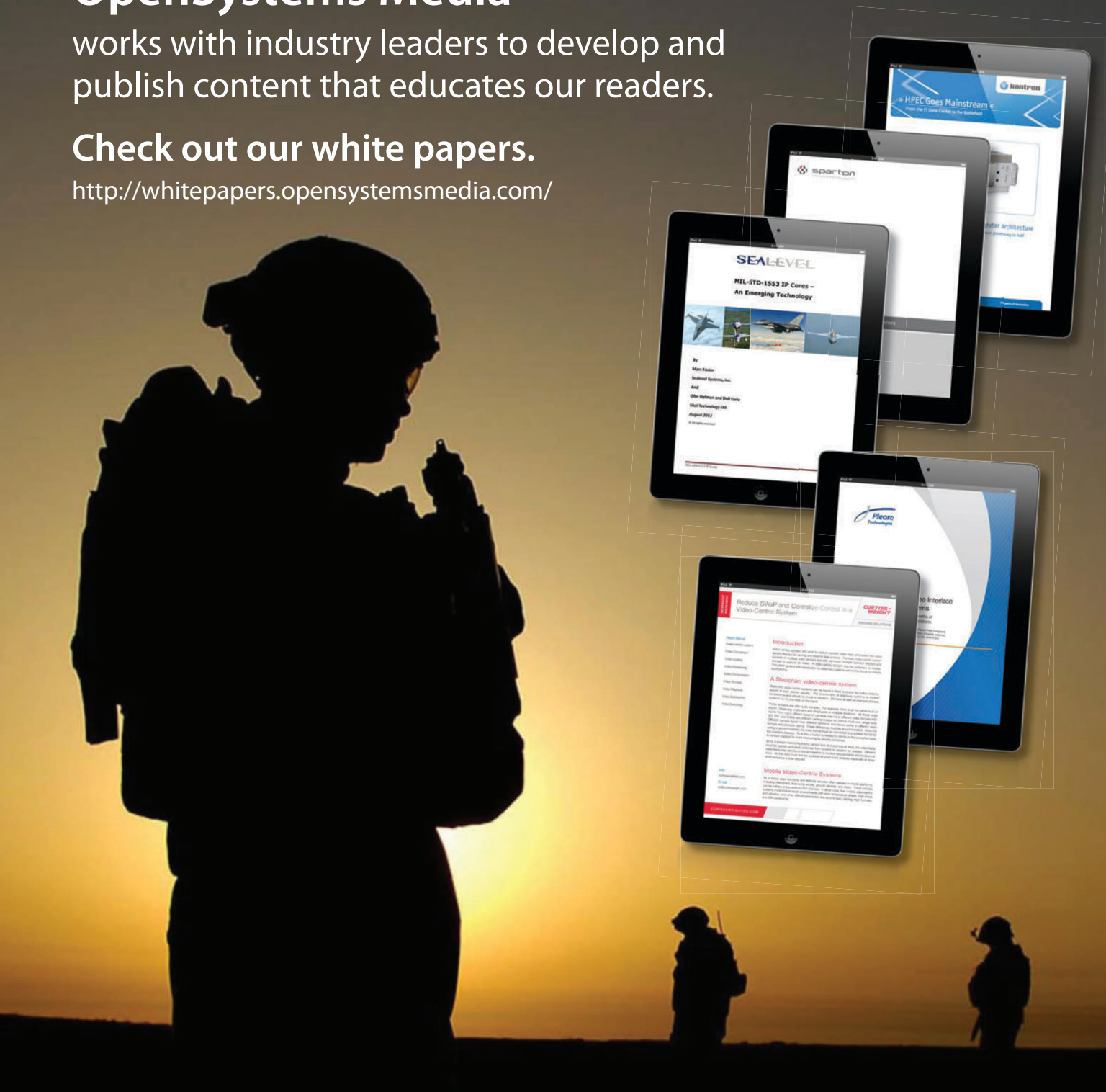

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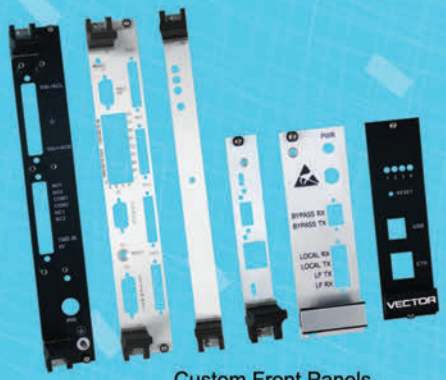

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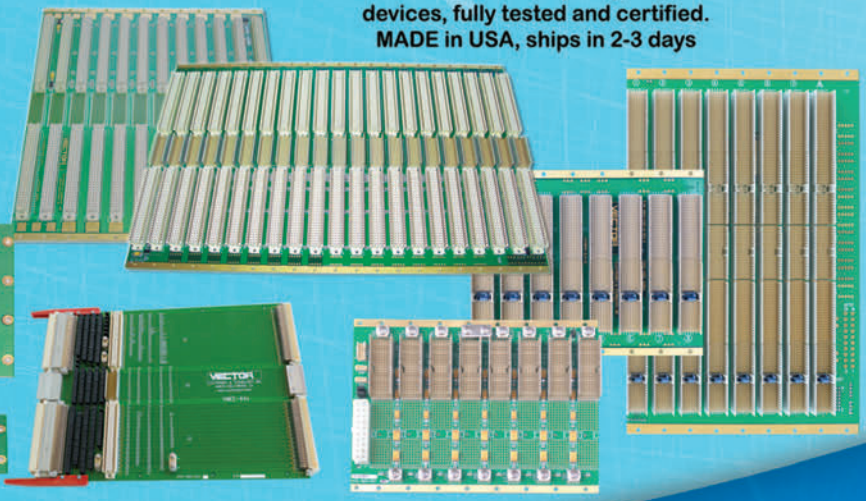

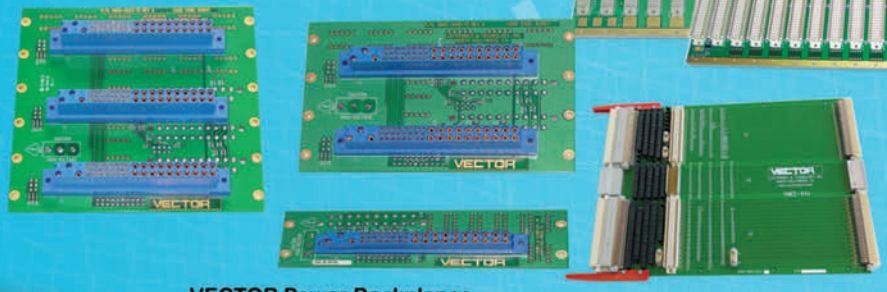

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