VITA TECHNOLOGIES

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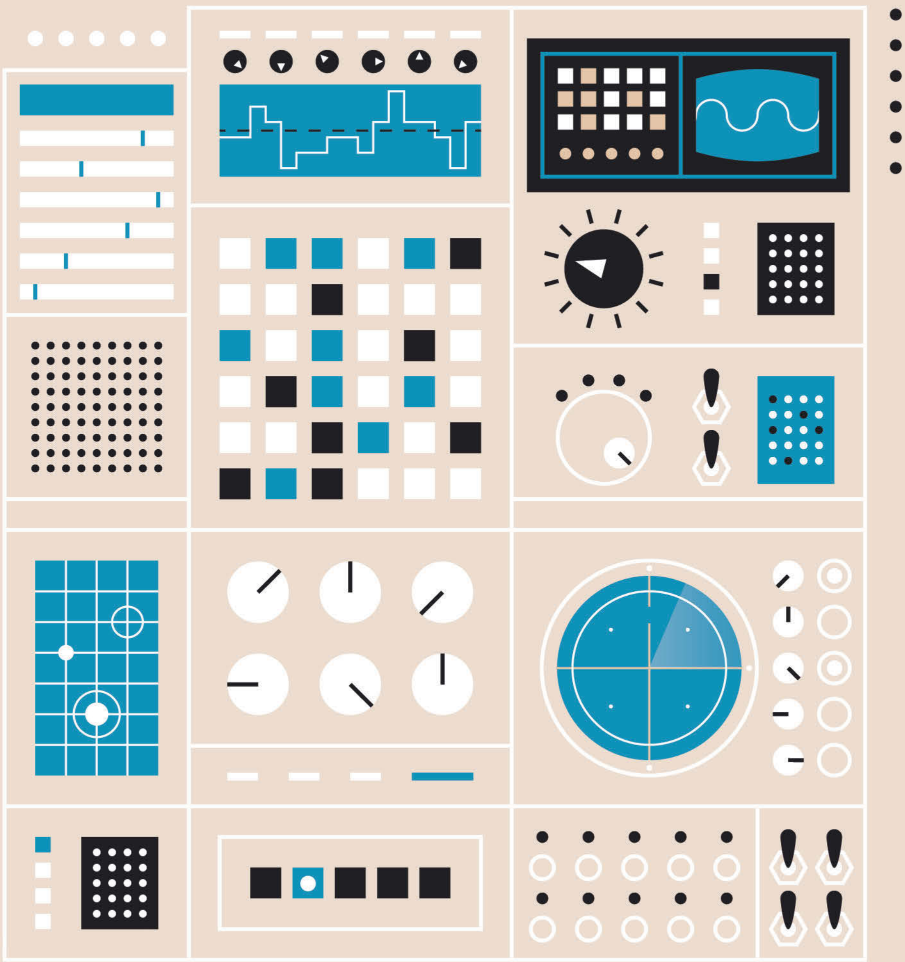

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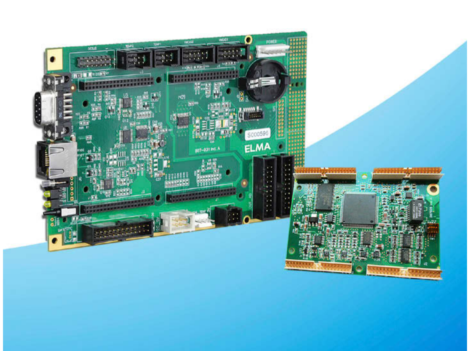

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On the cover

The Fall issue of *VITA Technologies* magazine features columns from Mercury Systems and VadaTech and contributed articles from Pigeon Point Systems and Elma Electronic. Topics covered in this issue include reliability prediction methods, interoperability of VITA 46.11, chassis management for VPX systems, and more.

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Editor's Foreword

By Jerry Gipper, Editorial Director

@VitaTechnology jgipper@opensystemsmedia.com

Autonomous system scenarios

Being from rural northeast Iowa, I am always excited when I see computer technology news from the area. Known more for its agriculture than its computer technology, news related to the latter is, at best, very infrequent. Imagine my excitement the other day when I saw technology news that additionally has potential impact on the world of VITA technology!

A June 25th press release from Rockwell Collins and the National Aeronautics and Space Administration (NASA) announced that they had scheduled joint risk reduction tests that will eventually enable unmanned aircraft systems (UAS) to safely operate in our national airspace. The release was inviting the media to attend but unfortunately I received the release a couple of weeks too late.

The testing, completed in late June, was focused on testing a data link waveform and the ability of a single tower to communicate to multiple aircraft. The waveform will eventually be released as a public resource to help the industry and the Federal Aviation Administration (FAA) develop an appropriate set of rules and requirements for unmanned operations in the national airspace system. This testing was part of the research project's first phase.

"The number of active UASs is only going to grow in the future," said Alex Postnikov, a principal engineering manager in the Advanced Technology Center (ATC) at Rockwell Collins. "Rockwell Collins and NASA are in an exciting position to ensure there is a safe and secure communications link between the pilot on the ground and the unmanned aircraft in the air."

"We tested at different altitudes, different frequencies, and through different modes of operation," said John Moore, principal systems engineer for Rockwell Collins. "We wanted to see if the system operated as we expected it to. We're happy to say things went very well." Moore added that Rockwell Collins will participate in research and testing through 2016. The goal is for the FAA to issue a technical standard order for UASs by 2017.

THE TESTS THAT ROCKWELL COLLINS AND NASA ARE CONDUCTING WILL HELP TO OPEN THE MARKET FOR MANY MORE PLATFORMS OUTSIDE OF THE TYPICAL MILITARY APPLICATIONS.

Unmanned air and ground vehicles are quickly becoming a normal part of our everyday lives. Besides all of the airborne vehicles we hear so much about, there are the efforts by the likes of Google with demonstrations of driverless automobiles. States are now starting to look into revising rules of the road or they are already passing legislation to manage the integration of unmanned vehicles into the open road.

All kinds of scenarios for driverless aircraft and automobiles are emerging, from Amazon package delivery with drones to the FBI warning that driverless cars could be hacked to become lethal weapons by criminals. I am sure new, innovative use models will emerge, some of them useful, others not so much.

The day of unmanned aircraft is already here, and autonomous automobiles and trucks are not too far away. The safety benefits of removing or minimizing the human element and replacing it with technology will far outweigh the disadvantages. The biggest obstacles will be in dealing with the fears and concerns that humans have in letting technology have control of the vehicles. Not only will vehicles become smarter, but the road and infrastructure must also evolve to become more intelligent, making the entire system more reliable and efficient. It is going to take many years to build out the infrastructure but the end product is sure to improve efficiency and safety by removing much of the human factors that lead to accidents.

These tests are important to our industry because many VITA technology suppliers target the UAS industry. VPX is especially suited to these systems – either airborne or ground-based systems. The tests that Rockwell Collins and NASA are conducting will help to open the market for many more platforms outside of the typical military applications. VPX is well-positioned to capture a number of new design wins as the market applications grow. Small form factor (SFF) VPX has opportunity in larger rugged vehicles as well as in the infrastructure for the intelligent highway where rugged SFFs are needed.

I expect to see more news on this from Iowa in the not-too-distant future when John Deere eventually announces a line of autonomous tractors. They have early technology in the fields now so I will keep my eye open for my first UTS – Unmanned Tractor System!

Jerry Gipper, jgipper@opensystemsmedia.com

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VITA Technologies Editorial/Production Staff

Jerry Gipper, Editorial Director
jerry.gipper@opensystemsmedia.com

Amanda Harvey, Assistant Editor
aharvey@opensystemsmedia.com

Steph Sweet, Creative Director
ssweet@opensystemsmedia.com

John McHale, Group Editorial Director
jmchale@opensystemsmedia.com

Sales Group

Tom Varcie, Sales Manager
tvarcie@opensystemsmedia.com
(586) 415-6500

Rebecca Barker, Strategic Account Manager
rbarker@opensystemsmedia.com
(281) 724-8021

Eric Henry, Strategic Account Manager
ehenry@opensystemsmedia.com
(541) 760-5361

Kathleen Wackowski
Strategic Account Manager
kwackowski@opensystemsmedia.com
(978) 888-7367

Asia-Pacific Sales
Elvi Lee, Account Manager
elvi@aceforum.com.tw

Regional Sales Managers
Barbara Quinlan, Southwest
bquinlan@opensystemsmedia.com
(480) 236-8818

Denis Seger, Southern California
dseger@opensystemsmedia.com
(760) 518-5222

Sydele Starr, Northern California
sstarr@opensystemsmedia.com
(775) 299-4148

Europe Sales
James Rhoades-Brown
james.rhoadesbrown@husonmedia.com

Reprints and PDFs

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OpenSystems Media Editorial/Creative Staff

Embedded Computing Design · Military Embedded Systems · DSP-FPGA.com · Industrial Embedded Systems · PC/104 and Small Form Factors · PICMG Systems & Technology · VITA Technologies

John McHale
Group Editorial Director
Military Embedded Systems
PC/104 and Small Form Factors
PICMG Systems & Technology
VITA Technologies

Rich Nass
Embedded Computing Brand Director
Embedded Computing Design
rnass@opensystemsmedia.com

Joe Pavlat, Editorial Director
PICMG Systems & Technology
jpavlat@opensystemsmedia.com

Curt Schwaderer, Editorial Director
Embedded Computing Design
cschwaderer@opensystemsmedia.com

Monique DeVoe, Managing Editor
Embedded Computing Design
DSP-FPGA.com
mdevoe@opensystemsmedia.com

Christine Long, DIY Brand Manager
clong@opensystemsmedia.com

Joy Gilmore, Assistant Webcast Manager
jgilmore@opensystemsmedia.com

Brandon Lewis, Assistant Managing Editor
Embedded Computing Design
Industrial Embedded Systems
PICMG Systems & Technology
blewis@opensystemsmedia.com

Lisa Daigle, Assistant Managing Editor
Military Embedded Systems
PC/104 and Small Form Factors
ldaigle@opensystemsmedia.com

Sally Cole, Senior Editor
Military Embedded Systems
scole@opensystemsmedia.com

Rory Dear, Technical Contributor
Embedded Computing Design
rdear@opensystemsmedia.com

Konrad Witte, Senior Web Developer

Dave Diomede, Creative Services Director

Joann Toth, Senior Designer

Jake Rojas, Graphic Designer

Corporate

opensystemsmedia.com

Patrick Hopper, Publisher
phopper@opensystemsmedia.com

Rosemary Kristoff, President
rkristoff@opensystemsmedia.com

John McHale, Executive Vice President
jmchale@opensystemsmedia.com

Rich Nass, Executive Vice President
jmchale@opensystemsmedia.com

Christine Long, Vice President Online Business
clong@opensystemsmedia.com

Wayne Kristoff, CTO

Emily Verhoeks, Financial Assistant

Headquarters – ARIZONA:
16626 E. Avenue of the Fountains, Ste. 201
Fountain Hills, AZ 85268
Tel: (480) 967-5581

MICHIGAN:
30233 Jefferson
St. Clair Shores, MI 48082
Tel: (586) 415-6500

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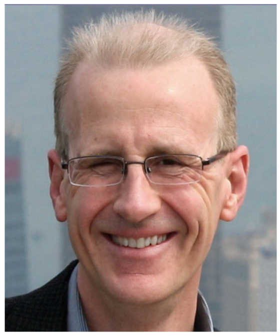

VITA News

By John Bratton

jbratton@mrcy.com

Pacific Pivot focus accelerates demand for OpenVPX server-class embedded processing

Over the past several years, the Obama administration has indicated it would be changing focus from the Middle East and rebalance, or pivot, toward the Pacific. This "Pacific Pivot" regional strategy will require new roles and missions in "more contested" environments, which means that airborne intelligence, surveillance, and reconnaissance (ISR) platforms will be required to operate differently than they have before. In previous Middle East-based conflicts, adversaries typically lacked aircraft and air defenses, allowing us the freedom of deploying ISR platforms in theatre virtually unchallenged. However, as we shift towards the Pacific, these platforms will need to operate at much higher altitudes, for longer periods, and at much greater stand-off distances. They will also need better and more sophisticated sensors than are available today. Finally, as we've seen over the past decade, onboard exploitation or the transformation of vast quantities of data into actionable intelligence in real-time will remain a critical need. This will require more compute or intelligence onboard the platforms so that they can operate more autonomously. Size, weight, and power (SWaP) optimization is critical, as more is demanded from the same size, weight, and power budget. Open architecture-based solutions will be necessary to speed innovation and reduce development costs.

Ever since former U.S. Defense Secretary William Perry announced the commercial off-the-shelf (COTS) initiative in 1994, the pursuit of commercial-item leverage has been underway. The best commercial technology, when expertly adapted for military applications, delivers sophisticated solutions and often dominates whole technology genres. Commercial LCD displays, cell phones, and laptops are examples. When properly architected and packaged for military applications, commercial technology such as CPUs, GPGPUs, and FPGAs have provided huge benefits for delivering rugged, embedded computing subsystems to power sensor platforms. Increasingly, Intel Xeon server-class multicore CPU engines are making inroads to on-platform ISR applications such as radar, EO/IR, and EW, especially as applied to aging platform modernizations, where onboard compute capability is so vital and SWaP and packaging requirements are so challenging.

One example of successfully bringing the highest performing commercial enterprise server technology to embedded computing subsystems can be found in Mercury Systems' Intel Xeon server-class OpenVPX-compliant sensor processing solutions. Mercury's ability to leverage server-class processor technologies, package them so that they are highly reliable in demanding operational environments, and efficiently integrate them with other sensor chain functional elements is well known. The result is a well-engineered, operationally balanced subsystem that can make maximum use of server-class compute engines in modern defense subsystems. These types of subsystems must demonstrate a high Technology Readiness Level (TRL) while delivering balanced, yet massive compute capability, affordably, with the lowest program/technology risk.

Server-class processing modules generate a lot of heat, and thus require innovative cooling and packaging while maintaining open architecture, standards-based compliance. In the Mercury example, the Xeon CPU and memory devices are directly attached to their respective printed circuit boards (PCBs) to reduce volume and ensure thermal efficiencies. Mercury's VITA 48.1-compliant Air Flow-by implementations provide some of the industry's most efficient air-cooling technology, which the company applies to all of their server-class module offerings. As ISR missions in Afghanistan and Iraq transition to higher-altitude, longer dwell missions in the Pacific, even more robust cooling methods will be required to ensure SWaP envelopes are not exceeded. In response to this demand, Mercury recently augmented its Xeon server-class ecosystem with innovative Liquid Flow-by cooling. Liquid Flow-by cooling techniques provide an efficient and elegant solution to high-altitude cooling challenges by using the platform's own fuel or a dedicated coolant source with which to cool the on-platform compute resources, while maintaining open standards-based compatibility. Multiple cooling options provide choices for myriad application needs.

The Pacific Pivot is only the latest regional strategy to emerge as global dynamics and potential threats continue to develop. As new challenges like changing roles and missions in less permissive environments arise, ISR subsystem providers like Mercury continue to stay ahead of the curve, adapting commercial-item technology to solve complex embedded computing challenges.

John Bratton • Product and Solutions Marketing Specialist • Mercury Systems, Inc.

By Justin Moll

justin.moll@vadatech.com

FMCs provide versatility and modularity across multiple platforms

The VITA 57 specification defining the FPGA Mezzanine Card (FMC) has been adopted since 2008. Today FMCs are commonly used in architectures from VPX to CompactPCI to MicroTCA and more. The versatility of the mezzanine approach allows a broad swath of acceptance in various applications.

FMCs are being used as I/O devices in all types of configurations. Since it's an open standard, an engineer can choose the FMC that works for them among dozens of vendors. The FMCs are also used for data conversion, RF interfaces, clock generators, and other specialty purposes. An FMC for ADC is compelling in mil/aero and physics applications. They can be used across multiple subsets of the application, with the flexibility of being changed for unique requirements of an experiment or for specific applications.

The mezzanine approach of FMCs also makes it attractive in many mil/aero and research applications. The modularity of the FMCs provides a cost-effective and easy upgrade path. The FMC can simply be swapped for the interface that meets the performance level. For example, a 1.25 GSPS 10-bit FMC can be upgraded for a 2.5 GSPS version. This is achieved without having to replace the entire FPGA, and without any hardware redesign. Similarly, another advantage of FMCs is the ability to shift I/O options. For example, an FMC with dual RJ-45s (Gig E) can be upgraded to a dual QSFP+ for higher data rates. See Figure 1 for a photo of an RJ-45 Gig E FMC, an SFP+ 10 GbE FMC, and a QSFP+ 40 GbE FMC. Of course, the FPGA carrier where it resides must have the appropriate level of performance as well.

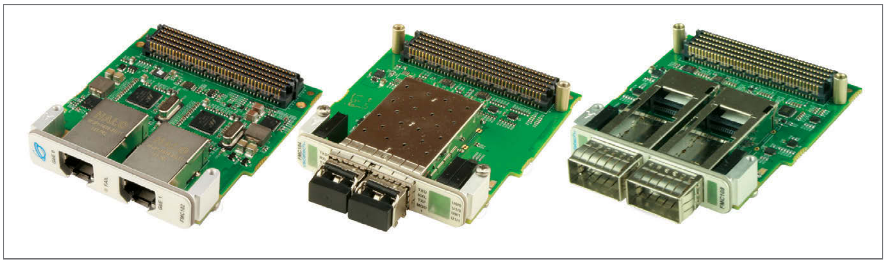

Figure 1 | FMC group photo, from left to right: RJ-45 Gig E FMC; SFP+ 10 GbE FMC; and QSFP+ 40 GbE FMC.

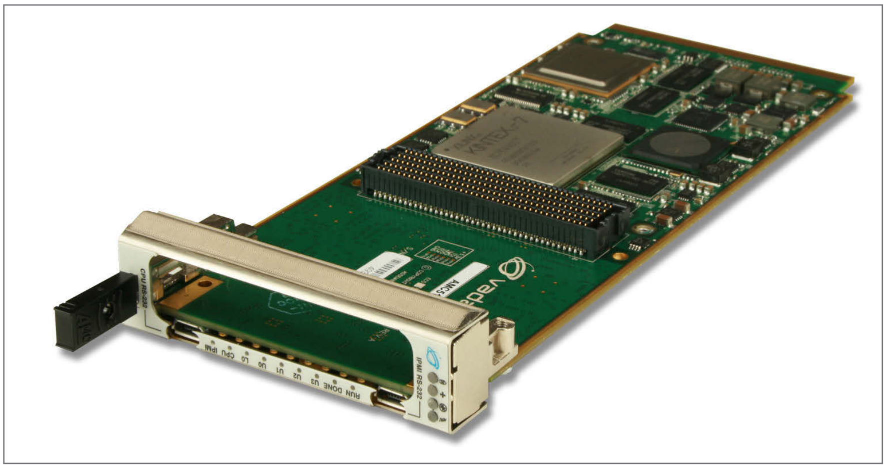

Figure 2 | The Kintex-7 FPGA includes an interconnection for an FMC per VITA 57.

As a VITA standard, one might think of FMCs for VITA form factors such as VME and VPX. However, FMCs are widely used in MicroTCA as well. Figure 2 shows a Kintex-7 FPGA with the interconnection for an FMC per VITA 57. The FMC allows a wide range of ADC and I/O options while the FPGA processor, separate P2040 QorIQ for distributed processing, and DDR3 memory reside on the AMC. Another option for a design is choosing between the wide range of Xilinx- and Altera-based FPGAs. This is typically just a matter of the skill set of the customer's engineering team. Both companies are moving to system on chip (SoC)-style designs that are very efficient, such as Xilinx's Zynq. It has a nice integration between the CPU and the FPGA, making a designer's task a little easier. The dual-core ARM processor provides a smooth development path.

The versatility of FMCs is very beneficial for many applications. They provide a cost-effective and efficient upgrade path for FPGA requirements.

Justin Moll
Director of Marketing • VadaTech

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Choice of reliability prediction methods

By Jerry Gipper, Editorial Director

The role of a reliability engineer is unbearably difficult in today's age of electronic components, especially when it comes to making solid predictions on component and system failure rates. Over time, reliability has increased but at the same time, many of the tools used to make predictions have decreased in capability. Efforts by VITA members have reversed the deficiency in many of the tools.

Since the day of the very first computer, there were failures. Components burned out, circuits shorted or opened, solder joints failed, pins were bent, and metals reacted with each other. These and countless other failure methods plagued the computer industry from the very first circuit to today. Learning how to compensate for failure, understanding failure mechanisms, and how to predict computer failure has become a full profession in itself.

Failure rate predictions are utilized by logistics, systems, and reliability engineers for a myriad of purposes, including reliability analysis, cost trade studies, availability analysis, spares planning, redundancy modeling, scheduled maintenance planning, product warrantees, and guarantees.

Reliability predictions are very important to the management of a product life cycle. These predictions are necessary for many reasons, such as:

- Help assess the effect of product reliability on the maintenance activity and on the quantity of spare units required for acceptable field performance of any particular system. Reliability prediction can be used to establish the number of spares needed and predict the frequency of expected unit level maintenance.
- Provide necessary input to system-level reliability models. System-level reliability models can be used to predict frequency of system outages in steady-state, frequency of system outages during early life, expected downtime per year, and system availability.
- Provide necessary input to unit and system-level life cycle cost analyses. Life cycle cost studies determine the cost of a product over its entire life. This includes how often units and systems fail during the first year of operation as well as in later years, helping to establish total life cycle cost estimates.
- Assist in deciding which product to purchase from a list of competing products. As a result, it is essential that reliability predictions be based on a common procedure. Given that everything else is equal, reliability predictions can be a deciding factor.
- Can be used to set factory test standards for products requiring a reliability test. Reliability predictions help determine how often the system should fail, making it possible to determine if adequate testing is being performed.

- Are needed as input to the analysis of complex systems such as weapon systems and complex control systems. It is necessary to know how often different parts of the system are going to fail even for redundant components.
- Can be used in design trade-off studies. For example, a supplier could look at a design with many simple devices and compare it to a design with fewer devices that are newer but more complex. The unit with fewer devices is usually more reliable.
- Can be used to set achievable in-service performance standards against which to judge actual performance and stimulate action. Feedback can then be used to adjust testing procedures.

Reliability prediction methods

Accurate prediction of the reliability of electronic products requires knowledge of the components, the design, the manufacturing process, and the expected operating conditions. Once the prototype of a product is available, lab tests can then be utilized to obtain more accurate reliability predictions. Several different approaches have been developed to predict the reliability of electronic systems and components. Each approach has its unique advantages and disadvantages. Among these approaches, three main categories are often used within government and industry: empirical (standards based), physics of failure, and life testing.

Prediction Method	Applied Industry
MIL-HDBK-217F and Notice 1 and 2	Military
Bellcore/Telcordia	Telecom
IEC 62380 (RDF 2000)	Telecom
SAE Reliability Prediction Method	Automotive
PRISM	Military/Commercial

Table 1 | Empirical prediction methods in common use.

Empirical prediction methods are based on models developed from statistical curve fitting of historical failure data, which may have been collected in the field, in-house, or from manufacturers. These methods tend to present good estimates of reliability for similar or slightly modified parts. Some parameters in the curve function can be modified by integrating existing engineering knowledge. The assumption is made that system or equipment failure causes are inherently linked to components whose failures are independent of each other. There are many different empirical methods that have been created for specific applications. Table 1 lists some of the commonly used prediction standards.

A physics of failure (PoF) approach is based on the understanding of the failure mechanism and applying the physics of failure model to the data. PoF analysis is a methodology of identifying and characterizing the physical processes and mechanisms that cause failures in electronic components. Computer models integrating deterministic formulas from physics and chemistry are the foundation of PoF.

With the life testing method, a test is conducted on a sufficiently large sample of units operating under normal usage conditions. Times-to-failure are recorded and then analyzed with an appropriate statistical distribution in order to estimate reliability metrics. Operating conditions are often accelerated and amplified to compress lifetime wear and tear into a manageable test time measured in days or weeks. This testing is often called Life Data Analysis, Weibull Analysis, or Highly Accelerated Life Test (HALT). Some time-to-failure data from life testing may be incorporated into some of the empirical prediction standards (i.e.: Bellcore/Telcordia Method II) and may also be necessary to estimate the parameters for some of the physics of failure models.

Failure of the methods

The old methods of predicting reliability in electronics have begun to fail us. MIL-HDBK-217 has been the cornerstone of reliability prediction for decades. But MIL-HDBK-217 is rapidly becoming irrelevant and unreliable as we venture into the realm of nanometer geometry semiconductors and their failure modes. The uncertainty of the future of long established methods has many in the industry seeking alternative methods.

ACCURATE PREDICTION OF THE RELIABILITY OF ELECTRONIC PRODUCTS REQUIRES KNOWLEDGE OF THE COMPONENTS, THE DESIGN, THE MANUFACTURING PROCESS, AND THE EXPECTED OPERATING CONDITIONS.

On the component supplier side of the equation, semiconductor suppliers were seeing such increases in component reliability and operational lifetimes that they slowly began dropping MIL-STD-883B testing and nearly all have dropped their lines of mil-spec parts. Instead they have moved their focus to commercial-grade parts where the unit volumes are much higher. The purchasing power of the military markets has become insignificant to the point where there is no longer any leverage. Instead, system builders took the commercial-grade devices, sent them out to testing labs, and found that a large majority of them would, in fact, operate reliably at extended temperature ranges and environmental conditions. Field data gleaned over the years has improved much of the empirical data of complex algorithms for reliability prediction.

A new set of problems have arisen with smaller die geometries. Previous semiconductor generations were showing operational lifetimes of 10-15 years or more. However, empirical evidence is now showing that nm-geometry integrated circuits (ICs) are wearing out in just 3-5 years. The small geometry parts are plain wearing out faster, and the commercial users really don't care. They would rather see consumers replace their smart devices every two or three years so the shorter life cycles play into their product strategies. However, with multi-billion dollar weapons platforms, those life cycles just don't fit the model.

Reliability Community to the rescue

Several years ago VITA members saw the need for improving the consistency and traceability of reliability prediction (MTBF) data for electronic devices used in defense and aerospace applications.

The Reliability Community working group was formed to investigate and develop industry standards to address electronics failure rate prediction and assessment.

The community is comprised of representatives from electronics suppliers, system integrators, and the Department of Defense (DoD). The majority of the work is driven by the user community that depends so heavily on solid reliability data. BAE Systems, Bechtel, Boeing, General Dynamics, Harris, Lockheed Martin, Honeywell, Northrop Grumman, and Raytheon are some of the demand-side contributors to the work done by the Reliability Community. These members have developed community of practice documents that define electronics failure rate prediction methodologies and standards. The efforts have produced a series of documents that have been ANSI and VITA ratified. Where applicable, these standards provide adjustment factors to existing standards.

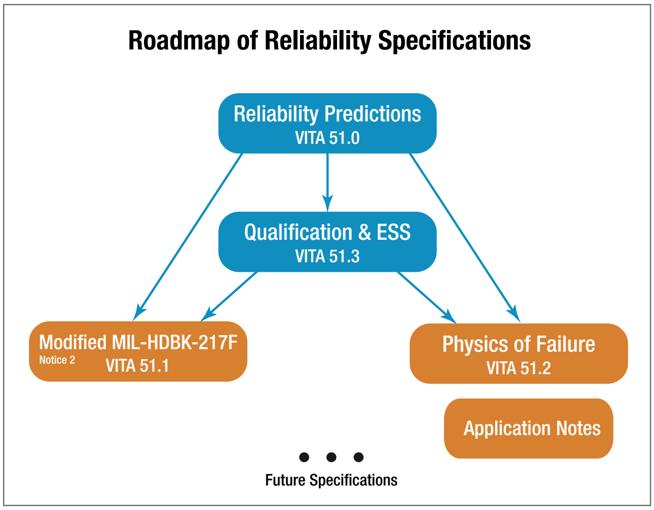


Figure 1 | Current roadmap of VITA 51 Reliability specifications.

The Reliability Community addresses the limitations of existing prediction practices, with a series of subsidiary specifications that contain the "best practices" within industry for performing electronics failure rate predictions. The members recognize that there are many industry reliability methods, each with a custodian and acceptable practices to calculate electronics failure rate predictions. If such a method is identified as requiring additional standards for use by electronics module suppliers, a new subsidiary specification will be considered by the working group.

ANSI/VITA 51.0 Reliability Prediction and its subsidiary specification – ANSI/VITA 51.1 Reliability Prediction: MIL-HDBK-217 – define consistency and repeatability for mean time between failure (MTBF) calculations (see Figure 1). The intention is to supplement MIL-HDBK-217.

ANSI/VITA 51.2 PoF Reliability Predictions defines standard methods for using physics of failure in reliability prediction.

ANSI/VITA 51.3 Qualification and Environmental Stress Screening in Support of Reliability Predictions provides information on how qualification levels and environmental stress screening (ESS) influences reliability.

Current status

Work continues in all of these specifications. Adjustments have to be made for new components and new thinking on failures. As new electronics technology is developed, new methods will be developed, documented, and added to future releases of these standards and subsidiary specifications.

The VITA Reliability Community invites participation in both the development and implementation of the documents. The Reliability Community maintains a LinkedIn group, which is open to anyone with an interest in reliability predictions: www.linkedin.com/groups?home=&gid=4701272

For more information or to get involved in development of these specifications, visit www.vita.com/reliability.

Validating the interoperability of VITA 46.11-based system management elements

6-slot VITA 46.11-enabled OpenVPX chassis. Photo courtesy of Mercury Systems, Inc.

By Mark Overgaard

VITA 46.11 was adopted by the VITA Standards Organization (VSO) as a Draft Standard for Trial Use in November 2013. VITA 46.11 aims to enable the creation and integration of standardized, independently implemented, chassis and plug-in module system management components, reducing integration time and cost, as well as time to theatre. The article "System management on VPX: Leveraging VITA 46.11 for VPX plug-in modules," in the Spring 2014 issue of VITA Technologies *introduced the standard, with an emphasis on its plug-in module level.*

A key premise of the VITA 46.11 initiative and an important basis for high expectations on its benefits is that independently implemented management components, such as Intelligent Platform Management Controllers (IPMCs) on plug-in modules and Chassis Managers can successfully interoperate. The VITA 46.11 working group has realized that this premise requires not only careful attention to the content of the standard, but complementary live interoperability testing as well. Consequently, the group has organized the first VPX System Management Interoperability Workshop (VSM-IW) to perform such testing. This first VSM-IW is scheduled in early September 2014, and will be hosted by the current VITA 46.11 working group chair, Mercury Systems.

This article discusses the approach to interoperability testing that will be used in these VSM-IWs, including how that approach leverages corresponding work by PICMG for ATCA.

How is the VSO taking advantage of PICMG's interoperability testing experience?

The VSO made a conscious choice to base VITA 46.11 on the corresponding management layer of PICMG's AdvancedTCA (ATCA) architecture, rather than start from scratch. This choice accelerated development of the standard and will hasten availability and maturity of VITA 46.11-compliant products.

This choice is also benefiting the VITA 46.11 interoperability initiative. PICMG has held dozens of interoperability testing events (now called TCA-IWs, or Telecom Computing Architecture Interoperability Workshops) dating back to 2002. Continuing its strong cooperation in this area, PICMG has authorized the VSO to use the relevant subset of the test plans from those events as a basis for VSM-IW testing. PICMG uses over 30 of these plans, each developed by IW participants, then reviewed and iterated with other participants.

Each test plan focuses on a functional area where interoperability testing is important. The VITA 46.11 working group has picked a subset of the PICMG plans for review and adaptation, as necessary, to the VPX context. The group has also defined a further set of test areas that are specific to VITA 46.11 and is developing test plans for each of those areas as well.

PICMG has also passed on to the VSO the organizational tools that it has developed over its decade-plus of TCA-IWs. Several of the active VITA 46.11 working group members, including Pigeon Point Systems, participated in most or all of the PICMG TCA-IWs, and are contributing that overall experience as well.

What are the critical interoperability interfaces for VITA 46.11?

Figure 1 shows the management stack defined by VITA 46.11, starting at the bottom with the IPMC on each compliant plug-in module. Next up is the

Chassis Manager, which monitors and supervises the IPMCs in a chassis and represents the chassis to a logical System Manager. The Chassis Manager may be implemented on a redundant basis, but even in that case, would still implement a single logical Chassis Manager function.

Interoperability across the Chassis Manager-to-IPMC interface (System IPMB in the figure) facilitates combining plug-in modules from multiple vendors, each of which can potentially make different implementation choices for their IPMCs. Some IPMCs in a given chassis may be adapted from generic commercial off-the-shelf (COTS) cores, as recommended in the earlier article referenced above. Other plug-in modules may integrate IPMCs implemented from scratch by their respective vendors.

Interoperability across the System Manager Interface allows potentially large investments in upper level management applications (all encompassed within the logical System Manager) to be applied across multiple independent Chassis Manager implementations. VITA 46.11 does not attempt to define the functionality of the System Manager, only the minimum characteristics of its interface to the Chassis Manager.

The lead-in photo for this article shows an example VITA 46.11-enabled OpenVPX chassis with modules that would be suitable for use in a VSM-IW. The Chassis Manager Ethernet interfaces on the front of the chassis could be used as the System Manager interface.

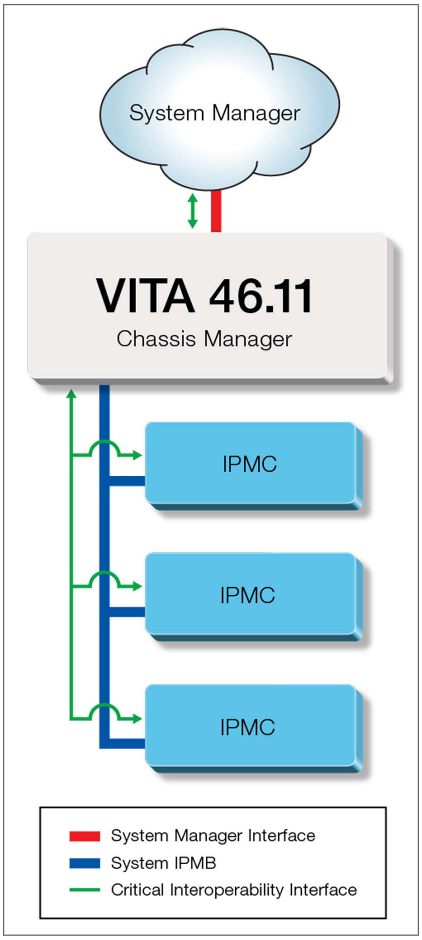


Figure 1 | VITA 46.11 system management stack, highlighting critical interoperability interfaces between: a) System Manager and Chassis Manager; b) Chassis Manager and IPMCs.

How will VITA 46.11 interoperability be tested in VSM-IWs?

Interested vendors with VITA 46.11 products will bring equipment for testing at each VSM-IW. For the Chassis Manager to IPMC (or System IPMB) interface, the basic idea is to allocate a test session for each important [Chassis Manager + IPMC] pair where that pair is exercised according to the applicable test plans. This typically means a session for each [VITA 46.11 chassis provider + VITA 46.11 plug-in module provider] pair. Each chassis and plug-in module supplier may have multiple chassis or plug-in modules, possibly with some variations in their VITA 46.11 implementations. The idea for each of these sessions is to use the test plans to check interoperability of that set of chassis and plug-in modules. The overall VSM-IW is a series of test blocks, perhaps two or three hours each, with parallel test sessions in each test block and a goal to have at least one session for each pair of participating chassis and module vendors by the end of the event.

Participant companies use the group-developed test plans during these sessions in whatever way they wish. Ideally, they will have automated test scripts that make the testing quick and reproducible. Any such test automation is developed by each participating company for its own use.

In the PICMG TCA-IWs, there are mutually agreed ground rules, including that testing results are confidential to the vendor of a component under test and are not to be used for competitive purposes. Comparable rules have been adopted for VSM-IWs so that potential participants can be confident that their participation is a constructive experience.

How does the tiered architecture of VITA 46.11 affect interoperability testing?
VITA 46.11 defines two tiers of functionality for the Chassis Manager and IPMC components. Tier 1 components have minimal facilities, which can be simpler and less expensive to implement. Tier 2 components deliver more functionality in the management layer, allowing greater reuse of those facilities across applications. Each component asserts compliance with one of those tiers. Figure 2 shows the tier architecture.

VITA 46.11 requires that tier 2 Chassis Managers work with a chassis that contains either tier of IPMCs, including a mixture of both tiers. Tier 1 Chassis Managers are required to work only with tier 1 IPMCs. Other combinations are optionally supported. Given these requirements, the VSM-IW test sessions and test plans need to consider the tier level of components under test and any test automation should be designed to support at least the mandatory tier combinations.

How do other PICMG management layer specs affect VITA 46.11 interoperability?
Because of the strong affinity between ATCA management and VITA 46.11, there are two other specifications in the PICMG Hardware Platform Management (HPM) series that can be applied, essentially as-is, in the VITA 46.11 context. HPM.1 and HPM.2 define implementation-independent frameworks that enable: 1) upgrading firmware on management controllers, especially IPMCs and 2) connecting IPMCs to an inside-the-box Ethernet to supplement communication on the much slower (System) IPMB.

Of these two specifications, HPM.1 is the most crucial for a VITA 46.11 IPMC, since an IPMC is virtually certain to need firmware upgrade(s) across a potentially long lifetime. HPM.1 is the only vendor-independent firmware upgrade architecture available for management frameworks based on the Intelligent Platform Management Interface (IPMI). Both VITA 46.11 and ATCA management are based on IPMI.

The VSO may eventually do an explicit adaptation of HPM.1 and HPM.2 PICMG specifications to the VITA 46.11 context, but they can benefit VITA 46.11 users immediately, especially HPM.1.

Figure 3 shows the HPM.1 architecture for a VITA 46.11 context. HPM.1 defines a fairly sophisticated firmware upgrade facility. Firmware upgrade images and IPMCs are identified and

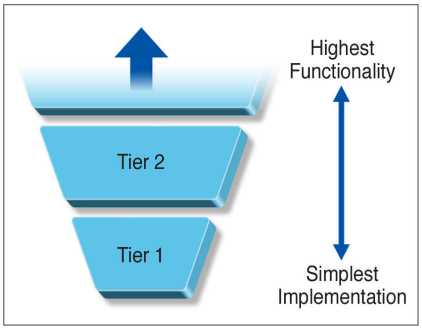


Figure 2 | HPM.1 architecture for VITA 46.11.

matched by the upgrade agent to be sure that only compatible firmware is loaded on an IPMC (see the IPMC types A and B in Figure 3). IPMCs can have multiple upgradeable elements, such as microcontroller (μC) firmware and a supporting Programmable Logic Device (PLD). Type A IPMCs in the figure have just the first element class, while type B IPMCs have both.

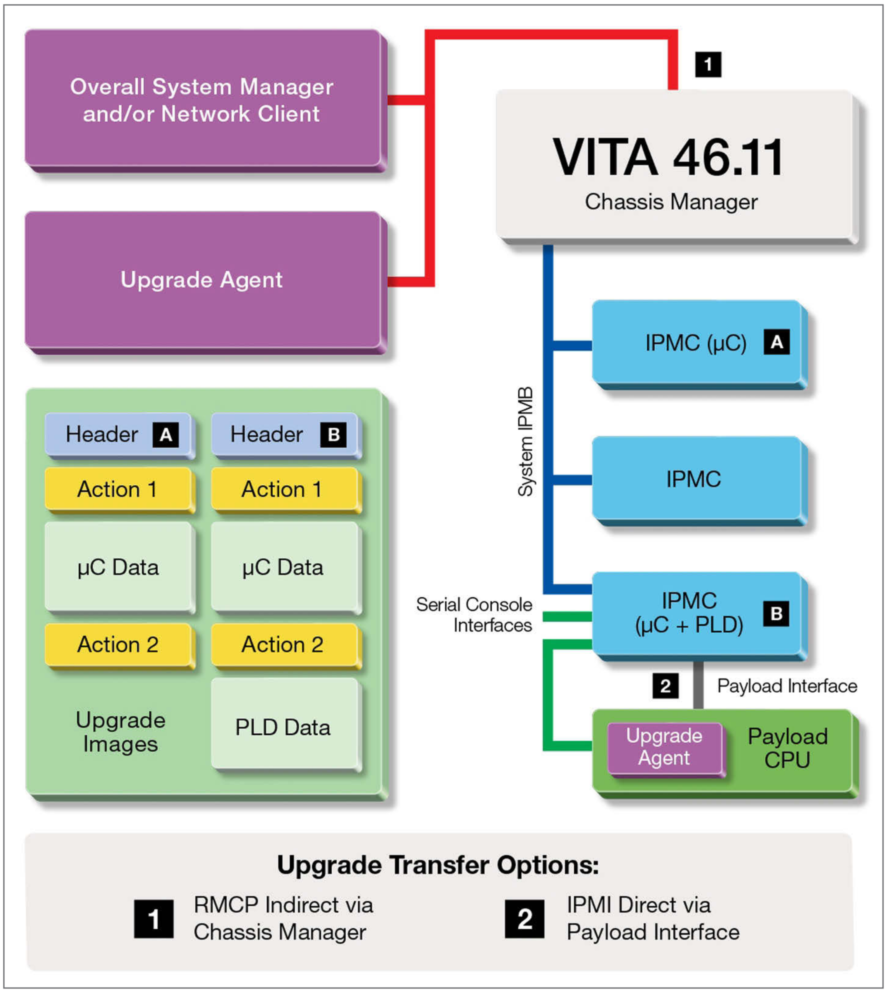


Figure 3 | The VITA 46.11 architecture defines functionality tiers for both Chassis Managers and IPMCs to make it easier to adapt the management layer for differing application needs, while preserving predictable interoperability.

As Figure 3 shows, there are two ways to transfer upgrade images to an IPMC. In the first way, the upgrade agent establishes a Remote Management Control Protocol (RMCP) session with the Chassis Manager, which proxies that session to the IPMC being upgraded via System IPMB. RMCP is a UDP-based protocol defined by IPMI. It is important to demonstrate interoperability for this upgrade method, so that a single upgrade agent can successfully upgrade firmware for multiple types of IPMCs in a single chassis or group of chassis that make up a system.

In the second upgrade approach, an upgrade agent could run on a main payload CPU (perhaps a Xeon or a PowerPC) and communicate with the IPMC over what VITA 46.11 calls the payload interface between them. This approach is much more likely to be vendor-specific, since it depends on the implementation details of the payload CPU and its operating system, as well as the payload interface. Therefore, this path is much less important for interoperability testing.

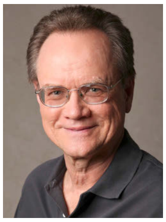
How can VPX vendors and users help to ensure VITA 46.11 interoperability?

VPX users who need VITA 46.11 support in their platforms should insist on system elements (including chassis and plug-in modules) with a demonstrated interoperability record, developed by vendors with a commitment to interoperability.

VPX vendors who incorporate VITA 46.11 support into their chassis and/or plug-in modules can maximize interoperability for their products by:

- Basing their management layer on COTS components, adapted to their specific needs, since they are likely to have a better interoperability record;
- Choosing COTS management component vendor(s) who are participating in the VITA 46.11 VSM-IW initiative and whose components have already benefited from thorough interoperability testing and field validation in the ATCA context.

Pigeon Point Systems' Chassis Manager and IPMC solutions are both examples of COTS management components for VITA 46.11 that meet the above criteria.



__Mark Overgaard__ is the Founder and CTO of Pigeon Point Systems. He is a leader in the VITA 46.11 working group and actively contributed to the development of VITA 46.11. Within PICMG, he chairs the HPM.x subcommittee and participates in numerous others. Readers may reach him at mark@pigeonpoint.com.

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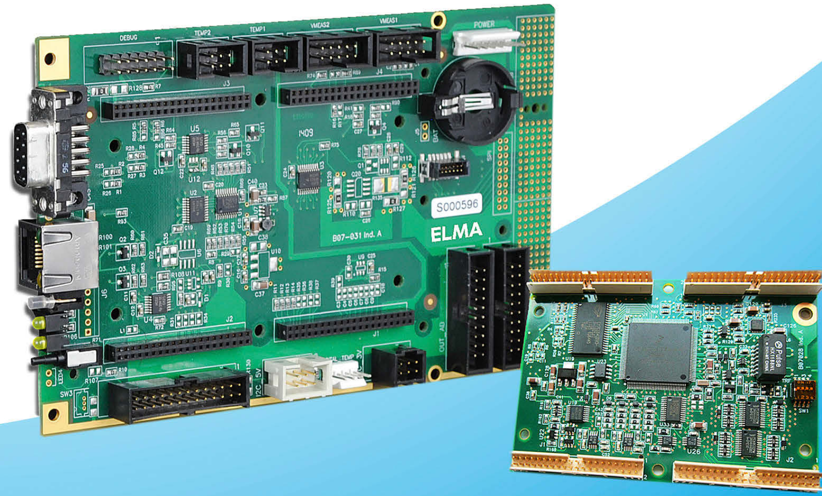

Chassis management for VPX systems

By Gary Hanson

Elma VITA 46.11 chassis manager and carrier card for VPX shelf manager.

Systems built to VITA standards, such as VME, have not traditionally needed the high reliability of many of the telco systems, and have relied upon front panel LEDs to indicate fan failure, voltage monitoring, and thermal issues with the boards and chassis. While VME has long been the preferred architecture of the military and aerospace industry, as higher speeds and increased reliability became more critical to system operation, it was apparent that these older architectures just wouldn't cut it. VPX, or VITA 46.0, was VITA's answer to implement modern high-speed interconnects, real-time monitoring, and remote mitigation of certain system parameters in harsh environmental applications.

However, due to the large number of possible configurations, the interoperability of these VPX-based systems was questionable. VITA introduced OpenVPX, which addressed many of the interoperability and configuration concerns.

The next iteration was VITA 46.11 "System Management on VPX" specification, released in November 2013 as a draft standard for trial use. VITA 46.11 leverages the shelf management functionality that has been used for years in the telco industry to add reliability and robustness to typical VPX applications.

Chassis management

VITA 46.11 brings a new level of chassis management to VPX as an advanced monitoring tool versus using LEDs as indicators of problems. Prior to this specification, the various VITA systems had very limited management or monitoring capabilities unless custom software was written to interface with the boards. For example, the only real monitoring in VME systems was from the utility bus signals:

- System Clock (SYSCLOCK)
- AC Fail (ACFAIL*)
- System Reset (SYSRESET*)
- System Failure (SYSFAIL*)
- Serial Bus A (SERA)
- Serial Bus B (SERB)

While there are various timing requirements for these signals that make sure the boards come up when all the boards are ready, the only real oversight traditionally done on these systems was to monitor the backplane voltages, and sometimes the fan speed (or a fan fail signal) or the chassis temperature. Without elaborate middleware there was no central location where a developer could consistently monitor critical parameters, such as board temperature and health, backplane voltages, chassis temperature, or fan speed.

The new VPX chassis manager enables remote access to any board and chassis that supports VITA 46.11. Since the VPX shelf manager is based on PICMG's ATCA version of shelf management, a brief overview will provide some needed background.

CompactPCI shelf manager

PICMG started using shelf management in the 2000s, when the PICMG 2.9 CompactPCI Shelf Management specification was released. At this point, the shelf management primarily consisted of maintaining an inventory, logging events, and monitoring sensors. For CompactPCI, there are only 18 IPMI commands that need to be supported.

IPMI, or intelligent platform management interface, is a standardized computer system interface or protocol that communicates across an I2C bus connected to each board, the shelf manager, and any other intelligent FRUs (field replaceable units). CompactPCI provided for one IPMB (intelligent platform management bus) for communication.

ATCA shelf manager

The shelf management function was expanded with the ATCA (PICMG 3.0) specification, providing extensive management capabilities. These include low-level hardware management service, high-speed management services based on TCP/IP protocol, and in-band application management. Because it was geared towards the telecommunications industry, ATCA was designed for redundancy using two IPMBs, which could be bussed or radial.

While low-level management consists mainly of monitoring power, cooling, and interconnect resources, the ATCA shelf manager watches over the basic health of the system, reports anomalies, and takes corrective action when necessary. It monitors, controls, and ensures the proper operations of the ATCA boards and any other chassis components. The shelf manager can also retrieve inventory information as well as receive event reports and failure notifications. If necessary, it can perform basic recovery operations including resetting or power-cycling boards.

VITA 46.11 (VPX shelf management)

By leveraging the inherent capabilities of the PICMG ATCA shelf manager, VITA is reducing a great amount of the preliminary development work for the implementation of the VITA 46.11 chassis manager.

One of the major differences between the PICMG 3.0 shelf manager and the VITA 46.11 chassis manager is that PICMG 3.0 requires all boards to have IPMCs (IPMI controllers), however, IPMCs are optional for VITA 46.11 boards.

The standard VPX system does not require system management to function and hot swapping is not required, which precludes the ability of the VPX chassis manager from providing power management. Since the chassis manager does not provide power management and not all boards will have IPMCs, electronic keying (E-Keying) cannot be used for the VPX systems.

However, the VITA 46.11 specification does state that there may be some level of E-Keying in the future, and the existing VPX specification does provide for physical keying to prevent plugging incompatible boards into the wrong backplane slot.

The primary functions of the VITA 46.11 chassis manager are: inventory management; sensor management; system configuration; recovery; and diagnostic management. The three VITA 46.11 chassis manager layers are: IPMC; chassis manager; and system manager. These management layers are hierarchical in nature, where the IPMC (board level management) communicates with the ChMC (chassis manager), which, in turn, reports to the system manager. The system management layer monitors multiple chassis.

IPMC (IPMI controller)

The lower logical layer of management would be the IPMCs, which are required on all intelligent FRUs, such as front loading VPX plug-in modules, fan trays, power supplies, etc. An IPMI controller for boards or intelligent FRUs is used to monitor: health of the board or FRU; voltages; temperature; device ID; serial numbers; part numbers; and software versions. The SDR repository will provide a full list of all the sensors on a particular board or FRU.

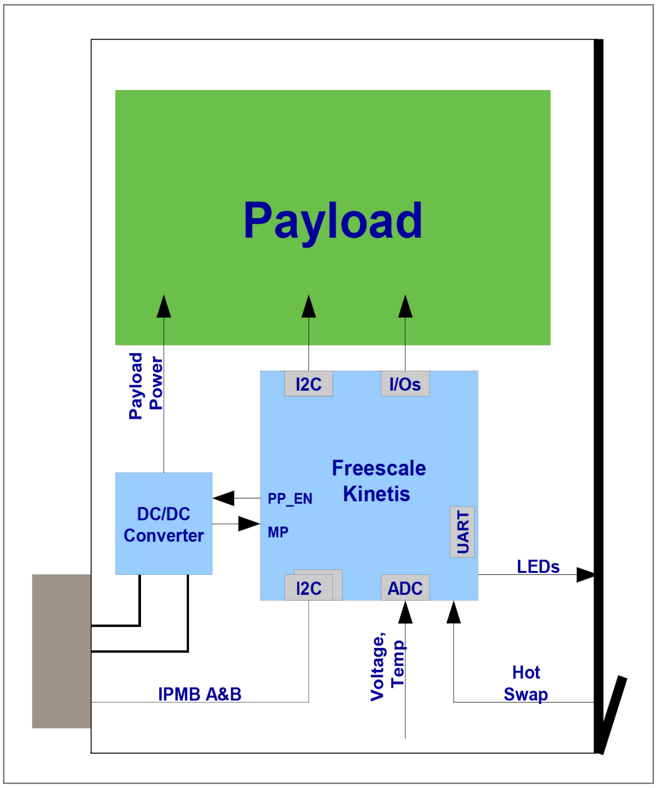

Figure 1 | The IPMC monitors several parameters simultaneously for better system management.

Figure 1 shows a block diagram of an IPMC where the Freescale processor has connections to the IPMB and the payload through both I2C and analog I/O, providing information on most of the sensors. This IPMC also has links to the DC/DC input power enabling power management to the hot swap controller, allowing for hot swapability as well as links to LEDs on the front panel. The IPMC shown will support cPCI, ATCA, AXIe, and VITA 46.11 applications.

Chassis management controller (ChMC)

Next up is the chassis management controller (ChMC), which could be implemented in several ways. It could be implemented on one of the front-loading VPX plug-in modules, as a mezzanine board that plugs onto the backplane, or as a standalone board.

The lead image of this article shows a VITA 46.11 chassis manager next to a 3U x 160 mm carrier card. In this implementation, the chassis manager could be mounted to the carrier card allowing for a pluggable interface.

The advantages of any VPX chassis management controller are numerous:

- **Redundancy.** While not a requirement for a VPX chassis manager, this would make the system more robust.
- **Simplified power management.** VITA 46.11 does not require E-Keying or power management, but they may be useful in the future. And since ATCA requires them, most VPX chassis managers will already support this.

- **Cooling control.** Although several methods could be used, a typical method is to monitor board and chassis temperatures, then adjust the fan speed to maintain the predetermined range.
- **Inventory management.** The chassis manager maintains a full list of all intelligent FRUs and boards as well as any other components that support VITA 46.11 (mandatory support of VITA 46.11 in VPX boards is not yet a requirement).
- **Sensor management.** A list of all sensors connected to each intelligent FRU in the system, along with any threshold or limits, is maintained via the chassis manager.
- **Sensor event log.** Although the actual log size will vary among chassis managers, it provides a history of all events such as an over temperature condition or an under voltage condition and typically will begin overwriting when the log is full, starting with the oldest event.
- **Diagnostics and recovery.** The specific VPX boards in a system, and their compatibility with VITA 46.11, will determine the level at which the chassis manager can diagnose and respond to system events.

System manager

At the top of the logical management layer is the system manager, which oversees multiple chassis and will communicate with multiple chassis managers. The system manager can be middleware, a SNMP MIB browser, custom software, RMCP, or something as simple as the ability to Telnet into a system.

The system manager is how the outside world communicates to the VITA systems via the chassis manager. Since the chassis manager supports several external interfaces via RS232 and Ethernet interfaces, many also have a built-in GUI that could be used for a lower level of system management.

The system manager provides the ability for users to remotely access the VITA 46.11 chassis to manage board inventory, and monitor the health of the boards as well as the health of the chassis and all manageable FRUs in the system.

While a VITA 46.11 chassis will typically have intelligent FRUs, such as fans and power supplies, the challenge for board manufacturers is to implement IPMCs on their boards, allowing for remote monitoring. This will further enable boards and IPMCs that support VITA 46.11 to be easily inventoried and that are monitored for health and, in some cases, the boards may be remotely reset, if necessary.

Advanced system management

As more intelligent monitoring functions are implemented into VPX applications, existing shelf management capabilities will continue to increase the effectiveness, value, and reliability of these embedded systems well into the future.

Gary Hanson is a Sr. Systems Engineer for Elma Electronic.

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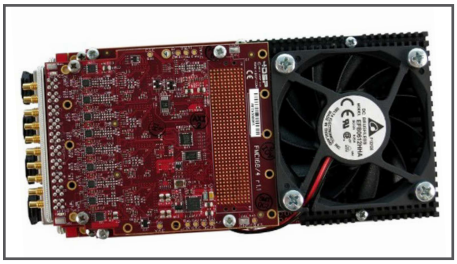

Complete data acquisition, signal processing, and storage solution

The race to improve signal processing performance and capture density is never over. 4DSP's FM788 XMC is designed to deliver performance for beamforming, direction finding, RADAR, and satellite communications. Based on Xilinx's Virtex-7 and featuring eight 16-bit A/D channels running up to 250 Msps each, its design provides the largest channel count in this frequency range and the most onboard memory for real-time buffering of large data vectors. With four 10 Gbps optical transceivers, the FM788 can be directly connected to a remote storage system without any CPU involvement.

"This approach of offering a way to digitize multiple analog channels, perform signal processing using the Virtex-7, and offload data to a storage system using optical connections on a single card overcomes the inherent limitations of bussed architectures," said 4DSP CTO Pierrick Vulliez. "The FM788 provides predictable performance in a small form factor and reduces overall system power consumption."

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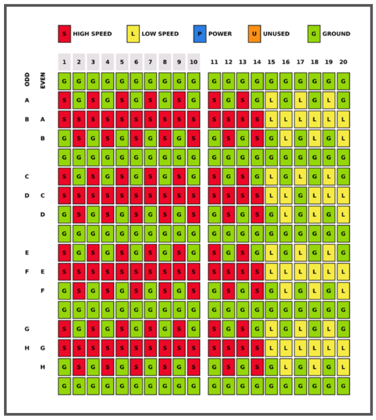
Custom designs made easy



Engineers are always looking for an edge during product design. Backplane configurations resulting in unused pins add unnecessary size and cost. Balancing performance and cost is key to successful backplane design. A new Molex online configurator tool provides that edge by quickly generating pin maps based on backplane application. The Backplane Pin Map Configurator guides users through a series of inputs to identify backplane parameters and quickly generate a pin map for their backplane application.

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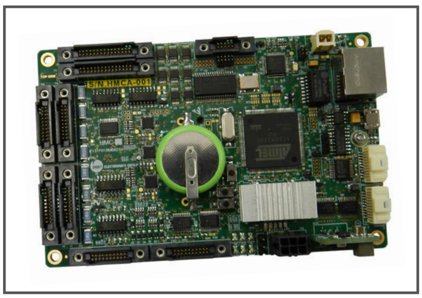

Monitoring your system's health

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The System Health Monitors provide dramatically expanded graphical user interfaces (GUIs) that enable system design engineers to quickly and easily establish a broad range of operating parameters, and monitor performance with exceptional clarity and detail.

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