COOLING … 3GPP … PICMG 2.16 MIL/AERO … VoP PLATFORMS

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APRIL 2006 VOLUME 10 NUMBER 3

Crash course?

AdvancedTCA and electron-on-positron collisions

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COLUMNS

EVENTS

Server Blade Summit – Consortium Blades
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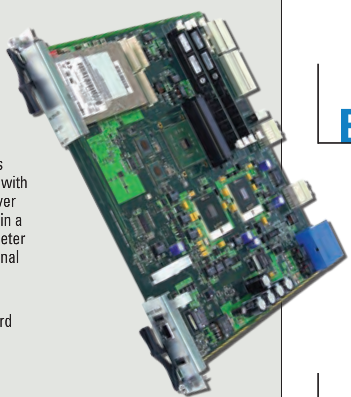

COVER:
Why the need to use High Availability (HA) electronics systems in a high-energy linear accelerator dovetails with AdvancedTCA design strengths. See page 18. The cover shows an artist's conception of one of the RF cavities in a cutaway view. The actual size is approximately one meter end to end. There are about 40,000 RF cavities in the final machine. Artwork courtesy DESY.

Photo of the ATCA-7820, an AdvancedTCA Single Board Computer, courtesy of GE Fanuc.

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By Rosemary Kristoff, Vice President Editorial

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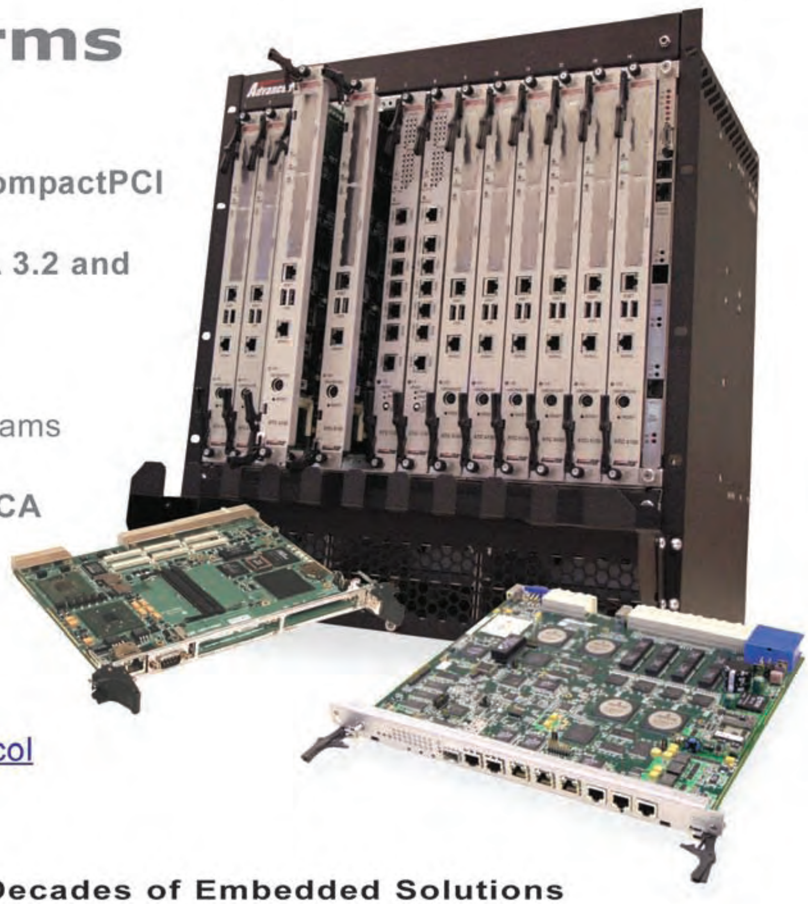

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By Joe Pavlat

Putting it all together

AdvancedTCA technology continues to gather momentum as the basis for major equipment programs at many of the world's large telecom equipment suppliers. While the standard has been out for about three years and there are hundreds and possibly thousands of product offerings, new requirements are being brought forward that promise to further shape its evolution.

Open hardware standards such as AdvancedTCA enable cost efficient infrastructure solutions but are only a piece of a larger puzzle. In order to be useful to the Telecom Equipment Manufacturers (TEMs) and Network Equipment Providers (NEPs) operating systems must be installed and configured, high availability middleware must be integrated, and the platform must be tested to some standard of usefulness. Even more basic is the need to make sense of the myriad options that exist for each one of these system elements. AdvancedTCA has literally thousands of *Shall, Should,* and *May* normative requirements. Putting working systems together by pulling pieces from multiple vendors can be a huge challenge. Defining exactly what the customer wants for a given application in terms of those normative requirements is emerging as the next important challenge vendors and customers face.

Fortunately, a number of new initiatives and organizations are emerging to tackle this problem from top to bottom. These organizations are working together closely to identify their respective goals and contributions, and to eliminate overlaps and gaps. Organizations involved include PICMG, the Service Availability Forum (SAF), SCOPE Alliance, the Mountain View Alliance, and the emerging Communications Platform Trade Association (CP-TA).

SCOPE Alliance

At the top of this chain is a new organization created to identify very high-level requirements for equipment for carrier grade applications. It is an extraordinary collection of major equipment suppliers who compete with each other in the marketplace but who are coming together to further their common interests. The founding members include Alcatel, Siemens, Motorola, NEC, Nokia, and Ericsson. Their stated goals include the definition of carrier grade base platforms that are application ready and are primarily based on AdvancedTCA. These preferred platforms will be defined through a family of profiles with detailed software and hardware requirements and descriptions. These profiles will serve as the basis for all of the work the other organizations will undertake. For more information, visit www.scope-alliance.org.

Communications Platform Trade Association

This new organization, currently being formed by industry giants Motorola and Intel, will tackle two additional pieces of the puzzle, namely interoperability and testing. CP-TA intends to further refine the high-level profiles into specified hardware and software pieces and then develop test software to determine whether or not a particular combination of elements complies with the profile being tested. The development of standardized tests can then be used to verify profile compliance, which will enable the TEMs and NEPs to lower their total development costs and encourage supplier competition. CP-TA also plans to create an independent testing laboratory in conjunction with the University of New Hampshire, which has well-established interoperability and compliance testing programs for a wide range of open industry standards.

PICMG Requirements Engineering Subcommittee

The newly formed PICMG Requirements Engineering Subcommittee (PICMG RES) sits at the bottom of the stack, feeding the layers above. The purpose of RES is to sort out all of the *Shall, Should,* and *May* language in relevant PICMG specs and create a requirements matrix that defines all of the requirements and options in an ordered and consistent way. This taxonomy, or classification language, will be used to describe thermal, power, management, data and control plane, and regulatory elements of the specifications. The initial focus will be on AdvancedTCA and the Advanced Mezzanine Card, as they are seen as crucial parts of the platforms the TEMs and NEPs are moving to deploy. In the future, related specifications such as MicroTCA and AdvancedTCA300 will likely be included in the effort. Figure 1 details some of the interaction and information flow among the groups.

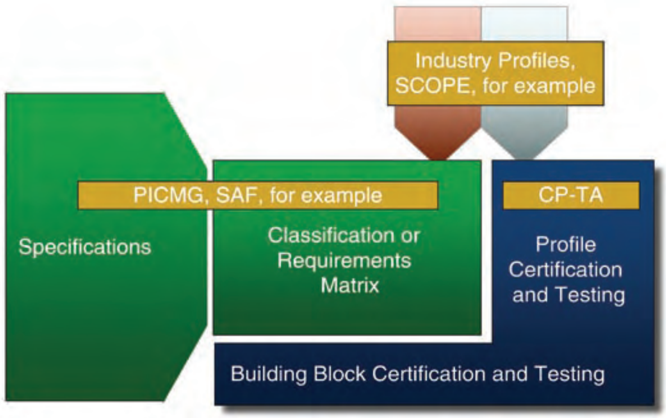

Figure 1

Mountain View Alliance

The mission of this *consortium of consortia* is to accelerate the adoption of open standards in the communications industry and to facilitate cooperation between the various standards bodies. Currently the members include PICMG, the SAF, the Network Processing Forum, and the RapidIO Trade Association. MVA has been active in reaching beyond the TEM and NEP communities to their end customers, the carriers. At a recent joint PICMG/SAF meeting Jim Sylvester from Verizon and Fred Cook from Sprint Nextel presented carrier perspectives and requirements for open platform standards, including AdvancedTCA. Their insightful presentations and additional overviews of SCOPE and PICMG RES can be viewed at www.mountainviewalliance.org.

Joe Pavlat
Editorial Director

By Curt Schwaderer

IP vendor offers voice over packet application platforms

The trend toward integrated software capabilities and programming interfaces for hardware platforms has found its way into System-on-Chip (SoC) design. For example, CEVA, an intellectual property company licensing DSP technology to a number of companies in a variety of markets, has recently introduced a Voice over Packet (VoP) application environment called CEVA-VoP. Interestingly enough, the core to this application platform is not a board-level design. Instead, the core of the application environment leverages CEVA DSP core intellectual property to create SoC designs targeted for items from IP phones and dual mode cellular over Wi-Fi products, to larger products such as home gateways and Voice over Internet Protocol (VoIP) broadband equipment. I recently had the opportunity to talk with Moshe Sheier, spokesperson for CEVA-VoP. We talked about how software trends are influencing SoC providers such as CEVA and new software and application innovations from CEVA to address these demands.

VoP platform overview

CEVA is a licensor of DSP cores with more than 115 million chips shipped with CEVA cores in 2005. Their DSP cores are widely used in cellular, DVD, disk drives, and consumer electronics.

In addition to a large portfolio of DSP cores and related subsystems for SoC products, CEVA has added platforms in multimedia, audio, GPS, and storage solutions.

One of those platforms is the CEVA-VoP platform. The product is a fully integrated, single DSP-based VoP system ready for integration into SoC designs. There are four main components to the platform:

- SoC and software interface framework
- Hardware
- Software
- Toolset

The hardware platform itself is available in two different configurations: *voice processor* configuration and *voice + networking processor* configuration. The voice processor configuration supports up to eight channels of G.729AB voice, telephony, or packetized data with tasks that interface with a host processor. This configuration is targeted for applications that will use a network processor function as the incoming/outgoing network interface and a host processor to provide signaling and management functionality. The *voice + networking processor* configuration provides a solution that can offload or even eliminate the need for host and network processing functions, which can dramatically reduce the cost of gateway and VoIP phone applications at the cost of fewer payload processing channels provided by the voice processor configuration.

The software solutions with the platform include:

- ITU-compliant G.7xx suite of voice encoder/decoder algorithms and echo cancellation (G.168-2000) for the DSP core
- UDP/IP stack network protocols
- Real-time Transport Protocol (RTP) packetization
- Operating kernel used as the framework for the software
- Session Initiation Protocol (SIP) signaling stack

These components work together to provide network interface, signaling, and content processing functions for the platform.

VoP: A closer look

Figure 1 shows the CEVA-VoP platform architecture. The blocks in light blue are the voice plus networking components. The blocks in the dark blue are the voice processing components, and the green blocks represent the external interfaces.

The two external interfaces are the network interface itself, which is an Ethernet MAC connected to a LAN either directly or through a Layer 2 switch. The other interface is the Subscriber Line Interface Circuit (SLIC), which carries the Time Division Multiplexed (TDM) channels between the application platform and the ultimate input/output destination(s) of the payload carried within the channels.

The VoIP circuit and software is designed to handle up to eight channels of G.729AB voice codec channels simultaneously at a power of approximately 20 mW. More specifically, each channel consumes 0.1 mA/MHz per channel.

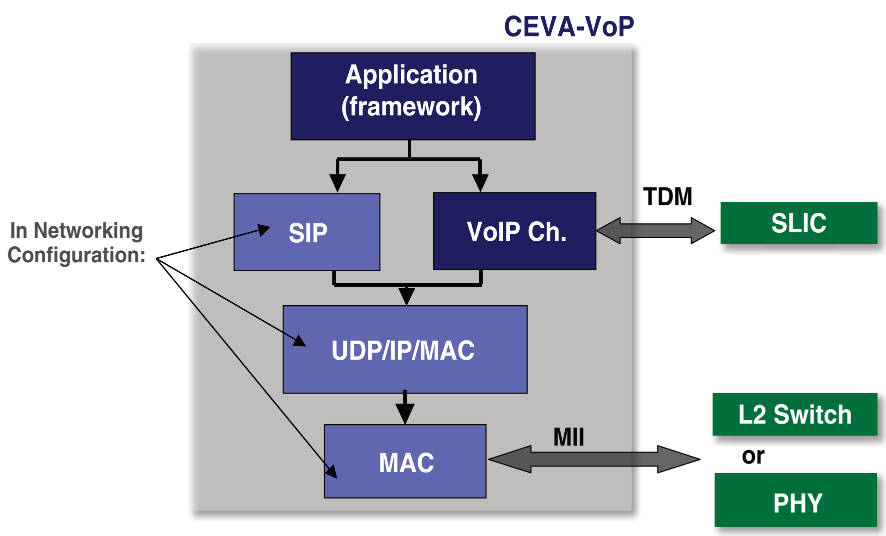

Figure 1

nel operating at 25 MHz multiplied by eight channels, that totals 20 mW. Within the voice-only engine configuration, the system can be set up to provide eight G.729AB voice channels with telephony and RTP processing. Another common configuration includes six G.729AB channels with two T.38 fax channels in addition to the telephony and RTP processing.

The voice plus networking engine provides the same configuration, but adds UDP/IP and SIP signaling to the configuration. The additional network and signaling processing will limit the number of channels that can be supported. Exactly how many channels are supported depends upon the application's call setup-per-second characteristics as well as the amount of UDP/IP traffic coming into the system.

The application software framework provides a set of application programming interfaces to configure the voice processing in addition to getting basic statistics and signaling control interfaces to the environment. The framework is written in C/C++ and can be ported to the host processor's operating system environment.

SIP signaling and UDP/IP packet processing functions can also be performed within the environment if a front-end network processor and/or a host processor is not needed for the application. This increases the processing and bandwidth utilization on the DSP, so fewer channels are supported, but at the same time, the SoC subsystem becomes quite a combination networking, signaling, and voice processing machine.

The uniqueness of SoC

One of the things I found fascinating while talking to Moshe about the CEVA-VoP platform is the range of software and tools support needed to provide a SoC application environment for today's customers. The software ranges from C/C++ programming interfaces, signaling, and networking software to DSP assembly codec and payload processing and verilog for the DSP and component subsystems themselves. Therefore it's no small undertaking to provide a fully validated and integrated SoC solution.

Starting with the silicon intellectual property, the CEVA-VoP hardware intellectual property package contains the following elements:

- Fully verified synthesizable verilog code
- RTL to GDSII complete and robust design flow with scripts for mainstream EDA tools
- Verification and simulation environments for verification of the IP integration in the target SoC
- RTL on FPGA for system prototyping prior to silicon fabrication

The IP integrator combines the top level CEVA-VoP verilog block into the SoC design, while using the AHB/APB bus interfaces to connect to the host CPU and system memory, and on the other side the TDM ports to the subscriber line interface (SLIC/SLAC) modules and into the RJ-11 telephony ports. The integrator uses supplied test suites to validate the IP integration following completion. Once validated, the physical implementation (synthesis and place and route) is initiated to form the complete GDSII view for fabrication.

VoP development environment

Figure 2 shows all the different kinds of languages and environments that go into the single Integrated Development Environment (IDE). The myriad of tools and capabilities under one integrated environment allows complete software development from verilog integration, DSP algorithms, and C/C++ interface library interfaces for the platform.

> "The voice + *networking processor* configuration provides a solution that can offload or even eliminate the need for host and network processing functions…"

The set of DSP algorithms includes:

- Voice encoding and decoding for G.711 64 kbps A-law/m-law Pulse Code Modulation (PCM)
- G.726 40/32/24/16 kbps ADPCM
- G.729A/AB 8 kbps CS-ACELP
- G.723.1/A 6.4/5.3 kbps MP-MLQ/ACELP

An adaptive low delay jitter buffer helps minimize data loss and delay through the platform. There is also a unique three-way conferencing capability in the algorithm that allows mixing of two audio sources on one side into one combined signal on the other side.

Telephony features include:

- Tone generation and detection
- Fax/modem detection
- Automatic volume level control
- Caller ID

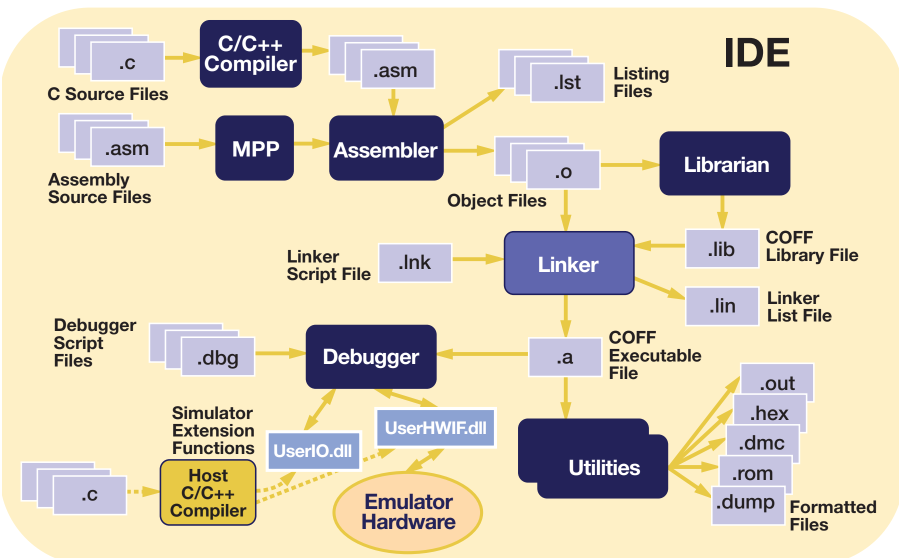

Figure 2

- Call waiting
- Error mitigation/bad frame interpolation
- Host and TDM interfaces drivers

The CEVA software development tools consist of an IDE, a C/C++ Compiler, macro preprocessor, assembler, linker, debugger, and several utilities. They aim to provide an efficient, user-friendly environment for application development. The development tools run on Windows, Linux, and Solaris platforms. The macro preprocessor, assembler, Linker, and C/C++ Compiler are part of the code generation tools, as they build executable code from either C source code or assembly source code.

Once the code has been developed, the IDE includes a graphical debugger as well as simulation. The GUI debugger supports generation and execution for command line and TCL scripts. The debugger can interface to popular verilog simulators as well as emulator interfaces through USB or JTAG ports.

The entire IDE, simulators, and profilers for the DSP software are implemented in C/C++. Low-level DSP assembly with C/C++ level APIs are also provided for external software interface. Moshe mentioned that development tools and an integrated environment are key to the development and customer selection process, so CEVA has developed all its tools internally. The benefit of this approach is that the tools can be tuned for their intellectual property and target applications.

Once the code is developed and debugged using the debugging and simulation environments, an application profiler is also provided to determine performance metrics for the application.

Control and management plane considerations

Typically, the CEVA VoP platform might be integrated with SIP signaling and network management software such as Simple Network Management Protocol (SNMP) to provide an SNMP-managed device. These components would typically run on a separate control and management plane processor and use APIs to communicate to the VoP platform components as well as gather statistics. These functional APIs include things such as call initiation and termination, opening packet streams, specifying DMA channels and memory locations for each voice circuit, and control activities relating to the SIP call control protocol.

We also talked a bit about the Communications Assistance for Law Enforcement Act (CALEA). This involves VoIP systems' ability to support lawful surveillance for law enforcement and homeland security. Similar to the control and management plane functions, these activities would also be controlled from a separate host processor and control the routing of the voice channels through the APIs provided.

Conclusion

SoC designs require a wide variety of software from verilog to assembly, to C/C++ and Java in order to achieve the integration level today's multimedia applications demand. The CEVA-VoP platform is a good example of the next generation of integrated hardware and software intellectual property solutions supplied for the creation of these kinds of applications. Targeted at home gateway (two to eight channels) as well as VoIP phones (voice and cellular over Wi-Fi), it also provides a good example of the flexibility that must be incorporated into a successful SoC platform.

For more information, contact Curt at cschwaderer@opensystems-publishing.com.

By John Meredith

Voice call continuity in 3GPP

Voice call continuity requires maintaining a voice call when a mobile terminal moves from one cell to another for second generation Global System for Mobile Communications (GSM) digital cellular communications systems. Operational for many years, this technique enables a conversation to continue when the Circuit-Switched (CS) call reroutes to use a new basestation as the mobile moves from one coverage area to another. The parties will perceive no break whatsoever.

Today, the scenario is rather more complicated, with calls being handed over not only from 2G to 2G cells and from 3G to 3G cells, but also between 2G GSM and 3G Universal Mobile Telecommunications System (UMTS) cells. This is relatively easy from an administrative point of view, given that generally the same cellular network is involved throughout.

Earlier work carried out within the 3rd Generation Partnership Project (3GPP) envisaged telephony using packet-switched connections – Voice over Internet Protocol (VoIP) – using either the 3GPP-defined IP Multimedia Subsystem (IMS) on the 3G Universal Terrestrial Access Network (UTRAN), or Wireless Local Area Network (WLAN) radio access technology based on IEEE 802.11, and other standards. This was covered by the WLAN interworking work items.

However, until now, handover between CS and IMS (packet-switched) calls was not addressed. 3GPP is now investigating the problem of handing over a voice (or potentially video or other multimedia conversational service) call between the cellular network and a WLAN, possibly operated by a completely different service provider. Again, for conversational service, the handover has to be seamless, with no break in service perceived by either party to the call. Until recently, such handover had only been considered for services that are not real-time, such as file-transfer, where short breaks during the handover process are acceptable and probably go unnoticed by the user.

The approach taken by 3GPP is to have the WLAN operator use the information registered by the home operator for the mobile terminal subscriber in this sequence:

1. Validate the eligibility of the handover to happen at all
2. Manage charging for the call that is effectively transferred from one network operator to another

It is generally, though not necessarily, the case that WLAN hotspots are also well covered by cellular service. Thus, such handover may take place when cellular coverage is reduced to an unacceptable level, yet an adequate WLAN hotspot service is available. The handover is more likely to occur when spare bandwidth exists on the WLAN but where excess demand for cellular channels exists.

The goal is to maintain the conversational service call, thus optimizing the service to the users, which in turn will maximize the revenue accruing to the operator(s). 3GPP embarked on the technical activity required to enable this service by approving a work item on Voice Call Continuity (VCC) in the June 2005 meeting of its Technical Specification Group *System Aspects and Architecture* (TSG SA). In order to be accepted onto the 3GPP work plan, any work item needs to have the support of at least four supporting member companies, and no sustained opposition. The VCC work item has no fewer than 16 supporters, and its progress can be tracked on the 3GPP website, www.3gpp.org. It is intended that this work be achieved in the Release 7 time frame.

A prerequisite of VCC is cooperation between the home network IMS and the WLAN operator. Given this prerequisite, an added bonus is that the VCC handover mechanism should be applicable regardless of the precise nature of the radio, or even wireline, access technology. For example, wireline *IMS over Internet* or radio *IMS over General Packet Radio Service (GPRS)* could replace WLAN, and the same basic mechanisms should be at work.

As if this were not complicated enough, due regard must be taken to security issues as they apply to GSM/UMTS CS calls, WLAN access, and IMS.

Feasibility study

The work item was immediately approved, and 3GPP TSG SA working group 2 started work on Technical Report (TR) 23.806. This TR would contain the result of an architectural feasibility study into the possible approaches to VCC. Approximately 150 pages, the TR was approved at the TSG SA meeting held December 5 to 7, 2005 in Malta. Although the TR is considered complete, working group members identified several points requiring detailed resolution during the ensuing specification work. Among these were further consideration of whether supplementary services would be best supported centrally or distributed among the cooperating networks, and the possible interactions with Customized Applications for Mobile network Enhanced Logic (CAMEL) services. The TR identifies several possible approaches, but participants narrowed the options down to two techniques dubbed *Original Domain Controlled* and *IMS Controlled Static Anchoring*. The pros and cons of each will be determined during the detailed specification phase.

Technical specification

The service requirements as perceived from a user's point of view are essentially identical to those for existing voice calls, so no new Stage 1 specification is needed. However, some aspects of the effects on, for example, charging and supplementary service operation need to be documented. So far, seven change requests to the Stage 1 specification TS 22.101 have been approved. Most technical specification work will be captured in a Stage 2 (architecture and functional information flows) specification. A draft has been prepared for this specification, TS 23.206, and it is envisaged that several existing Stage 3 (detailed function and protocol) specifications will be modified to cater for the required signaling. Generally, the group agreed that this signaling should be minimized in order not to place an excessive burden on the two networks during the handover process and also to keep to an acceptable level the capability negotiation between terminal and network as the mobile unit moves in and out of service coverage, which may be different for CS and IMS service.

Meanwhile, detailed architectural discussions are taking place in of SA working group two, largely via e-mail. A couple of dozen VCC enthusiasts exchange an average of approximately 20 e-mails daily to thrash out solutions to the open issues.

The companies most active in the discussions represent a wide geographical spread that includes Europe, North America, and Asia and encompass both equipment providers such as Motorola, Ericsson, Nokia, ZTE, Lucent, Nortel, Huawei, Siemens, and others, and network operators such as Vodafone, Cingular, and others.

CAMEL

The VCC concept relies on CAMEL functionality (3GPP TS 22.078, TS 23.078, 29.078). Refer to TS 21.978 for a feasibility study of VoIP support via CAMEL. Presently, no alternative mechanism is envisaged. From the standardization point of view, minimizing the number of options is a good thing. However, it is a fact of life that there are mobile networks in the world that do not support CAMEL. If this state persists, then VCC implementation would obviously be adversely affected.

Network domain selection

Probably the major topic that has exercised the engineers has been the consideration of the Network Domain Selection (NeDS) function, and where this function should best be situated. This function is the point where the decision is taken to deliver a call either in the CS domain or in the IMS domain. While it is logical for a call that was originated in the CS domain to remain CS end-to-end, and similarly for an IMS-originated call to remain IMS throughout, there are circumstances when a change of domain is appropriate. Apart from technical issues, there are the questions of terminal capability, whether or not the destination terminal is already CS-attached or IMS-registered, and not least the preference and subscription options of the terminating user. Although the feasibility study identified many of the issues to be examined, by its nature, it provided very little in the way of concrete answers.

NeDS functionality has been conceptually split into two:

- Functionality required to determine whether an incoming CS call should be routed to IMS
- Functionality required to determine whether a call currently in the IMS should remain in IMS or be transferred to CS

The current mindset is that the first area need not be standardized, but various techniques might be described in an informative annex to the standard. For the second area, several possibilities are being discussed, though it is not proposed to have a standardized reference point. This implies that, when it comes to writing Stage 3 specifications, signaling is also likely to have at least some proprietary element. The NeDS entity will interact either with the Serving Call Session Control Function (S-CSCF) or with the Call Continuity Control Function (CCCF) (refer to TR 22.806), implying the use of either IMS Service Control or Diameter. Part of the thinking behind the placement of NeDS is whether or not it may one day be desirable to support VCC in pre-Release-7 networks. That is, VCC effectively becomes release-independent.

As is often the case with abstract architectural discussions, there is a tendency to map functionality onto known or envisaged physical boxes. After all, the implementation will be in equipment manufactured and sold to operators, not in ethereal clouds in Stage 2 specifications. The trick is not to start this mapping process too early, to allow correct functionality to be specified in advance of detailed considerations of marketable products. It is clear that a great deal of work remains to be done on this topic before the TS can hope to reach stability. Nevertheless, time scales are aggressive, and the target is to have all the major standardization work completed by June 2006.

This column has touched upon some of the current considerations of the VCC work currently unfurling in 3GPP. A more detailed review can be found via the VCC exploder list digest. While participation in the 3GPP meetings is limited to 3GPP member organizations, anyone may join exploder lists and contribute to discussions. To join, visit www.3gpp.org/email/lists.htm.

For more information, contact John at john.meredith@etsi.org.

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By Hermann Strass

European test and measurement applications

European business

Kontron, Germany, reports good business in 2005. More than 2,300 employees have contributed to sales of close to € 300 million (approximately U.S. $375 million). They claim an average of 20 percent growth annually since their start as a spinoff from BMW in 1999. Systems (41 percent) more than modules/boards (33 percent) is their main business. The global orientation of Kontron is reflected by company locations in Germany (headquarters), Canada, China, Russia, Taiwan, and the United States. Tailor-made solutions for their customers require that approximately one third of their workforce are dedicated to research, development, and engineering. No customer has more than 5 percent of Kontron's sales.

European applications

Acqiris, (Switzerland), uses their AC240 signal analyzer in an FFT spectrometer, which is a great step forward in speed and capabilities over previous systems. In the past broadband spectrometers for millimeter waves were mostly based on acousto-optical design (diffraction of coherent light), which is very limited in stability, dynamic range, and cost. Digital techniques using hard-wired registers were limited in bandwidth. The large bandwidth FFT spectrometer from Acqiris on a 6U CompactPCI or PXI card uses an FPGA for the FFT core. The two 1 GSps ADC converters can be interleaved to form a 2 GSps converter. Multiplications with 36-bit results are done in less than 5 ns by any of the 328 dedicated multipliers inside the FPGA. This powerful computation engine needs only a maximum of 73 W to accomplish its high-speed FFT analysis. Similar boards are available for 3U PXI applications. The DC140 and DC135 with up to 2 GSps versions consume less than 16 W when using 16 Mpoints of onboard memory.

Rohde & Schwarz (R&S), Germany, one of the global leaders in test and measurement equipment, is using CompactPCI boards from Kontron for its CompacTSVP test platform. Figure 1 is a board from their CompacTSVP test, measurement, and analysis CompactPCI-based system. The increasing need for flexibility in Automatic Test Equipment (ATE) demands a flexible modular system design. The CompacTSVP system from R&S can be configured with CPU boards from Kontron, test and measurement boards from R&S, Special PCI (SPCI) or PXI, and possibly boards from other vendors to customize and optimize a system for specific customer requirements including rear I/O capabilities. In ATE applications mass plug connections, including typical PC cabling for such items as monitor, keyboard, and mouse are lined up and locked on these rear extension boards. Windows for general and Linux for industrial applications support the ATE systems from R&S. Variants of these CompacTSVP systems are available for the extended temperature range E2 (-40 °C to +85 °C).

European products

Polyrack, Germany, has launched a new series of CompactPCI enclosures with microprocessor-controlled monitoring of system components (fans, voltages, AC-failure, temperatures, and AUX-I/O pins). Remote operation via Web interface or RS-232 are also implemented. Cards are placed horizontally, making it possible to insert hard disks adjacent to the CompactPCI boards in the 19-inch wide racks (1U with two CompactPCI slots or 4U with eight slots). A similar card cage (4U) is also available for VME64x applications. CompactPCI backplanes with integrated packet switching according to PICMG 2.0, 2.1, 2.9, and 2.16 are available for these card cages.

SMA, Germany, has a Cool Box to reduce the average temperature inside the box significantly and therefore increase Mean Time Between Failure (MTBF) dramatically. According to the Law of Arrhenius, MTBF is cut in half for each increase of 10 °C (18 °F) in operating temperature. This is an important factor in so-called *fanless* systems, which typically operate at very high temperatures especially at a CPU load close to 100 percent. Baffles guide the filtered air bottom to top in a 4U CompactPCI box. A CD-ROM or DVD drive can be mounted in addition to CompactPCI cards. When used in road vehicle applications a shock-protected hard disk can be integrated into the Cool Box. SMA was awarded second place in the German government-sponsored contest *Great Place to Work 2005*, reflecting how SMA employees like their place of work.

For more information, e-mail Hermann at hstrass@opensystems-publishing.com.

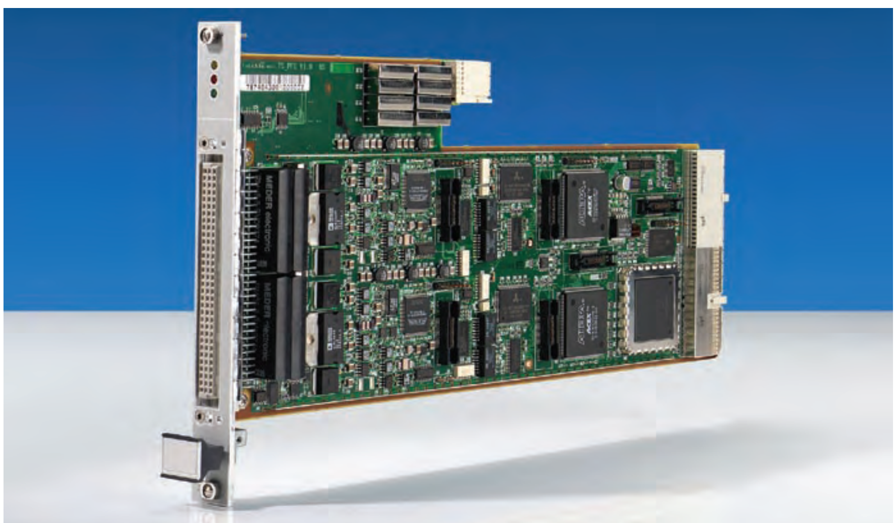

Figure 1


EMBEDDED PLANET

Crash course? AdvancedTCA and electron-on-positron collisions

By Robert Downing

Large particle accelerators in the world have been colliding electrons and protons together for many years. Each set of experiments has answered questions and raised new ones. To probe the new questions has led to ever more powerful machines. The latest high-energy accelerator at the CERN high energy physics laboratory in Europe, the Large Hadron Collider or LHC, is under construction and will start operation of the next generation of proton-on-proton collisions in 2007, reaching the astounding energy of seven trillion electron-Volts (TeV) per proton. In this article Robert explains why the need to use High Availability (HA) electronics systems in a high-energy linear accelerator dovetails with AdvancedTCA design strengths.

To probe deeper into questions about the fundamental building blocks of nature with much finer resolution beams, a large electron-positron machine is being proposed. In a project known as the International Linear Collider (ILC), a collaboration of physicists from all over the world is in the early phases of designing a high-energy linear accelerator to study the properties of the fundamental building blocks of nature. This group is striving for a base line design later this year. From this a first cost estimate will be extracted.

As accelerators have become more and more complex, serious issues have come into play concerning both bringing accelerators into operation and keeping them operating. In the case of the ILC the cost of downtime may be as high as $150,000 per hour. One obviously needs reliability, yet the number of parts that have to be functioning at one time makes the MTBF for these components unreasonably large. Therefore the solution is one with practical MTBF along with HA design of the electronics.

The proposed machine is to be built in two stages. In the first stage there are two approximately 10 kilometer tunnels, with a 250 GeV electron accelerator in one and a 250 GeV positron accelerator in the other, for a 500 GeV collision energy (1 GeV = 10^9 electron volts). The design must be extendable in the future to a collision energy of 1 TeV. The accelerators are pointed at each other, and electrons and positrons collide in one or two large detectors installed in the middle. By analyzing the data from these collisions physicists will be able to further probe the fundamental properties of the elemental particles that make up everything.

In addition there are so-called Damping Rings that are necessary to tightly focus and stabilize the electrons and positrons before sending them to the main linear accelerators that will boost them to their final energy. The overall length for the 500 GeV machine, including the experimental areas, is about 30 kilometers. During the second stage each of the two *linacs* will grow to about 20 kilometers resulting in an increase in energy to 500 GeV for each machine or 1 TeV collision energy. The overall length of the site becomes about 50 kilometers. Figure 1 schematically shows both configurations.

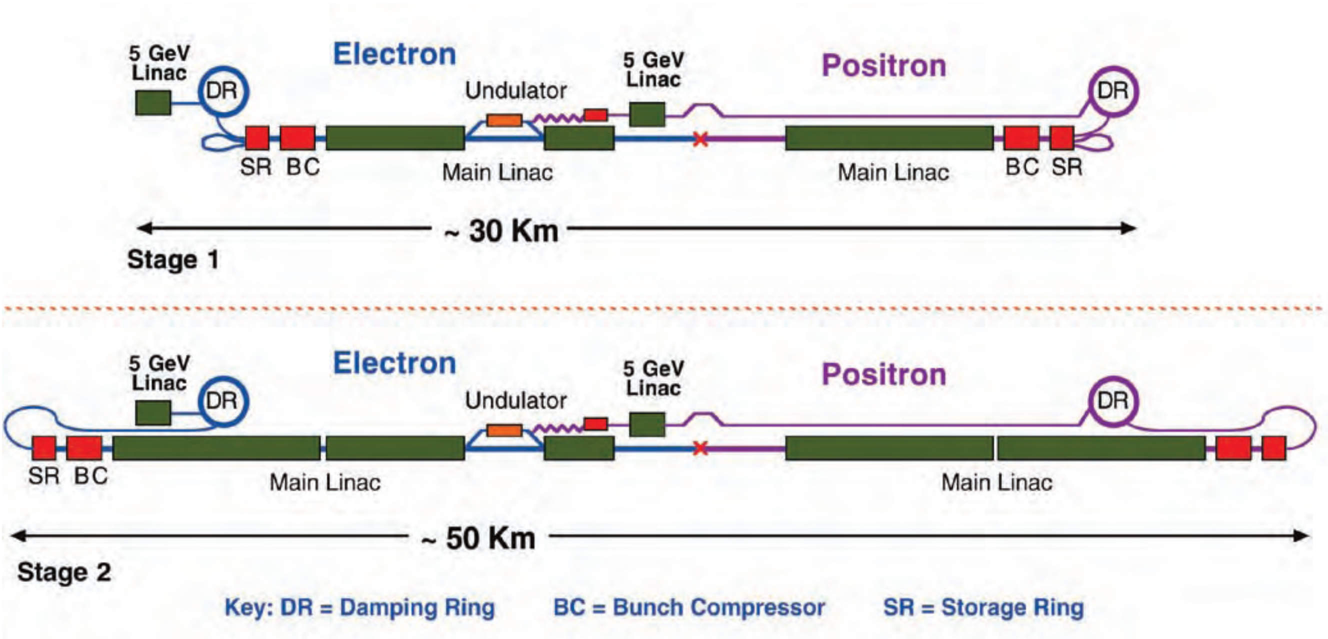

Figure 1

So what does this have to do with AdvancedTCA?

The controls and instrumentation for this machine constitute an enormous amount of electronics. If one uses an AdvancedTCA board size for estimating hardware just along the main linacs at one AdvancdTCA module per meter of machine with four daughter cards there would be 25,000 AdvancedTCA modules and about 100,000 AdvancedMC cards. The operational goal is to have a minimum of 85 percent uptime. An availability model of the entire machine showed that this was completely unachievable with standard design approaches of current machines unless HA design approaches are used for all electronics systems, employing both 1/n redundancy and hotswap features.

With the minimum 85 percent uptime goal in mind, ILC engineers are striving to develop a fault-tolerant design that will not cause an interruption in operations due to single-point failures. This presents both a hardware and a software challenge, as well as a severe challenge to design for cost as well as HA. ILC designers are looking to industry for a standard solution. AdvancedTCA seems to fit the requirement of high availability for controls and instrumentation.

The telco need for 5-nines is in line with the availability requirements for the ILC central core of the control system. How adaptable AdvancedTCA might be for the customized applications along the accelerator is an open question that will be evaluated aggressively over the next couple of years.

Possible AdvancedTCA configuration

Figures 2, 3, and 4 show the AdvancedTCA topology for just the main linac control. There are similar control systems for the damping rings, small linacs, bunch compressors, and so forth. Figure 2 is the top level of the control system. Data is collected here for the entire machine, and overall corrections are sent down to the various sections.

Figure 3 shows the hardware at the sector level. A sector is about one kilometer in length. The dual star network on the left side of the diagram connects the Level 2 nodes to the Central Control in Figure 1. Figure 4 is a typical RF of which there are about 400 in each of the first stage linacs. Data flows from the sensors in each RF Unit into a local computer where a fast correction calculation is made to adjust

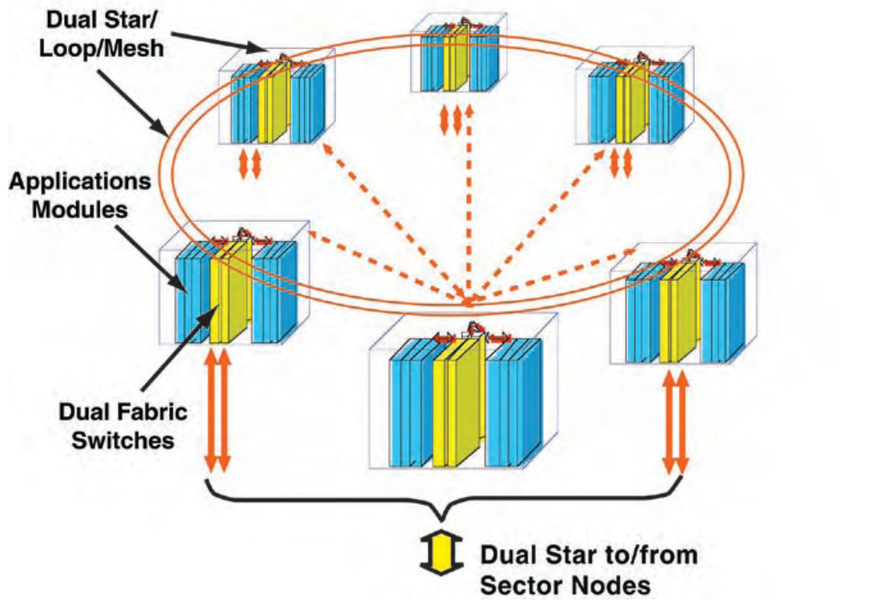

Figure 2

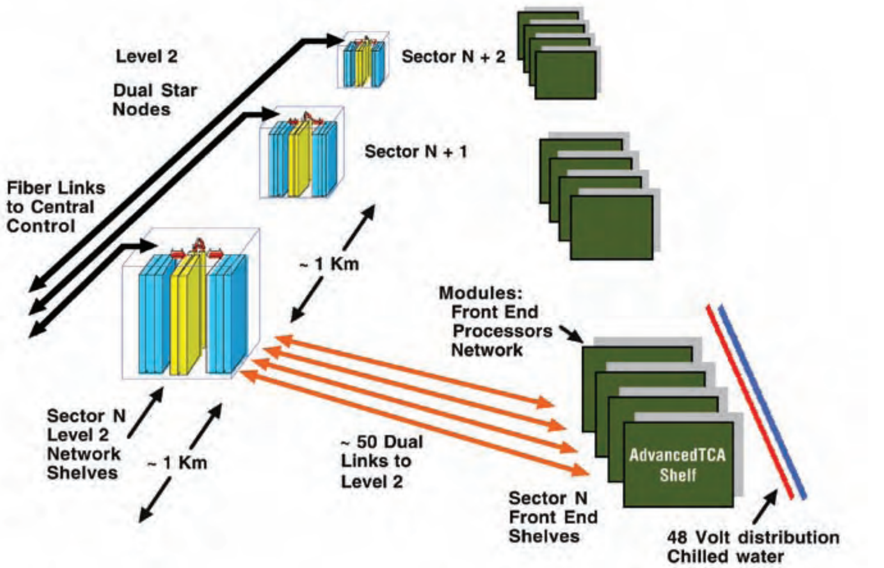

Figure 3

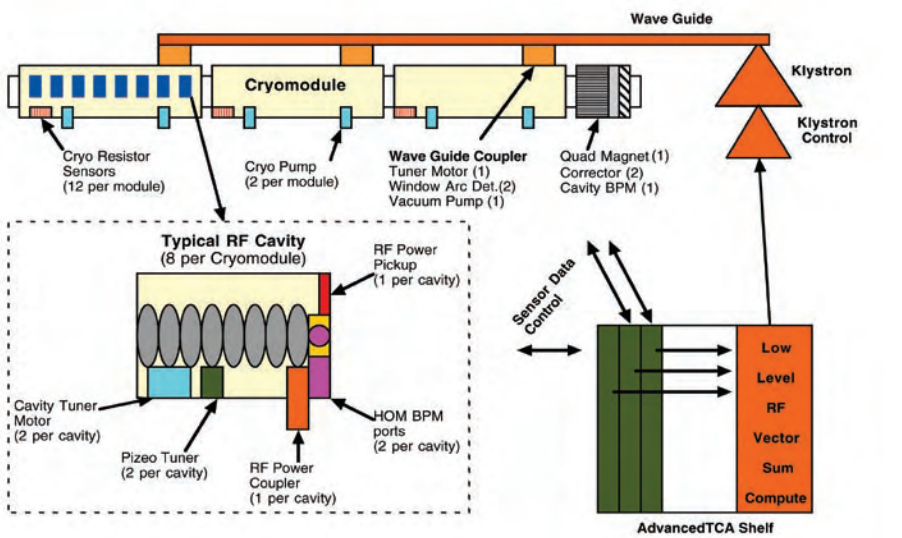

Figure 4

the steering of the electron beam. The estimate given previously is based on the equivalent of one AdvancedTCA card per cavity that is shown in Figure 4. A few more modules that control the klystrons and other hardware will be in the RF Unit shelves.

Another difficult problem for the ILC is its large geographic area – as much as 50 kilometers end-to-end in the final configuration. One must design to have as much information as possible on the health of the various systems at the machine control center in order to intelligently schedule maintenance. Also, knowing exactly which modules have failed or are showing signs of failure enables rapid hot swapping if necessary to prevent machine interruption. Here again, AdvancedTCA offers the features to implement such a scheme.

The AdvancedTCA design philosophy can be used in other components of the ILC. For example, large power supplies can be designed to be modular with 1/n redundancy so that when a sub-unit fails the entire supply does not go down. The shelf management features in AdvancedTCA can also be adapted in non-AdvancedTCA hardware. The large power supplies in the example could use the AdvancedTCA shelf management for such activities as monitoring voltages, current, and temperature, and switching out a failed section. One could connect to the same AdvancedTCA network. There is a big advantage from a management perspective to have a uniform system. Training and maintenance become much easier. The spares inventory is reduced. And, engineers can be diverted from not-invented-here projects into much more useful enterprises.

The ILC electronics wish list

What else might the ILC like to have? Given a shelf monitoring system that can effectively diagnose problems and the machine's very large geographic extend, one could envision a robot in the tunnel changing many of the modules. There would be some slight modification in the AdvancedTCA module to accommodate the robot's *fingers*. This would improve availability and lower labor costs. The robots would work 24/7 and always be on call. Technicians and engineers would only be sent out on long trips for complex issues that could not be fixed by swapping hardware. This feature should be of interest to other industries that deal with a majority of their electronics failures by swapping out modules.

Robotic servicing also demands cabling at the rear, as front panel cabling would add complication and be a source of failure. Front panel cables are also a proven source of errors when humans service electronics. Experience has taught us that all cabling should be in the rear to avoid misconnections or damaged cables and/or connectors. With the increased use of fiber this could be an even more serious issue involving such factors as contamination in connectors and overbend cracking. As a crosscheck, the

modules, shelves, and any other robotic serviced hardware should have a machine-readable feature the robots can use to confirm the module type and location.

Fluid cooling interests engineers who will be working on the ILC's electronic design. Chilled water removes all heat generated, about 250 MW total, from the tunnels. Eliminating cooling fans would remove another interface and improve reliability. All high-powered components will already by cooled by water, so the AdvancedTCA can take advantage of this infrastructure. If one assumes the hardware estimates made earlier, that comes to at least 2,000 shelves just along the main linac. With four fans in each and a 50,000-hour MTBF, six to seven fans would fail every day. (Note that the calculation does not account for age effects, which skew the failure time distribution.) Since the mission time is nine months of the year of 24/7 running, or about 6,000 hours continuous, eliminating fans in the tunnel is very attractive.

Fiberoptics is a third area of interest. ILC data has to be sent both long distances and through a noisy environment. We believe that fiberoptics will be the major communication technology. We would hope that AdvancedTCA develops some standard fiberoptic connection protocols, connectors, and the like, all of which can be blind mated at the rear of modules.

Finally, the topology of the machine will dictate the instrumentation topology. In some areas the standard shelf will not adapt without introducing a large, cumbersome, and expensive cable plant. For these cases the designers will explore more distributed modular architectures where smaller MicroTCA sized modules are placed as close as possible to the beam pickup and RF signals along the machine. The only downside to MicroTCA is our requirement that all connections be from the rear of any electronic modules so no cables are disturbed when modules are swapped.

What is the R&D plan?

Until the final design is set the various ILC electronics control groups will be evaluating AdvancedTCA. Several of the groups have purchased starter kits and are in the process of evaluation. Some signals from the ILC are low-level analog. One would like to have as much electronics on one board type as possible to reduce the hardware variants that have to be maintained. We will be testing to see if those signals can cohabit with the digital traffic and other potential noise generated in the AdvancedTCA shelves and modules.

From the mechanical side we will start to investigate fluid cooling, robot servicing, and fiberoptic hardware. Our hope is that these issues will be picked up and studied by the AdvancedTCA subcommittees and become part of the overall standard. Our goal is to avoid proprietary hardware as much as possible.

What is the time scale?

The first milestone (Figure 5) is a Reference Design by the end of 2006 with preliminary cost estimates. This will be derived from the 2005 Base Line design. Next will come a Technical Design with a more detailed design and better costs. Starting in 2007 countries that would like to host the project will indicate their interest. By the end of 2009 the goal is to have a final design and an approved project that can move to construction. All along this process an R&D program will evaluate and test design options. Also, as technology improves this program will adopt design upgrades to improve the machine and lower the cost. The current estimate for construction time is five years. This means that the first research data would appear in 2015.

For the AdvancedTCA vendor this schedule means that small prototype systems will be required until the construction is approved. Some joint development projects will probably be initiated. It also means that the ILC will track technology during the design phase, only hardening the specifications at the latest practical time. This will ensure that the electronics will have the best lifetime and be as current as possible. After that, production quantities will ramp up over the construction cycle, peaking in the last few years as inventory builds and installation commences. The anticipated quantities of shelves and modules will be more firmly estimated over the next year or two. The estimated value of the total controls and instrumentation hardware and software installed in the system will be in the order of several hundred million dollars.

Robert Downing *has his own consulting company. He has been doing work on high-speed data acquisition systems for Fermi National Accelerator Laboratory. Currently he is consulting with the Stanford Linear Accelerator Center (SLAC [1]) on the proposed new International Linear Collider. Bob has worked on standards committees for electronics over the last 30 years beginning with the National Bureau of Standards NIM Committee. He is the past chair of the VME Standards Organization and currently working with PICMG through his SLAC contract.*

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Acknowledgements

[1] The author would like to thank Ray Larsen at SLAC for his excellent comments and suggestions for this paper.

linearcollider.org

picmg.org

Figure 5

AdvancedTCA cooling design from concept to maintenance

By David Wright

In this article David uses AdvancedTCA as the main example in a discussion of approaches to high-power cooling problems. The methods described are equally applicable to any high-power cooling problem, whether custom designs or based on other open shelf specifications or standards.

Over the past few years, silicon – and as a result – board power densities have increased significantly. When PICMG released the AdvancedTCA specification with a maximum allowable board dissipation of 200 W, the industry saw this figure as at the extreme. Now four years later, with some boards dissipating up to 250 W, this figure has increased to a 400 W limit. At this level, a 16-slot system could be running at 6 kW (allowing a further 400 W for fan power). This is a considerable amount of heat to move out of the shelf and out of the office.

Different cooling techniques available

Among the cooling techniques available are convection and forced air cooling, cooling through solid interfaces (normally referred to as conduction cooling), and through different liquids called, obviously, liquid cooling. This article focuses on forced air cooling, which is still the most common approach for high-power systems.

The difficulty of moving the heat out of the rack and office is one problem. The need for high-power fans results in increased acoustic noise. Managing that noise is an additional problem. It is generally accepted that the acoustic noise limits can only be met by a shelf running under ideal conditions. Typically ideal conditions would be at an ambient of 25 ºC to 30 ºC with all fans operational. Acoustic noise is a function of air movement and can be reduced by ensuring that each FRU receives only the air needed for cooling, and little more. Excessive airflow is noisy in itself and requires more work, hence more noise, from the fans.

A custom system product can meet the challenge of high- power density during the design phase. The designer has full control over all the cooling parameters and can ensure that heat fluxes are balanced and adequate cooling air is provided where required. A problem might occur when one introduces a new function involving a board change. The new boards may well have different cooling demands, and this changes the hardware cooling parameters.

AdvancedTCA is an open specification designed to provide systems implementers a rapid time to market and a minimum development cost. To meet this aim the specification has significant thermal solutions built in. It is not the purpose of this article to repeat these requirements. Readers should see section 5 of PICMG 3.0 r2.0ECN002, available from PICMG.

From a cooling perspective, the major difference between a custom design and a design based on an open specification is that the shelves and boards available to the system implemented, while fully specified, can have widely different power dissipation and airflow impedance and flow characteristics.

During the board design phase it is common practice to use one of the many powerful Computational Fluid Dynamics (CFD) software programs to analyze and predict cooling. The CFD program can predict the needed mass airflow. This is usually given as a volumetric flow at a given worst case density. The primary focus of the simulation is to ensure that device temperatures remain within limits. The simulation will indicate the airflow needed for this. AdvancedTCA requires the board vendor to provide the board airflow impedance curve shown in Figure 1 to enable the system integrator to determine the performance of the board along with other boards in a shelf system.

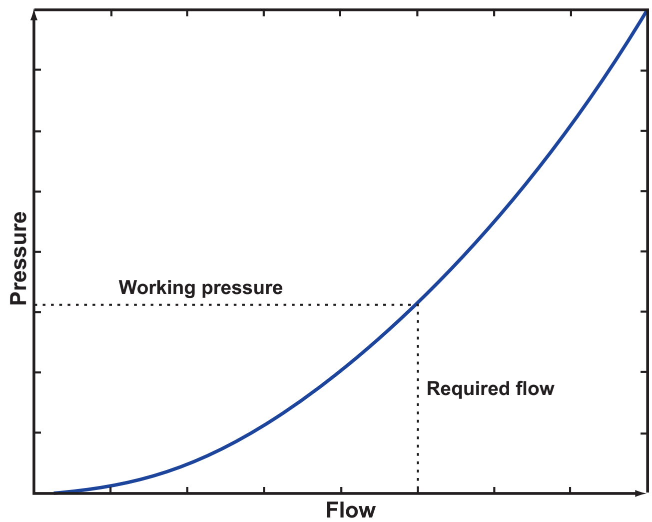

Figure 1

It is an unfortunate fact that a low-power board, requiring only a modest cooling airflow, will have low-profile components and small or nonexistent heat sinks. The resulting low airflow impedance will, for a given pressure, allow for an excessive airflow. Similarly, a high-power board requiring a high airflow will have large components and heat sinks and a high airflow impedance. For the same pressure the high-power board will have a low or inadequate airflow. These problems do not affect the board designer. They are major problems for the shelf designer and the systems integrators. This is illustrated graphically in Figure 2, which shows that board pressure operating points can vary from 8 to 64 Pascal and flow requirements between 0.001 and 0.025 M3/s.

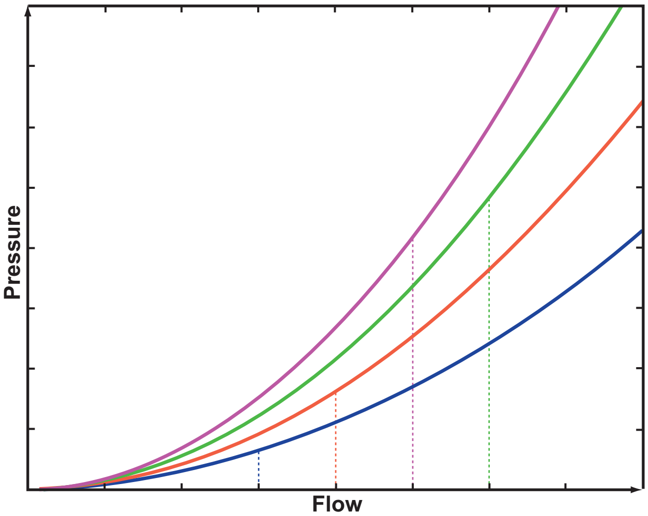

Figure 2

The AdvancedTCA shelf designer is asked to ensure cooling for boards that can be between 75 W and 400 W. With no prior knowledge of board characteristics the designer can only assume boards with identical power and airflow characteristics and provide as large an amount of airflow as possible. AdvancedTCA requires the vendor to provide a range of slot airflow and pressure curves similar to the one shown in Figure 3. The curves need to cover every slot and the range of fan speeds available. One key point should be noted: The slot pressure flow curve shown is not the fan curve. The fans in a shelf system need to move air against the back pressures of air filters. Fans must also move air against the pressure loss of direction changes as well as the losses of the boards needing to be cooled. AdvancedTCA demands that the set of curves (shown in Figure 3) represent the pressure across the slot, not the system.

System integration

A shelf and a set of boards do not make a viable system until they have been integrated together. The task of selecting and then bringing together a shelf and a set of boards, all from different vendors, falls on the systems integrator. With a high-power system this task is no longer constrained to the system electronic and management interoperability. The cooling needs to be addressed with a system level approach.

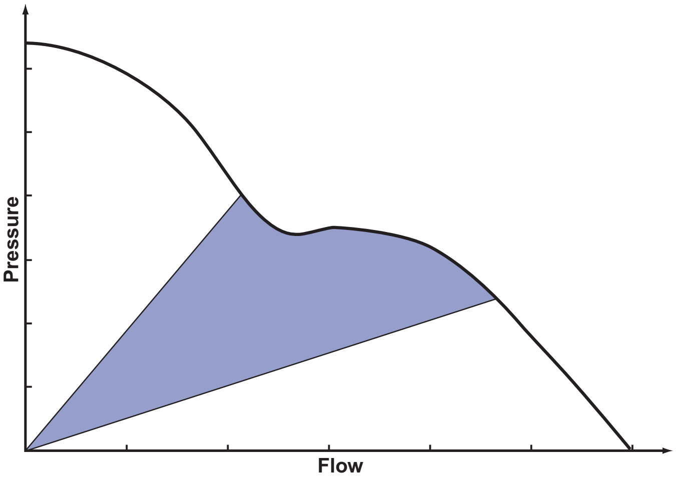

Figure 3

"Low power boards with low component profiles are most likely to be a problem ..."

The systems integrator has a number of tools available for this task. Graphical or spreadsheet analysis and simulation using CFD or Flow Network Modeling (FNM) can be used. We will discuss these briefly and present System Airflow Analysis Machine (SAAM), a numerical analysis tool.

Graphical or spreadsheet analysis based on the use of the shelf pressure/flow curves and the board impedance curves described earlier is a simple first line approach. For a single slot the intercept between the two curves provides the operating point as shown in Figure 4. Expanding this technique for multiple slots is possible, but new graphs need to be drawn for changes in fan speed, and calculation becomes extremely tedious. Solving for *what-if* scenarios is almost impossible.

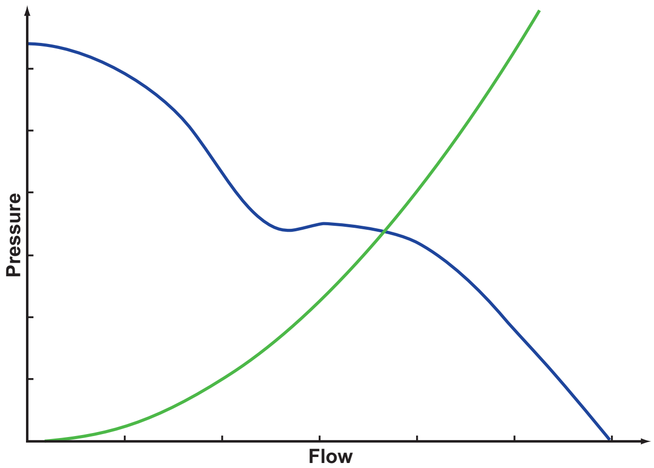

Figure 4

Finding the optimum operating point

Whether the systems integrator uses the tools mentioned earlier, or practical experience, it takes many iterations to find the system operating point suitable for the shelf and all the selected boards.

If the operating point is too low or too high, a different shelf pressure flow curve representing fans running at a higher or lower speed may need to be used. This is a simple operation for a single slot. For multiple slots the problem is greater. One can usually assume that the pressure across all slots is the same. The airflow through all the boards needs to be determined using the vendor supplied graphs with a given shelf pressure. Then each shelf slot is checked to see whether the airflow can be provided at the pressure and fan speed selected. If each slot has sufficient airflow the process should be repeated with a lower fan speed to reduce acoustic noise. If some or all of the boards have insufficient airflow, then the process is repeated by increasing fan speed until all boards have sufficient flow. If, as is likely, there is an imbalance in the airflows, and the shelf cannot provide the excess air taken by low impedance boards, then the systems integrator can request the board vendor to provide air baffles or select a different board

vendor. Low power boards with low component profiles are most likely to be a problem, requiring airflow baffles to ensure both cooling and acoustic noise requirements are met.

Computational Fluid Dynamics

CFD is a powerful tool for systems builders. A model can be built of every significant element in the airflow path. The resultant analysis can be quite accurate. The problem arises in the detail. Firstly, the integrator needs CFD models for every board and the shelf from all the candidate suppliers. Not all the vendors will have models they are prepared to release, and the models might not be compatible. Models might need to be built from mechanical STEP files or built from scratch with layout placement files and individual component data sheets. To obtain an accurate result from a board analysis using fine geometry components, particularly heat sinks, requires an analysis using a fine grid. This makes the simulation of a full system very difficult.

The system integrator needs to evaluate the effect of different board placements or of alternative board or shelf vendors and this may take considerable time. The process for finding the optimum operating point noted above remains the same requiring many simulation runs and its use can be considered impractical for a large and complex system such as AdvancedTCA.

Flow Network Modeling

The technique of Flow Network Modeling involves the representation of the flow system as a network of flow paths and components for the prediction of system-wide flow and temperature distribution. FNM is very fast in terms of model definitions, computation, showing of usable results. Figure 5, courtesy of Innovative Research, Inc., shows a typical Flow Network Model.

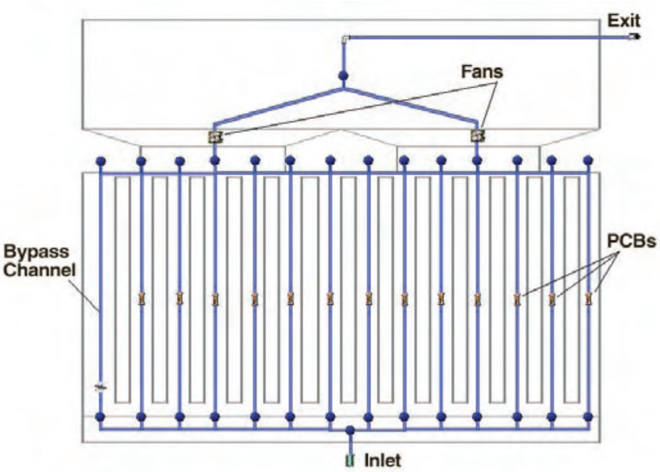

Figure 5

An FNM model is built up using the shelf elements of fans, ducts, filters (EMC and air), and boards. Simple board models can be built using Moody charts with corrections for the blockage effects of heat sinks. Unfortunately component blockage, particularly heat sinks, is the major problem in high-power systems. The solution to this problem is simple. CFD can be used to provide an accurate board impedance using as fine a grid as is necessary. These results are included in the FNM.

FNM allows for a fast and almost interactive what-if analysis of the effect of different vendor boards in different slot positions. Slightly more difficult is the what-if analysis of finding the operating point at different fan speeds.

The benefits of FNM are presented in the literature as an aid for the initial design of custom systems. For open systems the benefits of FNM extend through the system lifetime. The introduction of new or upgraded boards can be rapidly assessed.

Systems Airflow Analysis Machine

SAAM is a new software tool specifically targeted for the analysis of rack-mounted parallel board systems similar to AdvancedTCA. SAAM models airflow performance and does not provide detailed board temperature information.

The basis of the SAAM calculations is the data provided by the board and slot curves of Figures 1 and 3 required by the AdvancedTCA specification. Each slot can be modeled with a combination of the board airflow impedance (Figure 1) and the range of shelf pressure/flow curves over the fan speed operating range. These combined curves are shown in Figure 6.

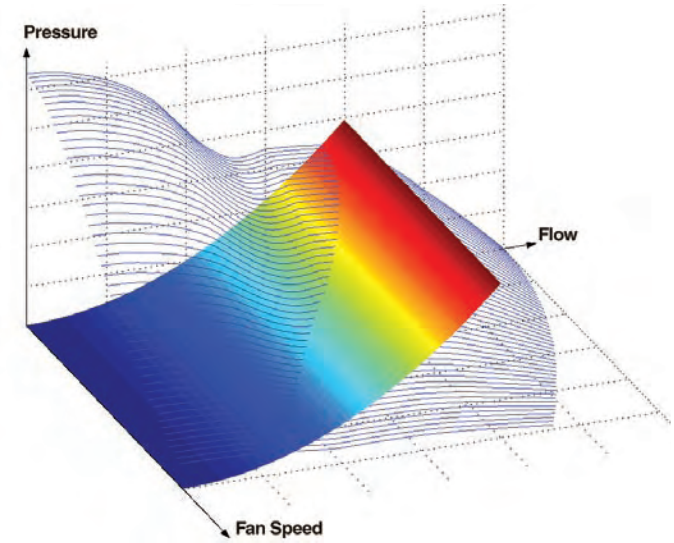

Figure 6

The board airflow impedance curve is a quadratic, and with an origin at 0,0 can be represented by two points. The shelf pressure/flow curve is more complex. SAAM uses a proprietary algorithm with the curve represented by 10 points. Five points, readable directly from the vendor published data, are taken from the maximum fan speed curve and five from the minimum fan speed curve. They are added into SAAM using text-based csv files in the MKS units of Pascal for pressure and M3/s for airflow taken from the vendor supplied board impedance and shelf pressure flow curves.

Each board in the system has a power rating and a limit to the differential temperature across the board of ΔT. SAAM can calculate the required airflow using the simple metric:

$$\text{airflow} = \text{Power} / \Delta T * \text{air-mass}$$

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The user can change this figure if an increased airflow is seen to be a necessity for specific semiconductor or other devices. Figure 7 shows a simplified version of the SAAM algorithm.

```
Set initial conditions
   While all of the slots OK or excess_airflow
      begin
         begin
         While shelf and board airflows are imbalanced adjust pressure
            For each slot calculate pressure and flow
            Save intermediate results
         end
      Reduce fan_speed
      end
            Display results
```

Figure 7

SAAM presents the required airflow, the calculated airflow and fan speed, and an evaluation of the board conditions. OK indicates that the cooling is between the minimum level and +10 percent. Airflow too low is as it says, and excess airflow shows that cooling resources are being wasted resulting in reduced fan lifetime and increased acoustic noise. The airflow too low condition can be resolved by running at increased fan speeds. The excess airflow condition is acceptable if cooling capacity and acoustic noise are not problems. If they are problems, then the system integrator has to arrange with the vendor for increased airflow impedance, typically by the addition of baffles on the board. A typical display is given in Figure 8.

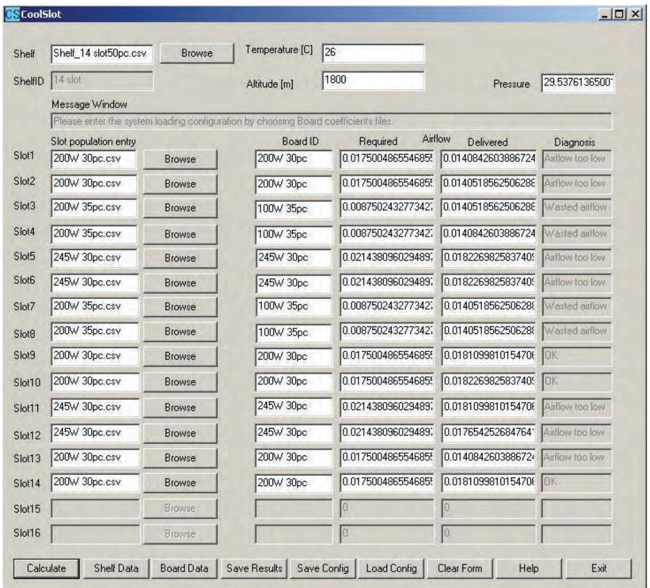

Figure 8

The SAAM algorithm provides an almost instantaneous solution for a mix of board types at different altitudes and ambient temperatures providing *what-if* scenarios during the lifetime of the installed shelf product.

Electronic C keying

Further use of the SAAM algorithms is being considered to provide electronic thermal keying of boards similar to E keying when boards are introduced into a shelf, perhaps to be called C keying.

If a board is introduced into an AdvancedTCA system without C keying there could be three results:

1. The airflow requirement matches the shelf capability and there is no problem.
2. The board does not receive the cooling and the board generates thermal events or eventually fails. Noise level may be excessive.
3. The board impedance is low. The board is adequately cooled but adjacent boards no longer receive adequate cooling and otherwise good boards start to fail.

The FRU data needed on the board would reside in four additional bytes. Shelf FRU data is larger at 20 bytes, and the shelf manager can easily run an equivalent of the SAAM algorithm.

With a C keyed system the three conditions above can be detected. Condition 1 is a *pass*. In Condition 2 the shelf manager will not allow the inserted board to run at full power and will generate a system alert. In Condition 3 the shelf manager could reduce power or shut off boards at risk as well as generate a system event.

Conclusion

The open systems integrator is presented with a range of cooling problems:

- Incorporating very different boards from multiple vendors into a shelf (or shelves) from still other vendors
- Dealing with AdvancedTCA boards of high power (between 150 W to 300 W)
- Handling performance with a wide range of ambient temperatures
- Understanding the effect of differing fan speeds
- Balancing all these with the acoustic noise limits

The integrator has some very powerful tools available for this task with CFD for the details, FNM for both initial concept and later what-if's, and FNM and SAAM for ongoing maintenance and C keying.

David Wright *has been involved in AdvancedTCA since 2002, and in practical electronics and mathematical modeling for much longer. David works for Comtel Electronics GmbH as the AdvancedTCA and MicroTCA Systems architect/consultant. David also owns and operates Wickenby Consulting Ltd. providing design and consultancy services including cooling.*

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Achieving higher reliability through system partitioning

By Paul Leroux, Jason Clarke, and Kerry Johnson

Most embedded systems today are dynamic, network-connected devices that can (or must) support new functionality throughout their mission life. This combination of upgradeability and network connectivity offers many advantages, but it also poses a number of design problems.

An embedded system must somehow be able to:

- Download and run new software components without compromising its existing real-time behavior
- Prevent untrusted components from corrupting other components or consuming system resources
- Maintain network connectivity while protecting itself from Denial-of-Service (DoS) attacks and other network-based exploits

Safeguarding the reliability and security of such systems represents a significant challenge – a challenge made all the more difficult by the sheer complexity of modern firmware. At one time, most embedded systems had modest software requirements. Typically, a few thousand source lines of code were all that was required. Today, however, an embedded system may contain millions of source lines and comprise hundreds of software threads or processes, all of them contending for a finite set of system resources, including CPU time. Some studies suggest that the code base for the average embedded project is doubling in size every 10 months.

> "From the developer's perspective, the lion's share of effort should always be spent on developing core functionality, not on schemes to protect it."

This complexity can undermine the goal of high reliability, for the simple reason that the more code a system contains, the greater the probability that coding errors will make their way into final product. Naturally, developers must employ every tool, methodology, and process at their disposal to ensure their code is correct and properly tested. The problem is that no one has developed a method to create code that is 100 percent bug-free. And no test suite can exhaust every scenario that a complex embedded system may encounter, partially because the number of potential scenarios can be almost limitless – especially if the system downloads new or untrusted software on an ongoing basis.

Facing this great number of potential scenarios, systems designers and software developers must adopt techniques that enable their products to identify, contain, and quickly recover from software faults and other threats. The real challenge, however, is finding or implementing techniques that consume a minimum of development effort and computing resources. From the developer's perspective, the lion's share of effort should always be spent on developing core functionality, not on schemes to protect it.

Virtual compartments

To address these reliability issues, some designs place virtual compartments, or partitions, around groups of software processes and allocate an engineered set of resources, such as memory and CPU time, to each partition. The system can thus prevent processes in any partition from commandeering resources needed by processes in other partitions.

Among other things, partitions can provide memory protection, where each partition is discretely controlled by the Memory Management Unit, or MMU. A microkernel operating system, for instance, can partition applications, device drivers, protocol stacks, and file systems into separate, memory-protected processes. If any process, such as a device driver, attempts to access memory outside of its process container, the MMU will notify the OS, which can then terminate and restart the process. Such an approach offers an immediate and measurable improvement to system reliability. First, it prevents coding errors in any process from corrupting other processes or the OS kernel. Second, it reduces fault-recovery times dramatically; rather than taking seconds to minutes to reboot when a memory violation occurs, the system simply restarts an individual process, a step that typically requires only a few milliseconds.

Nor are the benefits restricted to runtime. If any process attempts a memory-access violation during development and testing, the microkernel will identify the process responsible, at the exact instruction. Developers no longer have to spend days or weeks hunting down hard-to-reproduce memory errors. This ability to immediately detect access violations also minimizes the likelihood that such errors will ever make their way to a customer's premises.

Avoiding process starvation

Nonetheless, building a reliable device involves more than partitioning functionality into separate memory domains. For many systems, ensuring resource availability is also critical. If a key subsystem is deprived of, say, CPU cycles, the services provided by that subsystem would become unavailable to users. In a

DoS attack, for instance, a malicious user could bombard a system with requests that need to be handled by a high-priority process. That process will then overload the CPU and starve other processes of CPU cycles, making the system unavailable to users.

A security breach isn't the only cause of process starvation. In many cases, adding software functionality to a system can push it over the brink and starve existing applications of CPU time. Applications or services that were functioning in a timely manner no longer respond as expected or required. Historically, the only solution to this problem was to either retrofit hardware or to recode (or redesign) software – both undesirable alternatives.

To address these problems, systems designers need a partitioning scheme that enforces CPU budgets, either through hardware or software, to prevent processes or threads from monopolizing CPU cycles. An embedded operating system is a good candidate to enforce CPU partition budgets since the OS already provides centralized access to the CPU, memory, and other underlying computing resources.

Conventionally, embedded operating systems have used priority-based preemptive scheduling (Figure 1) to determine which process or thread gets control of the CPU. While this approach provides an easy, well-known method to define the scheduling priority of every thread, it can lead to process starvation. For instance, let's say you have two threads, A and B, where A has a slightly higher priority than B. If A becomes swamped with work, it will lock out B as well as any other lower-priority thread from accessing the CPU.

In other words, priority-based scheduling offers no guarantee that lower-priority threads will access at least a fraction of the CPU. Services provided by lower-priority threads – including diagnostic and fault-recovery services that protect the system from software errors or DoS attacks – can be starved of CPU cycles for unbounded periods of time, thereby compromising system availability. These issues become more acute as system complexity, and the number of threads, increases.

Fixed partition schedulers

To address this problem, some RTOSs offer a fixed partition scheduler (Figure 2) that allows the system designer to divide tasks into partitions and to allocate a percentage of CPU time to each partition. With this approach, no task in any given partition can consume more than the partition's statically defined percentage of CPU time. For instance, let's say a partition is allocated 30 percent of the CPU. If a process in that partition subsequently becomes the target of a DoS attack, it will consume no more than 30 percent of CPU time. This approach prevents the process under attack from consuming the entire CPU.

Fixed partition schedulers have their drawbacks, however. Since the scheduling algorithm is fixed, a partition can never use more CPU cycles than its

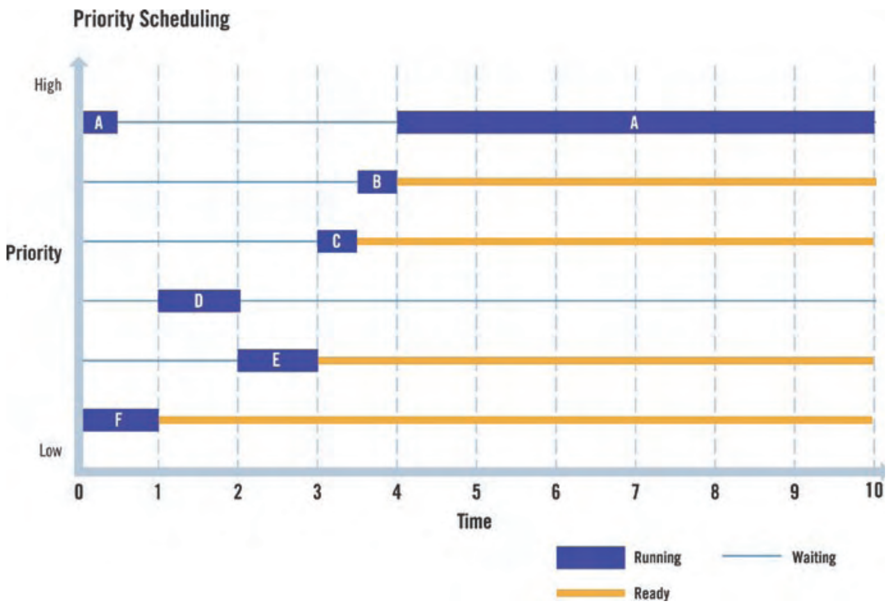

Figure 1

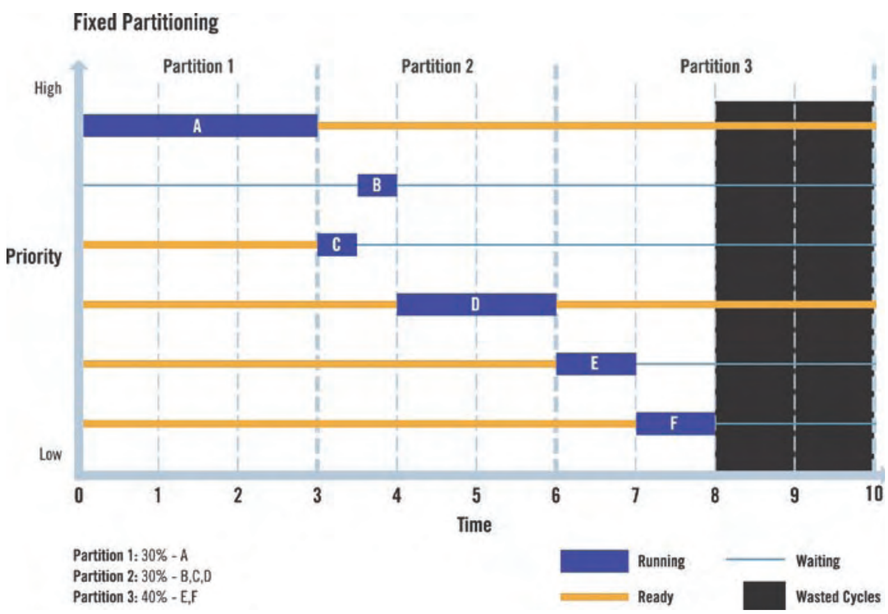

Figure 2

fixed budget, even if the system contains unused CPU cycles. Meanwhile, partitions that aren't busy waste time in an idle state. This approach squanders valuable (and available) CPU cycles and prevents the system from handling peak demands. This use it or lose it approach allows fixed cyclical schedulers to achieve only 70 percent CPU utilization. Manufacturers must, as a result, use more expensive processors, tolerate a slower system, or limit the amount of functionality that the system can support. As a further problem, developers must modify code to implement or change each partition.

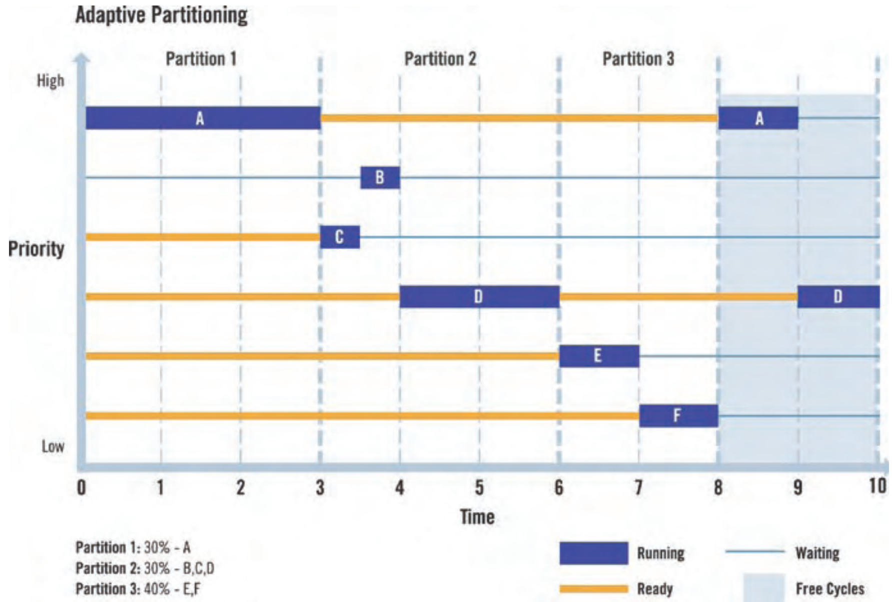

Figure 3

Adaptive partitioning schedulers

Another approach, called adaptive partitioning (Figure 3), addresses these drawbacks by providing a more dynamic scheduling algorithm. Like fixed partitioning, adaptive partitioning allows the system designer to reserve CPU cycles for a process or group of processes. The designer can thus guarantee that the load on one subsystem or partition won't affect the availability of other subsystems.

Unlike fixed approaches, however, adaptive partitioning recognizes that CPU utilization is sporadic and that one or more partitions can often have idle time available. Consequently, an adaptive partitioning scheduler will dynamically reallocate those idle CPU cycles to partitions that can benefit from the extra processing time. This approach, which was pioneered by QNX Software Systems, offers the best of both worlds: It can enforce CPU guarantees when the system runs out of excess cycles (for guaranteed availability of lower-priority services) and can dispense free CPU cycles when they become available (for maximum CPU utilization and performance).

Adaptive partitioning offers several advantages, including the ability to:

- Provide CPU time guarantees when the system is heavily loaded – this ensures that all partitions receive their fair budget of CPU time
- Use real-time, priority-based scheduling when the system is lightly loaded – this allows systems to use the same scheduling behavior that they do today

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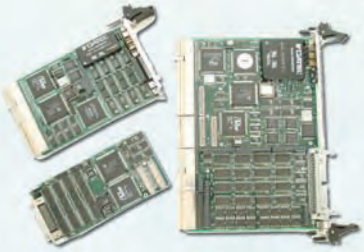

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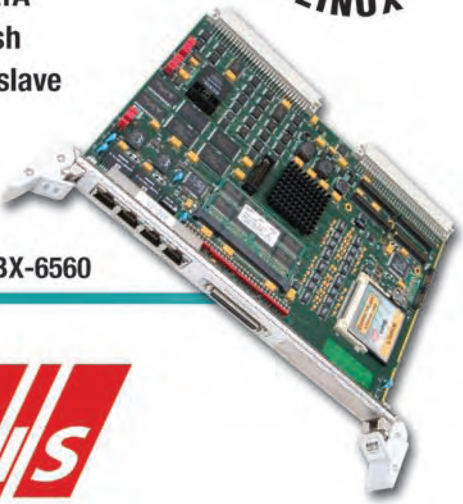

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- Borrow unused CPU time from partitions that aren't completely busy – this gives other partitions the extra processing time they need to handle peak demands and permits 100 percent processor utilization
- Overlay the adaptive partitioning scheduler onto existing systems without code changes – applications and system services can simply be launched in a partition, and the scheduler will ensure that partitions receive their allocated budget
- Guarantee that recovery operations have the CPU cycles they need to repair system faults, thereby improving Mean Time To Repair (MTTR)
- Stop malicious code from stealing all the CPU time through a DoS attack

Increased system availability

When a hardware or software subsystem fails in a high-availability embedded system, automated recovery functions must return the system to a proper operating state. An example is a *software watchdog* that automatically detects and restarts a failed process. The faster such recovery functions execute, the lower the MTTR and the greater the overall system availability. An approach such as adaptive partitioning can help by ensuring that these functions have the CPU time they require.

In systems that typically run at very high CPU utilization, processes that monitor system health and report errors don't get an opportunity to run in a timely manner. The CPU guarantees provided by a partitioning scheduler address this problem and ensure that routine diagnostic functions run as intended. These functions can thus detect and report problems before the problems result in hard failures.

In the most severe cases, the user must intervene to revive a system. In such situations, the system must notify the user of the failure and provide some way of diagnosing the problem. Again, adaptive partitioning helps by ensuring the system has enough CPU cycles to alert the user and to provide guaranteed access to the user interface, be it a system console, remote terminal, or other method. Regardless of system load, the user or administrator can always determine the system state.

Minimum risk

Properly implemented, an approach like adaptive partitioning doesn't require code changes, nor does it change the debugging techniques already familiar to designers. It can also use the standard POSIX programming model, allowing embedded developers to work with the same industry-standard APIs and task-prioritization schemes that they do today. To introduce adaptive partitioning, developers simply define partition budgets and decide which processes or threads reside in each partition. The processes themselves remain unchanged.

Other partitioning models

So far, we've discussed OS-level partitioning, but systems designers can also choose from other approaches to manage

CPU use. There is, for example, application-level process monitoring, in which a monitor application continually examines the CPU usage of every thread to detect when a thread consumes too much CPU. To succeed, this approach requires techniques to notify the offending thread and to have the thread back off in some way.

Unlike adaptive partitioning, this approach can place a significant burden on software developers. Besides building the monitor application, the development team must implement behaviors in every participating thread to monitor the thread's CPU use. The cost and complexity of such development quickly multiplies as more threads are added. Moreover, this approach relies on the correct behavior of all participating threads. Without considerable refinements, it can't easily differentiate between a runaway error condition and a thread that is simply busy performing its intended function. As a consequence, developers spend valuable design resources on developing (and maintaining) the partitioning scheme, rather than on creating core product features.

Designers can also consider hardware partitioning, which uses dedicated hardware to run various software subsystems, with the goal of minimizing resource contention between them. While effective, this approach requires additional hardware, which can add significantly to system costs. It thus offers a feasible alternative for systems that ship in limited volumes and where the deployed system cost is small in comparison to the development cost.

Partitioning plus performance

Embedded software is becoming so complex that, without some form of partitioning, system designers and software engineers will be hard-pressed to satisfy the conflicting demands for reliability, performance, security, time to market, and innovative features. An OS-controlled approach to partitioning goes a long way toward addressing these requirements by providing each subsystem with a guaranteed portion of CPU cycles, while still delivering the deterministic, real-time response that embedded systems require. Device manufacturers can, as a result, readily integrate subsystems from multiple software teams or third-party developers, allow new and upgraded components to run without compromising existing system behavior, and protect their systems from DoS attacks and other network-based exploits. If the partitioning model also provides a flexible, efficient scheduler that allows partitions under load to borrow unused CPU time from other partitions, then manufacturers can realize these various benefits without having to incur the cost of faster, more expensive hardware.

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PICMG 2.16: Rumors of death greatly exaggerated

By Stuart Heptonstall

Given that the demise of PICMG 2.16 has been predicted for some time, a recent introduction of a PICMG 2.16 compliant product might seem counter-intuitive. Weren't serial switched fabrics supposed to have sounded Ethernet's death knell? In this introduction to the PICMG 2.16 Mil/Aero Product Guide *that follows, Stuart answers that question with a look at the military market's needs.*

To begin with, the military market is inherently conservative. It values continuity and stability and has traditionally prized proven technologies above those that are less well proven, even if they offer superior performance. The reasons are obvious. First, if a telecommunications system fails, it is seldom a matter of life and death. Failure of a military system can mean just that. Second, the typical military system will see a development and deployment cycle that may run into tens of years, and that will require support, maintenance, and upgrade for the duration of its life. Both factors point to the selection of technologies that have been, and can be expected to be, around for the long haul. That's why the VMEbus architecture, celebrating its 25th anniversary this year, has historically been the architecture of choice for the armed forces.

Those same factors point to Ethernet as having been the military networking technology of choice for many years: The fact that it is the most widely used commercial networking technology (some estimates put its market share at around 90 percent) fits well with the military's strategy – now past its 10th year – of using COTS solutions wherever possible. It has been around as long as VMEbus and, like VMEbus, has seen its performance substantially upgraded over time, from the early 10 Mbps to the latest 10 Gbps today.

However, these reasons for conservatism should not be taken to mean that the military market has not evolved rapidly, that its requirements have remained unchanged, or that it is averse to new technologies. Nothing could be farther from the truth. The face of military computing is changing briskly. Network-centric warfare, and programs such as Future Combat Systems (FCS), are leveraging the astonishing power of today's technologies.

Over the past 20 or more years, however, there has been a discernible trend in military computing – no different, it could be said, to trends in computing in other markets – for a smaller, lighter weight, more nimble, and more flexible system, characterized by greater distribution of intelligence, greater asset autonomy, and greater reliance on the network to deliver actionable intelligence.

The VMEbus architecture was, in many ways, the ideal architecture for the more monolithic systems of the military's past, but despite the claims of its proponents it is not a *one size fits all* solution. It is to the great credit of the technology and of the trade association VITA[1] that it continues to be at the heart of the majority of today's military systems. VMEbus has adapted and evolved to meet changing requirements. However, VMEbus architecture is not without its important limitations.

VMEbus, for example, does not lend itself readily to the concepts of *small* and *lightweight* that are at the heart of network-centric warfare in such uses as unmanned and/or autonomous vehicles. Umanned Aerial Vehicles (UAVs), such as the APV-3 shown in Figure 1, also demand performance in the smallest, lightest possible package. Another concern is that VMEbus is power hungry, creating heat that can be difficult to dissipate in small enclosures. What's more, the full 64-bit

Figure 1

performance of VMEbus is available only in the 6U implementation; the 3U implementation is limited to 16 bits, creating performance constraints. That's why 3U CompactPCI is finding increasing favor in the military marketplace.

The military is at ease with CompactPCI because, while it may not have the extensive track record of VMEbus, it has now been around long enough and has been implemented widely enough to feel comfortable. It's unlikely that CompactPCI will ever come close to displacing VMEbus as the technology of choice for military systems, but in an increasing number of important niches its advantages are compelling.

PICMG 2.16 benefits

Radstone introduced its CPX24 rugged Gigabit Ethernet Switch (Figure 2) in December 2005. Its predecessors, the GBX8 and GBX16 Ethernet switches, were both VME boards. But the design goals for the CPX24 were extremely challenging. The requirement was to rise to the increasing need of the military for even greater connectivity: Support for 24 Ethernet ports was necessary. Beyond that, the required degree of expandability to 48 Ethernet ports could only be supported through the provision of two 10 Gigabit Ethernet uplink ports. VMEbus is unable to deliver the required pin count

Figure 2

to facilitate this kind of connectivity. In addition, the military's increasing focus on ease of diagnosis, ease of maintenance, and minimal downtime pointed to a rear I/O solution. The answer had to be a PICMG 2.16-compliant CompactPCI board.

PICMG 2.16 benefits with respect to switches aren't lost on the VMEbus community and have led to the development of the VITA 31.1 standard. VITA 31.1:

- Describes the addition of Gigabit Ethernet to a VME backplane via the P0 connector
- Adopts the familiar PICMG 2.16 P3 connector pinout
- Fully supports the PICMG 2.16 definition for Ethernet switch cards

This chameleon-like ability to coexist both in CompactPCI and VMEbus domains has helped to establish PICMG 2.16 as the standard of choice for 6U board-level Ethernet switches. The fact that CompactPCI is already well accepted by the military market makes this dominance even more deeply entrenched.

CompactPCI secure in military marketplace

InfiniBand, RapidIO, StarFabric, and PCI Express are garnering increasing interest among military buyers. In addition, the VPX (formerly VITA 46) standard has been specifically designed to provide VMEbus users with a path to the latest generation of serial switched fabrics. On the other hand, CompactPCI isn't about to lose the place that it has in the military marketplace – if anything, its presence seems likely to increase. Similarly Ethernet's long-term future in military systems is certainly assured. The fact that PICMG 2.16 is specifically embraced by a VITA standard is telling. And that should tell us that those who have been foretelling the imminent death of PICMG 2.16 might well have been somewhat premature.

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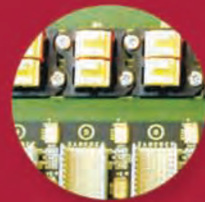
[1] VITA (vita.com) is the name of the organization formerly known as the VMEbus International Trade Association.



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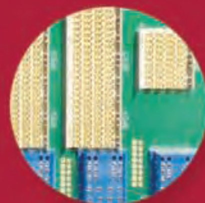

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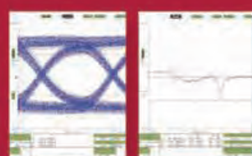

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8701-TX 10/100 Ethernet PMC	64-bit, 33 MHz universal 3.3 V and 5 V PCI, 8 W • RJ-45 for CAT 5 Unshielded Twisted Pair • Link LED indicator per port • Front I/O only

Continued on page 44

PRODUCT GUIDE

PICMG 2.16 MIL/AERO

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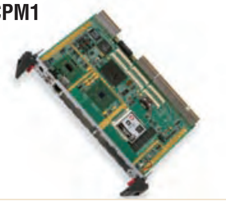
Company Name/ Model Number	Website/ Description
One Stop Systems	**www.onestopsystems.com**
4U CompactPCI Enclosures	A 4U high by 12" deep, horizontal CompactPCI enclosure • Provides a rugged CompactPCI platform for applications that require up to eight 6U slots but do not require the redundancy of larger CompactPCI enclosures • Cable routing to rear I/O boards • One 5.25" front-access drive bay and one internal 3.5" drive bay • Two large intake fans and two card cage fans cool with front-to-rear airflow • 350 W ATX-style power supply with independent fan
Vector Electronics	**www.vectorelect.com**
Vector Ruggedized Enclosures	1101.10 compliant • Rugged metal enclosure • MIL-461-D, E for shock/vibration, EMI/RFI CE and FCC Class B, Part 15 • 3, 5, 7, or 12-slot • VME, VME64x, CompactPCI • Accepts horizontally mounted cards, forced air cooling • Configurable up to three half-height or one full and one half-height drive bays • 250 W, 450 W, 750 W, and 1,000 W power options
Fabrics: Fibre Channel	
ACT/Technico	**www.acttechnico.com**
6U VME/VITA 31.1 GbE Switches 	Up to 10 Ethernet ports including one optical fiber channel (SX or LX) • VITA 31.1 switches use the PICMG 2.16 standards • Nine-port 1000BASE-T conduction-cooled version • Layer 2 bridging capabilities: Nonblocking with full wire performance, 4K MAC addresses, autolearning and aging, 802.1 Q support for 4K VLANs or port-based VLAN • Plug-and-play for basic switching • Backpressure flow control on half duplex ports, pause frame on full duplex • Four QoS traffic classes • MAC authentication, IEEE-802.1x compliant
Mezzanines and carriers	
AcQ InduCom	**www.acq.nl**
i4400	Low-cost 6U form factor PMC/PrPMC carrier • VMEbus to PCI interface implemented in FPGA • Selectable standard VMEbus addressing (A24) with byte • Even/odd) or word data transfers (D08(E/O)/D16/D32) • Features 2 single or 1 double PMC • 33 MHz/ 32-bit PCI interface to PMC modules • 3.3 V PCI signaling on PMCs • Support for two ANSI/VITA 32-2003 compliant Processor PMCs • Rear I/O on P2 or optional P0 connector • Available in 3-row and 5-row VME with optional P0 • Conduction cooling (optional)
Processor blades	
Diversified Technology	**www.atcatogo.com**
CPB4612 	CPU blade based on the Pentium M processor • :Low thermals with high performance • Speeds up to 1.8 GHz and 2 MB L2 cache • Dual 100/1000 Ethernet interface
CPB4305	CPU Blade based on the Intel Pentium 4-M Processor • Low cost board featuring Intel 845E Chipset and 400 MHz FSB • Two Gigabit Ethernet intefaces • 6U x 4HP, Operates as System or Peripheral Processor
Processor: Pentium II	
Dynatem	**www.dynatem.com**
CPM1 	Convection- and conduction-cooled versions • Supports two PMC sites in a single-slot configuration • Supports 1.8 GHz Pentium M, low-power 1.4 GHz Pentium M, and ultra-low-power 1.0 GHz Celeron M • Supports digital and analog graphics • 1 GB DRAM • Three GbE ports (including two for PICMG 2.16) • Up to 16 GB of onboard bootable CompactFlash • Supports USB 2.0, IDE, floppy, SATA • Four serial ports • Extended temp. versions to -40 °C/+85 °C

Continued on page 46

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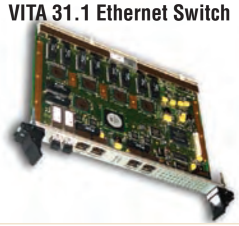
PRODUCT GUIDE

PICMG 2.16 MIL/AERO

Company Name/ Model Number	Website/ Description
Processor: Pentium III	
SBS Technologies	**www.sbs.com**
CT8	6U CompactPCI CPU single board computer • ULV Intel Pentium III processor • 512k, up to 933 MHz • Up to 2 GB SDRAM with ECC • Dual 10/100/1000BASE-T GbE ports •Two serial I/O with FIFOs • Part of SBS Gigaboards series • Supports full hot swap, IPMI (PICMG 2.9), redundant system slot • Usable in a system or non-system slot • Adheres to the PICMG 2.16 dual Ethernet specification • Supports the 64-bit/66 MHz CompactPCI bus
Processor: Pentium M	
Dynatem	**www.dynatem.com**
CRM Rugged 6U	Rugged Pentium M based with Universal bridge that can be a system slot controller, or peripheral SBC, or PICMG 2.16 compatible blade • Up to 1 GB of DDR-266 SDRAM at 2.136 GBps • Intel's 855GME GMCH provides DVO and VGA graphics • Intel's 6300ESB provides IDE at 100 MBps • Two SATA ports at 150 MBps • Four USB 2.0, two COM ports • Intel's 82541 front panel 1 GbE port • 82546 brings two 1 GbE ports to backplane • Two PMC sites
Fastwel	**www.fastwel.com**
CPC501 	Fully compatible with PICMG 2.16 specification, thus providing capability to build robust redundant systems • Intel Pentium M up to 2.26 GHz onboard • Two Gigabit and one Fast Ethernet ports • Flash disk soldered onboard • Hot swap and blade capability • Operating temperature range: -40 °C to +85 °C • Reliable and cost-effective • Smart temperature control • System and peripheral slot compliance • Suitable for telecom, factory automation, transportation, aerospace
Processor: PowerPC	
Curtiss-Wright	**www.cwcembedded.com**
G4C – cPCI SBC 	PowerPC 7457 with AltiVec RISC processor based SBC with dual, onboard PICMG 2.16 1000BASE-T (GbE) Ethernet ports • Standard 6U x 160 mm module with 64-bit CompactPCI interface and PICMG standard I/O pin-out • Onboard, dual-ported packet memory tied to dual GbE ports • 2 MB external L3 SBSRAM cache • 512 MB to 1 GB of onboard SDRAM • 64 KB of NOVRAM and 128 MB of program flash with write-protected boot area and onboard programming • Extended temp, rugged, air- or conduction-cooled versions
Extreme Engineering	**www.xes-inc.com**
XCalibur1002 	A 6U CompactPCI ruggedized blade • IBM 750GX PowerPC processor • Ruggedized • Operational from -40 °C to +85 °C • Dual PCI-X PrPMC slots • Up to 1 GB 266 MHz DDR SDRAM • 4-80 MB soldered flash and CompactFlash socket • Dual PCI-X PrPMC slots • Front panel serial and 10/100/1000 Mbps Ethernet ports • Two 10/100/1000 Mbps PICMG 2.16 backplane Ethernet ports • Complies with PICMG 2.0, 2.1, 2.3, 2.9, 2.16 • VxWorks, Linux, and QNX Neutrino V6.3 support
Routers/Switches	
ACT/Technico	**www.acttechnico.com**
VITA 31.1 Ethernet Switch 	24 10/100BASE-T Fast Ethernet and two GbE ports • VITA 31.1 switches use the PICMG 2.16 standards High-speed nonblocking Layer 2 switch with: Store-and-forward, 4,000 MAC addresses, static or automatic MAC address management, and broadcast filtering • Autonegotiation and auto-MDI/MDIX crossover • Prevents packet loss with backpressure and IEEE-802.3x flow control • QoS Layer 2/3 using two priority-queue with advanced congestion management • Supports VLANs based on ports and/or MAC addresses to simplify network management

Continued on page 49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The cPCIS-6230R/64 is a 2U-height three-slot CompactPCI chassis. It is equipped with a PICMG 2.1 hot-swap compliant 64-bit 6U CompactPCI backplane with P3 and P5 rear I/O. It supports one dual slot system board and two peripheral slots. The cPCIS-6230R/64 also features a built-in 300W AC-input power supply, slim-type EIDE CD-ROM, floppy drive and internal space for drive bays for one 2.5" HDD and one 3.5" HDD.

For more info, go to:
www.adlinktech.com/products

Full-size Intel® Pentium® 4 (LGA775) Processor SBC

The new NuPRO-851DV has a high-computing capability and supports an 800MHz FSB with hyper-threading Intel® Pentium® 4 (LGA775) processor.It has a large communication bandwidth with two PCI Express x1 Gigabit Ethernet ports. It supports Serial ATA for high-speed storage, USB 2.0 and other generic features including VGA, COM, keyboard, mouse and hardware monitoring.

For more info, go to:
www.adlinktech.com/products

6" Cube Multi-App Embedded Computer w/ Lots of Possibilities!

The GEME computer is powered by low-voltage fanless CPU making it ideal for embedded motion, vision, DIO, communication and high-speed link applications. It has an expandable enclosure designed for one PMC and up to three PC/104 modules. Integrated four-channel video capture supports NTSC/PAL cameras at up to 30 frames per second. The GEME is compact with frontal I/O access and multi-storage options.

For more info, go to:
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ATCA Blade with Advanced Switching Interface

The aTCA-6891 is an Intel® dual LV-Xeon 800FSB based AdvancedTCA processor blade featuring four PICMG 3.4 compliant Advanced Switching Interconnect (ASI) x4 Ports. The x4 ASI Ports are brought out on Fabric Interface Channels 1 - 4 and provide 32Gbps data throughput when used on a five-slot full mesh backplane. Software support for the ASI network is provided by Stargen's AXSys ASI Software Suite including a GUI module to view the interconnect topology, a management module for discovery and enumeration, a driver module to access the ASI fabric and an advanced services module for high availability, path redundancy and SNMP bandwidth reservation.

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PICMG 2.16 MIL/AERO

Company Name/ Model Number	Website/ Description
ACT/Technico (continued)	**www.acttechnico.com**
6U 2.16, Gigabit Ethernet Switch – 674x	Seven different configurations available in standard, extended temperature, and conduction-cooled models • Up to 10 Ethernet ports including 1 optical fiber channel (SX or LX) • Conduction-cooled version • Layer 2 bridging capabilities • Nonblocking w/full wire performance • 4K MAC addresses • Autolearning and aging • 802.1 Q support for 4K VLANs or port-based VLAN • Back pressure flow control on half duplex ports and pause frame on full duplex • Four QoS traffic classes
6U Fast Ethernet switch, PICMG 2.16, 24 port	24 10/100 Fast Ethernet + 2 GbE ports • High-speed nonblocking Layer 2 switch with • Store-and-forward • 4,000 MAC addresses • Static or automatic MAC address management • Broadcast filtering • Autonegotiation and auto-MDI/MDIX crossover for true plug-and-play • Prevents packet loss with back pressure and IEEE 802.3x flow control • QoS layer 2/3 using two priority queue with advanced congestion management
CWCEC	**www.cwcembedded.com**
CLX2500	A 16x16 physical layer switch in CompactPCI format • Allows any input signal to be connected to any output signal • The switch operates on signals from 65 Mbps to 3.125 Gbps • Various topologies are supported including: point-to-point, loop, and multicast
Radstone Embedded Computing	**www.radstone.com**
CPX24 	Rugged 24-port Gigabit Ethernet switch with PICMG 2.16 compliance • 24-port fully managed Gigabit Ethernet switch •10 Gigabit uplink ports for expansion • Layer 2/3 switching with advanced support for VLANs, QoS, and IPv6 • PICMG 2.16 compliant • 88 Gbps nonblocking switch fabric with full wirespeed performance • Configuration through Web interface • Expands to 48-port nonblocking solution • Unmanaged version available • Air- and conduction-cooled
SCSI controller	
Astek Corporation	**www.astekcorp.com**
A21320-PMC	PMC Ultra320 SCSI single-channel Host Bus Adapter • 64-bit, 33/66 MHz PMC • LSI Logic's TolerANT technology for reliability and signal quality • LSI Logic's Fusion-MPTTM architected featuring more than 140,000 I/O/sec • Supports all major OSs • Suitable for attaching JBODs, RAID arrays, tape drives, tape libraries, and other SCSI peripherals to workstations and servers • Integrated RAID is OS-Independent, no special device drivers
A22320-PMC	Ultra320 host board adapter • Suitable for workstations and servers needing boot volume and connectivity to legacy devices, tape backup, or external storage • Two independent Ultra320 SCSI channels, allowing a combined throughput of 640 MBps • Integrated RAID is OS-independent, no special device drivers • 64-bit, 33/66/133 MHz PCI-X • LSI Logic's TolerANT technology for reliability, signal quality
Thermal management	
Simon Industries	**www.simonindustries.com**
Heat Frames 	Conduction-cooled heat frames • Extensive experience in producing custom heat frames for conduction-cooled embedded applications • Can design a heat frame to precisely fit your board and then model its thermal and vibrational performance, proving the design before it goes into the production phase • Can supply ancillary heat frame components like wedgelocks, ejectors, and thermal interface materials, heat frame ready to use right from the box
Video Processor	
Aitech Defense Systems	**www.rugged.com**
M585 	High-performance 2D and 3D graphics combined with extensive video I/O capabilities (Permedia3 graphics processor) • 32 MB SDRAM frame buffer memory • RGB/RGsB analog output support resolution up to 1600x1200; analog video inputs supporting composite, S-video and RGB/RGsB; composite video/S-video outputs supporting NTSC or PAL (according to configuration)


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Page/RSC#	Advertiser/Product description
37	ACT/Technico – PICMG 2.16 Network Solutions
48	ADLINK Technology – ETX Modules
601	Advanet/Radic – PMC Modules
3	Aitech Defense Systems – VMEbus and CompactPCI products
36	Alphi Technology – PowerQUICC III
33	Artesyn Technologies – Telecom Technology
31	AZ-COM – Extenders
20	Comtel Electronics – Backplanes and Systems Solutions
7	Diversified Technology – High Reliability Modular Platforms
42	ELMA Bustronic – Custom Optical/CompactPCI Bus Backplane
27	ELMA Electronic – Handles and Panels
17	Embedded Planet – Hardware and Software Solutions
13	Excalibur Systems – MIL-1553
41	Hybricon – Liquid Cooled 100W/Slot 1 ATR
52	Kontron – Open Modular Solutions
21	Kontron – Dual Core Open Modular Solutions
15	MEN Micro – F14 cPCI SBC
602	MGV Stromversorgungen – CompactPCI Power Supply
11	Micrel – Micrel Ethernet Solutions
44	National Instruments – PCI and PXI Digitizers
50	One Stop Systems – PCI Express/Max Express
29	Performance Technologies – Advanced Managed Platforms
23	Positronic Industries – Zone 1 Power Connectors
2	RadiSys Corp – AdvancedTCA Solution
35	Red Rock Technologies – Mass Storage Modules
5	SBS Technologies – Pentium M Processors
39	Schroff – AdvancedTCA
51	Simon Industries – AMC Bezel Assemblies
9	SMA – 3U CompactPCI CPU7.2
43	Sundance – SMT3000
45	Sundance – SMT791
49	Sundance – SMT6050
25	TEWS Technologies – Embedded I/O Solutions
47	Vector Electronics – System Packaging
26	Winchester Electronics – ATCA Zone 1 Power Connectors

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