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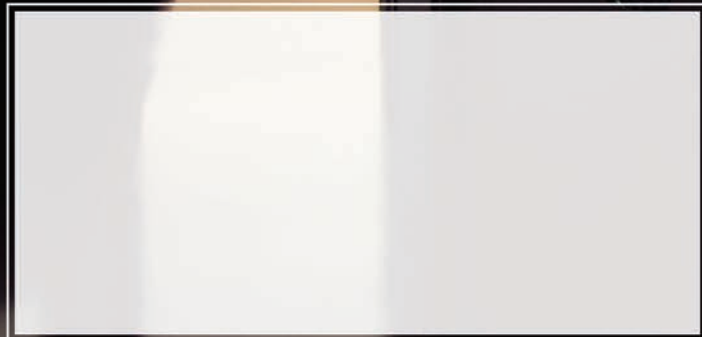
AUGUST 2006

VOLUME 10 NUMBER 6

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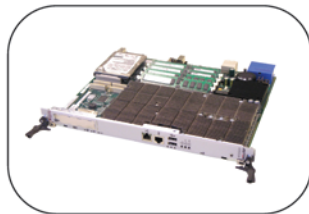
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www.tmcnet.com/voipdeveloper/

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CompactPCI 3U Express Expansion Link board photo courtesy of One Stop Systems.



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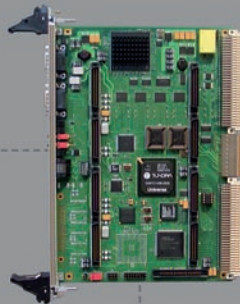
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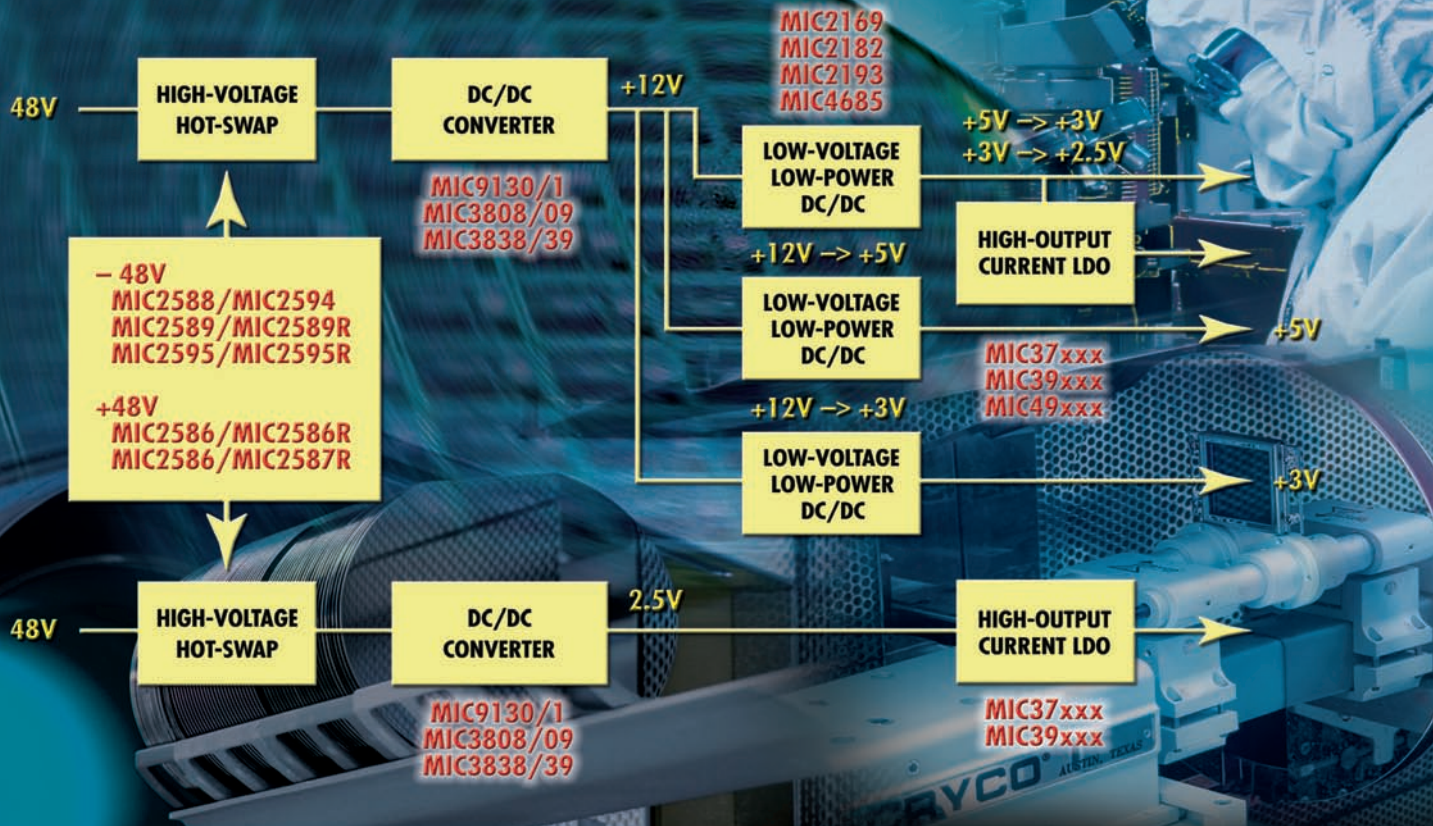
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Editor's Foreword

By Joe Pavlat

CompactPCI & AdvancedTCA Systems

GLOBALCOMM 2006

GLOBALCOMM 2006 saw more than 20,000 people attend North America's largest telecommunications infrastructure trade show. Exhibitors numbered more than 500 at the June 4-8 Chicago conference.

Forty-two PICMG member companies exhibited in the PICMG Technologies Showcase (Figure 1), one of the larger multicompany pavilions, with around 8 percent of total exhibitors in the Showcase. PICMG has reserved an even larger space for 2007 after Showcase spaces sold out this year. Quite a few PICMG member companies, including Diversified Technologies, Intel, Artesyn, Motorola, and Molex had stand-alone booths, many near the Showcase. I apologize if I missed any others, but it was a big show. Attendees included (left to right, Figure 2) Wade Appelman of StarGen and Warner Andrews of Zarlink, Jerry Gavin of NMS Communications, Daniel Sauriol of Kontron, and Mondo Mikhail of SBS.

Virtually all of the companies in the PICMG Showcase showed AdvancedTCA products, confirming that this technology is becoming mainstream and widely accepted as the right platform for next-generation infrastructure equipment. A number of providers showed AdvancedTCA-based equipment. Lucent Technologies announced an AdvancedTCA300-based product at the show, planning late 2006 deliveries.



Figure 1

The analyst community was very positive. "Recent Yankee Group research shows that leading Tier 1 telecom equipment manufacturers are embracing the concept of common platforms and estimate a 30 percent improvement in time-to-market and project development costs from using standards-based communications servers," said Brian Partridge, senior analyst of the Yankee Group.

MicroTCA had its real coming out at GLOBALCOMM, with dozens of functioning systems at the event. Figure 3 shows a unique MicroTCA system from CorEdge networks. A MicroTCA system from SBS capable of full redundancy is pictured in Figure 4.

Cooling 500 W

A group of PICMG member companies working privately under the banner of the Liquid Cooled Embedded Computer (LCEC) initiative debuted a prototype of innovative liquid cooling technology capable of cooling 500 W in a hot swappable module. The module is only the size of a medium-sized paperback book. Look for more on LCEC in an upcoming issue of *CompactPCI and AdvancedTCA Systems*.

Siemens has selected Motorola's Embedded Communication Computing business as their AdvancedTCA equipment supplier of choice. "Siemens is committed to applying an open standards-based common platform with AdvancedTCA as a main technology in both its mobile networks and fixed networks portfolio," said Dr. Dieter Carl, Siemens' Vice President Platform Strategy. "Our customers will benefit due to the need for rapid deployments and converged network build outs to provide new revenue-generating services."



Figure 3



Figure 4

IMS takes off

IP Multimedia Services (IMS) was a subject of major buzz at the show. A new study by ABI Research notes fixed and mobile network operators will invest a total of \$10.1 billion in IMS capital infrastructure over the next five years. They also predict that operators will generate \$49.6 billion in service revenue from IMS-enabled applications in 2011. IMS promises seamless meshing of mobile and fixed networks as well as services, including push-to-talk, Web browsing, video, streaming content, interactive games, and instant multimedia messaging. Many suppliers were talking up AdvancedTCA as an important platform for IMS.

Positive feedback at the show conveyed the general feeling that AdvancedTCA is here to stay in a big way and indicated MicroTCA will prove to be a very important open platform standard.

Joe Pavlat
Editorial Director



Figure 2



d¹

design.

d²

develop.

d³

deploy.

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Editor's Notes

By Rosemary Kristoff

CompactPCI & AdvancedTCA Systems

The train is starting to roll...

Following GLOBALCOMM, I struggled to find a way to describe the atmosphere. I think John Fryer, Director of Technology Marketing at Motorola, summed it up best when he said, "the train is starting to roll." John was referring to the pervasiveness of AdvancedTCA at the show as well as the affirmation of the AdvancedTCA platform by Tier 1 TEMs. Recent developments championing open standards support this trend. For example, Nortel is implementing its "Business Made Simple" initiative, partnering with Motorola to standardize on a new AdvancedTCA-based communications server. Meanwhile, GoAhead Software announced their high-availability, standards-based middleware is deployed on more than 10,000 nodes worldwide. The top photo in our gallery shows Lacy Williams, Marketing Programs Manager at GoAhead. Also, Lucent Technologies unveiled a new platform based on the emerging AdvancedTCA300 specification.

The standards organizations were well represented at the show. PICMG has been casting a wider net of late, with 54 new members added to the roster since January. More than 40 of these vendors exhibited their latest offerings in a technologies showcase pavilion. These exhibitors included long-time and recent PICMG members. For example, ADLINK and RadiSys, members since PICMG began, were joined in the PICMG Showcase by new member AVIVA Networks.

For a glimpse of the exhibitors at the pavilion, go to www.advancedtca-systems.com/globalcomm2006.

Adjacent to the PICMG booths was the CP-TA, OSDL, and SA Forum showcase. These three organizations provided educational sessions to update attendees on their progress. To date the SCOPE Alliance has finished the AdvancedTCA profile and the CP-TA association will also be focusing on pretesting and pre-validating specific AdvancedTCA profiles. SCOPE is about to release the Carrier Grade Linux profile, which next flows into the OSDL's Carrier Grade Linux specification and the SA Forum's specifications consistency/gap review process.

A quick tour

Thanh Ngyuen, Product Manager, demonstrated audio/video server platforms at the Emerson Embedded Computing (formerly Artesyn) booth. The demonstrations provided show attendees a first-hand look at the capabilities of Emerson's new AdvancedTCA blade and with Surf Communications' modules performing IMS video streaming and videoconferencing. Todd Wynia, vice president of product management and marketing, has been working with MicroTCA since the beginning. He explained how their MicroTCA development platform includes Emerson's shelf management software, SpiderWareM3, to help with managing, maintaining, and monitoring.

To make sure AdvancedTCA is an option for TEMs developing triple play applications, Performance Technologies has introduced a series of products including a base and fabric 10 Gigabit Ethernet (GbE) switch and to go along with the switch, a 10 GbE intelligent AdvancedTCA carrier. Hank Heneghan, director for product management, explained the processing power for their new 64-bit AdvancedMC module comes from the AMD Turion 2.0 GHz processor. He applauds AMD on the excellent job they have done on the architecture side. Shown in the second from top gallery photo are (left to right) Hank and Tom Saluzzo, who is hardware development group leader at Performance Technologies.

The AdvancedTCA server cabinet from Elma Bustronic in the third from the top gallery photo has a sleek, modern style favored by Apple. Also pictured are (left to right) Ron Hall, Regional Sales Manager, Optima, and Justin Moll, Director of Marketing, Elma Bustronic. The server cabinet's unique features include:

- Advanced cooling techniques
- Engineered cable management
- Front and rear door
- Rugged door hinges
- Removable side panels
- Three-piece top cover with fan plate and cable access panels
- Door gasket for environmental sealing
- Modular base with options for fixed mount, levelers, or casters

Embedded Planet's George Ishac, Sales Engineer, and Marketing Manager Tim Van de Walle (left to right, fourth gallery photo from the top) introduced attendees to the company's new AdvancedMC designed for wireless basestations, media gateways, enterprise network access systems, test systems, and server blades. The card boots from onboard flash so it can be used outside of a traditional integrated AdvancedTCA or MicroTCA environment.

An extensive line of WiMAX turnkey solutions from Alliance Systems based on AdvancedTCA and Intel's IXP Advanced-MCs offer carriers, service providers, OEMs, TEMs, and application developers an open solution rather than a proprietary one at the API level. Alliance's field engineering manager, Austin Hipes, remarked that NEBS-compliant higher density



storage solutions for iSCSI complement Alliance's AdvancedTCA servers.

On the optical front, Optovia's new hut skipping line system, an optical amplifier, eliminates intermediate network line amplifier sites saving telecom carriers, cable system operators, and corporate enterprises the associated operating costs. Niall Robinson, chair of the PICMG AdvancedTCA300 subcommittee, anticipates ratification of the spec by the end of summer 2006.

Educational programs

In addition to being *CompactPCI and AdvancedTCA Systems'* neighboring booth in the PICMG showcase, Kontron had its own booth. The company provided technology sessions on two topics in the GLOBALCOMM Exploration Theater:

- Changing the telecom landscape with standardized hardware and software building blocks
- MicroTCA – A system level revolution for edge and enterprise communications

Kontron's Sven Freudenfeld, responsible for North American business development for AdvancedTCA and AdvancedMC modular solutions, attributes the mobile infrastructure market as one driver of the growth in AdvancedTCA. Today, 66 percent of cell phones have cameras. Using AdvancedTCA, CompactPCI, and MicroTCA as reusable infrastructure standard building blocks will allow carriers to meet the anticipated \$42.5 billion growth in the MMS market.

Continuous Computing acquired Trillium in 2003. And, they have also taken on the task of updating the famous Trillium poster to illustrate today's protocols in the telecom network infrastructure including IMS, VoIP, SS7, and SIGTRAN, to mention only a few. To request your own copy, go to www.ccpu.com/poster.

David Asher, Director of Business Development, NMS Communications, mentioned NMS is planning to host a program in Arizona in October that will target key business and technical decision makers who wish to learn more about the telecom market, innovative applications, trends, and NMS products. If you are interested in attending, visit their site.

More to come

This show is so large that I can't cover it fully in the space of this column. Watch future *Software Corner* columns for infor-

mation on the several new advancements in the carrier grade software arena such as:



- Solid's always on database
- LongBoard's SIP standard-based server software for seamlessly handing off voice calls between cellular and WiFi networks
- BEA's J2EE-SIP-IMS application software
- Jaluna's multicore visualization software allowing an RTOS to run alongside Linux unmodified, without performance degradation

Mercury Computer Systems' John Moore, Systems Applications Engineer, and Paul DeBruyn, Account Manager, (left to right, fifth photo from top in gallery) were among the vendors with products at GLOBALCOMM and not-yet-announced products waiting in the wings. That's the case with products Mercury is working on with recently acquired Momentum Computers. Several companies are working on products that they weren't ready to announce at this show, so stay tuned.

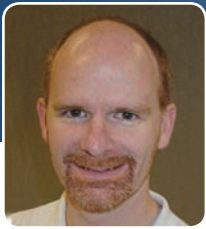
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Addressing network surveillance challenges through virtualization technology

The ever-increasing importance of the Internet in our daily lives continues to dramatically influence the way we all live, play, learn, and work. Network protection has advanced to the point where *perimeter* devices such as firewalls and Virtual Private Networks (VPNs) can help prevent unwanted intrusion into business local area networks or computers. But, how do we go about addressing security threats that reside inside the network? Examples of these threats include network abuse/misuse, cyber crime, identity theft, and terrorist activity. Deep packet inspection is a key ingredient for solutions to identifying these kinds of threats within the network. In this column, we will look at how IP Fabrics, Inc. uses their *virtualization technology* to fight these security threats *inside* the network. Thanks go to Kevin Graves, chief technology officer at IP Fabrics, Inc., for providing information and insight.

How does network surveillance work?

At the most basic level, computers identify themselves over the Internet using an IP address. Therefore, at first glance, it seems simple enough to create a system that sifts through packets on a network tap looking for the IP addresses of interest. Unfortunately, IP addresses are almost always allocated dynamically. The use of Dynamic Host Configuration Protocol (DHCP) is the widely accepted approach to assigning IP addresses to hosts. But DHCP is not the only protocol. VoIP uses H.323 standards to make and break connections. Session Initiation Protocol (SIP) is another *session setup/transfer/follow me* protocol. So, how can the surveillance occur if the addressing and connection information is uncertain? Answering this question leads to a surveillance system comprising two components. The first is called the User Identification (UI) component. The UI component is responsible for determining the addressing and connection activity for a given host name of interest. While the specific address identifier in this example is an IP address, it could be a number of things: A user name,

host name, or call identifier for VoIP. The UI component of the surveillance system must be flexible enough to identify users within multiple types of Internet-related protocols.

Once the UI component has identified the address and connection information of the party under surveillance, the second part of the surveillance system kicks in. We will refer to this component of the system as the Packet Traffic (PT) analyzer. The PT analyzer leverages UI-provided addressing and connection information to filter out everything except traffic addressed to or from the person under surveillance.

The UI component tends to be very protocol aware and must support a variety of session establishment protocols, such as dynamic host configuration protocol as well as SIP, FTP, and H.323. Many session establishment protocols are stateful. The user ID component must follow the state machine of these protocols to determine the address and connectivity of the user in question.

The PT analyzer monitors the actual data flows of specific connections, detects malicious or illegal activity, keeps statistics, and takes action when items being looked for in the content are found. It is very important that the PT analyzer be able to maintain deep packet inspection anywhere from hundreds of MBps up to a Gbps on links within the network.

Surveillance equipment approaches

In order to provide line-rate, deep content inspection capability needed for packet traffic analysis, surveillance equipment may incorporate:

- Parallel processing of the packets through multicore CPUs or network processors
- Fixed-function acceleration, for example encrypt/decrypt units, hash units, and Ternary Content Addressable Memories (TCAMs)

- Various memory types to accelerate processing either for lookup and/or content inspection
- Various buses and interconnects to other acceleration silicon
- Interaction with other system elements at the control or management plane

Often the design combines multiple items from this set of approaches to balance cost, time to market, and flexibility. One thing these methods have in common is increased software development complexity on the new-age boards needed to meet wire-speed deep packet processing requirements.

Network processors have an inherent affinity for this kind of application, because they:

- Are optimized for packet processing
- Incorporate a high degree of parallelism
- Provide bus interfaces and interconnects to various memory and silicon types

What's more, the operation of the parallel compute engines is programmed into the part using an instruction set optimized for the network processor, enabling network processors to lend themselves to maximum flexibility.

While network processor components offer many benefits to network equipment developers, they come at a potential cost. Programming the parallel compute engines and software integration and test of the parallel environment can introduce a learning curve and lengthen the development cycle, not only during design and implementation but during the test and validation phase as well.

Kevin points out another drawback: The lengthened software development cycle can mean a functional prototype is unavailable until late in the project cycle, which delays integration and overall

system functional and performance modeling. In conjunction with the complexity, developers may hesitate to modify or enhance working designs due to the risk of performance or functional timing changes causing problems within the highly parallel environment.

IP Fabrics uses virtualization technology to manage this complexity. Specifically, programmers implement runtime software and tools that abstract the underlying Network Processing Unit (NPU) hardware and parallel processing environment using a Virtual Machine (VM). It is a very interesting and compelling notion. Java has been an enabler in the proliferation of Internet-connected software. Why not apply the same principles to network surveillance systems? Implementing a VM on top of a network processor provides the programmer an architecture-independent environment that provides portability and scalability. Further, since the VM is already implemented and tested on the network processor, functional prototypes can be ready for initial integration within hours, which greatly lowers development risk and shortens integration and test time.

In Figure 1, we can see how the virtualization concept works:

1. The developer writes a program using packet-processing policies in a high-level language.
2. The compiler builds the VM *byte code* from the program source that the VM will use to run packet-processing instructions on all the compute engines of the network processor.

This approach eliminates the timing and logic complexities related to parallel programming environments by incorporating these notions directly into the VM.

Using virtualization technology for network surveillance

Now that we have looked at surveillance system requirements and virtualization technology, let's put it all together.

Turning our attention to the packet traffic analyzer, it must:

- Monitor specified packet flows
- Perform flow lookups to get state information

```

ipv4_filter: Policy classify
  DATABASE(PKT_TRAFFIC_IPV4_FILTER_DB_NAME)
  DATA(PKT_TRAFFIC_IPV4_FILTER_DB_DATA_PARAM)

ipv6_filter: Policy classify
  DATABASE(PKT_TRAFFIC_IPV6_FILTER_DB_NAME)
  DATA(PKT_TRAFFIC_IPV6_FILTER_DB_DATA_PARAM)

event(SM_EVENTNUM)

rule eq(IP_VERSION,4)
  apply(ipv4_filter)
  eq(REG_PPL_RTN,FuF)
  jump(miss_disposition)

rule eq(IP_VERSION,6)
  set(REG_IPV6_SOURCE,IP_SOURCE)
  set(REG_IPV6_DEST,IP_DEST)
  apply(ipv6_filter)
  eq(REG_PPL_RTN,FuF)
  jump(miss_disposition)
    
```

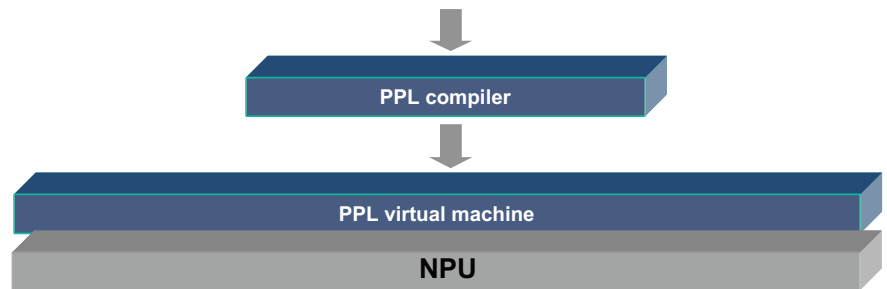


Figure 1

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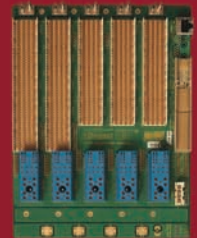
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Generally, the programmer of the PT analyzer must program the processor to first classify the packet to determine if it is a packet of interest. If it is, perform a flow/session lookup to determine if the packet is part of a session already being monitored. If not part of an existing session, the packet traffic analyzer software must allocate and initialize a session entry for this packet. Lookups are often performed on the IP packet five-tuple (IP source and destination address, protocol, and Layer 4 source and destination ports). Sometimes lookups are performed on a Virtual LAN (VLAN) tag. Since session tracking may include up to one million independent flows, the session table typically requires some kind of hash table, further complicating the packet analyzer design and implementation.

Expressing this logic using assembly language code takes thousands of lines of code involving the packet logic noted earlier as well as code to deal with the parallel processing environment (mutual exclusion and semaphores to prevent table entry allocation duplication, and so on).

Implementing the logic in C is also a challenge. C does not include constructs for parallel computing, so the developer must incorporate these things in the design and implementation. Further, the lack of a *parallel engine operating system* requires the C programmer to interact directly with the hardware. Efficient pay-

load scanning and pattern matching can also be extremely complex. Programming effective algorithms involves researching and coding state-of-the-art algorithms in order to take advantage of every cycle in the hardware.

The IP Fabrics virtualization approach uses a high-level programming model that provides a set of built-in algorithms (which they call policies in the language) optimized for the hardware it runs on and incorporating the latest optimized algorithms that can be simply and directly invoked by the program running on the virtual machine. Algorithms built into the virtual machine include connection lookup, header encapsulation or de-encapsulation, rate monitoring, and content inspection using strings, regular expressions, or a patterns database, to name a few. IP Fabrics DeepSweep™ product uses virtualization technology for network surveillance at gigabit data rates (Figure 2).

When asked about overhead of the virtual machine, Kevin mentions that the virtual machine uses highly optimized, best-of-breed algorithms in addition to the VM architecture using both pipelined and parallel processing across the compute engines. In turn, these hand-tuned aspects of the virtual machine will often outperform those written by general purpose network processor software developers. The more complex the processing becomes, the higher performance the virtual machine achieves when compared with complex network processor software implementations.

“As network surveillance requirements continue to drive more surveillance systems deeper into the network, it will be interesting to see how virtualization technologies can revolutionize line-rate, complex packet processing for these applications.”

When asked about future products from IP Fabrics, Kevin alluded to plans for a series of network surveillance products using IP Fabrics' virtualization technology. Like network processors, the new Intel and AMD multicore processors could also be targets for IP Fabrics' virtualization technology.

Conclusion

As network surveillance requirements continue to drive more surveillance systems deeper into the network, it will be interesting to see how virtualization technologies can revolutionize line-rate, complex packet processing for these applications. Virtualization technology aims to remove complexities in the development cycle, shorten time to market, and enable system engineers to bring better, faster, more flexible products to market sooner.

For more information, contact Curt at cschwaderer@opensystems-publishing.com.



Figure 2

More on IP Fabrics:

www.ipfabrics.com

More Software Corner columns:

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Alone up in the air

The ILA2006 Berlin Air Show held May 16-21 is always a good place to see new things that move through the air. Approximately 250,000 visitors (25 percent more than last year) had the opportunity to see the Airbus A380, the world's largest commercial aircraft, and the Barracuda, an Unmanned Aerial Vehicle (UAV) from EADS (Germany and Spain). The Barracuda is a heavyweight UAV at 3.25 metric tons, including the CompactPCI-based mission control system. It is very large at approximately 8.25 meters (26 feet) in length with a wingspan of 7.22 meters (23 feet). This jet-powered UAV is propelled by a turbine delivering 14 kilonewtons of thrust. It is the largest UAV built in Europe by European companies. It successfully flew over southern Spain prior to being shown in Berlin. This is not a rebuilt aircraft. It was designed from the ground up to become a UAV for commercial and military applications.

EADS and industrial partners such as SBS Technologies Europe built this high-performance, all-electric plane in an extremely short time by using COTS products with a proven record of reliability and high availability. The body was completely built from EADS patented Carbon-Fiber Composites (CFC) to save on dead weight, leaving more weight for scientific or military payloads. Except for the landing gear, everything is controlled electrically (steer-by-wire), not using any hydraulics. The wings are exchangeable to suit different types of operating conditions, such as slow-speed sailing at high altitudes or precise contour following very low above ground at very high speeds.

The Barracuda UAV operates completely automatically and autonomously (including takeoff and landing) based on mission data uploaded into the onboard advanced mission system. Plans call for many different applications including *network-centric operations* and *intelligent UAVs* that can switch from surveillance to reconnaissance or completely change the mission during unmanned flights.



Figure 1

Figure 1 shows the Barracuda alone on another mission without remote control guidance.

Engineers from SBS Technologies in Augsburg (Germany) built the Mission Management Computer (MMC) under contract directly from EADS. The rugged enclosure (AVC series) is equipped with four CompactPCI 3U backplanes (22 slots total), arranged in a dual redundant configuration in two sections. A four-port Ethernet hub provides redundant communication between the modules (boards) in the system in addition to the CompactPCI parallel bus. The enclosure and boards are all conduction cooled. The two CPU boards (CM4) are 3U PowerPC SBCs. Two dual-channel boards provide the 1553 interfaces, and a digital I/O board handles various functions. Two power supplies feed the two redundant computer sections.

SBS Technologies supplied a mission-ready system completely tested and equipped with board support packages for use with the VxWorks real-time operating system from Wind River Systems, Inc. The electronic systems on the UAV jet are built in an open architecture configuration from commercially available products. This approach generates a versatile system that adapts quickly to widely differing applications. The CompactPCI backplanes built by SBS Technologies for EADS have a large number of empty slots remaining to be equipped with different modules for a variety of missions.

Ready for (virtual) launch

Launching a missile is an expensive operation. Simulating it with electronics and software is obviously much less costly. MEN Micro Elektronik GmbH (Germany) has built a 3U CompactPCI system for a government institute, using seven CPU boards in one 19-inch chassis. One of these CPUs acts as a control unit and the other six CPUs are execution units. The communication load is very high. That is why six Ethernet dual-channel PC•MIP (ANSI/VITA 29) mezzanine modules (P16) on two PC•MIP carrier cards are required in addition to the Ethernet channel on the CPU card. Digital I/O channels and a motion counter are implemented on M-Module (ANSI/VITA 12) mezzanines. The M81 module provides 16 output channels (0 V and 36 V, up to 500 mA each) and the M82 module has 16 input channels (0 V to 40 V). The motion counter M-Module (M72) has four independent cascadeable 32-bit channels (optically isolated) usable as timers, counters, or comparators.

For more information, e-mail Hermann at: hstrass@opensystems-publishing.com.

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Next-generation network management: Is NETCONF a magic bullet?

By Carl Moberg

As network infrastructures grow more complex, so do the demands placed on networks. In this complex landscape, efficient network configuration and provisioning are crucial components of a successful network. Yet the wide range of current methods lacks cohesiveness. For instance, a slew of device-specific Command Line Interfaces (CLIs) exists, each with its own specifications for session establishment, user authentication, configuration data exchange, and error responses. The absence of standards across – or even within – systems makes it difficult to manage networks efficiently and without errors. The IETF recently approved a device configuration protocol, NETCONF. In this article, Carl assesses both NETCONF and the challenges it addresses.

Increasingly complex network architectures

A range of internal and external pressures contributes to the increasingly complex network architectures in many enterprise environments. As businesses continue to grow in population, locations, and range of services, their networks must keep pace. The addition of new offices, points of presence, or data centers results in additional architectural issues that increase the complexity of the organization and the network. For example, company growth through acquisition typically adds new sites to the company Virtual Private Network (VPN), which requires complex network reconfiguration by the VPN service provider.

The horizontal growth pursued by many companies presents a different set of challenges. For example, to attract and retain customers many telephone service providers now offer cable television and Internet service. This presents the challenge of unifying organizations and networks previously conceived as separate entities.

Finally, the network elements themselves present a new level of sophistication. An increased number of heterogeneous elements coexists in the typical network, such as devices that increase capacity, reliability, and security. The added complexity can cause significant management and configuration challenges.

The price of network failure

As the network architectures of network service providers – such as telecom companies, mobile operators, Internet service providers, and even enterprise networks – grow increasingly complex, there is a simultaneous increase in the importance of seamless operation. Network or service outages lead directly to loss of revenue, organizational inactivity, PR nightmares, and the alienation of customers and/or employees, any of which can cost tens or hundreds of thousands of dollars per hour, if not millions, while also creating significant long-term setbacks.

Among other potentially disastrous situations, the loss of control over customers' and subscribers' personal data has become an

increasingly central issue over the past few years. This liability, as well as the misuse of services, such as abuse, fraud, worms, viruses, and other malevolent or vulnerable software, place increased demands on the network architecture. Such network security challenges arise from having complex services that can be abused when misconfigured.

State of the network management arena

In response to the complex networks present in most enterprises, manufacturers of network elements have added management interfaces to their devices, such as specialized CLIs and data stores, allowing network elements to be configured and managed. Unfortunately, each network device must be individually configured to cooperate and communicate with other devices on the network. This hampers long-term network management because of disparate data stores and custom management solutions that make intradevice integration harder to achieve.

While the stovepipe CLIs help to make each device manageable, each CLI leads to higher acquisition and maintenance costs. Consider a network with a brand A router. The system administrator replaces the router with a brand B router. At this point, all A-specific scripts operating on networked devices must be updated to B-specific scripts. A manual update is, as usual, tedious and error prone.

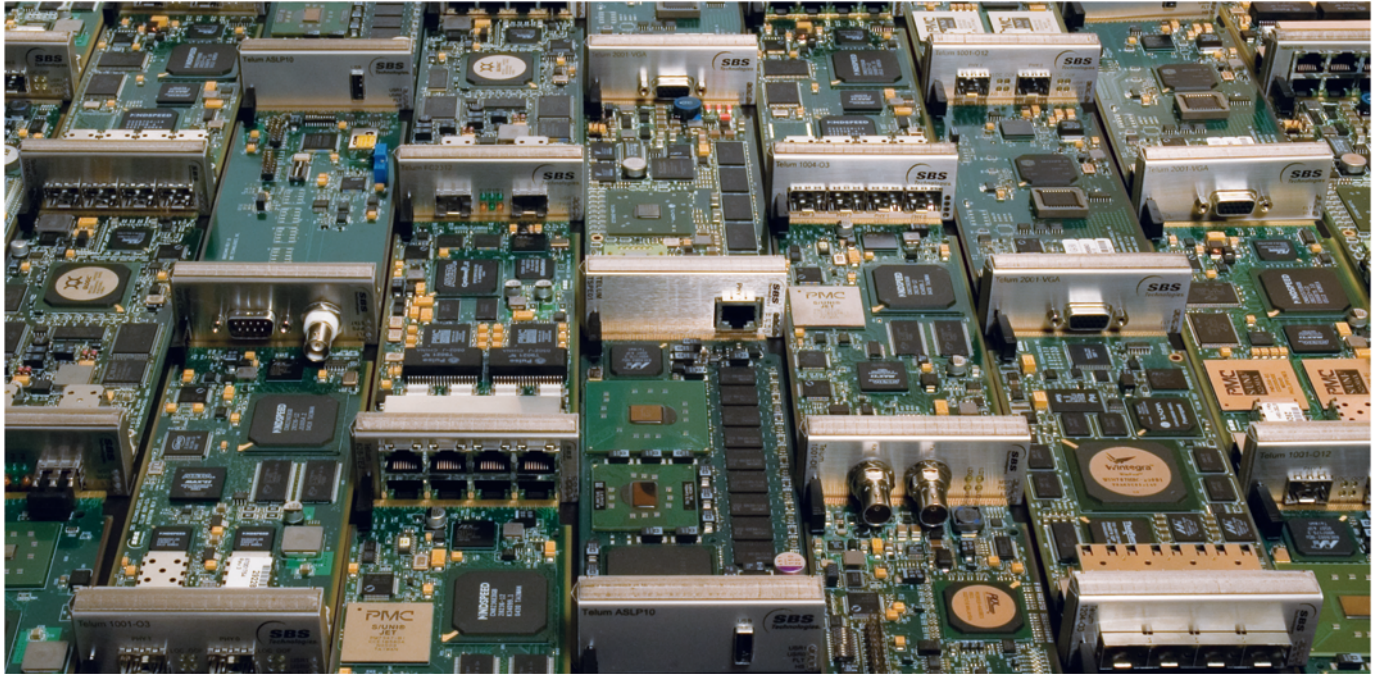
Traditionally, Simple Network Management Protocol (SNMP) has been the standard for remote management. However, certain elements of SNMP make it less suitable for some management tasks. SNMP operates over User Datagram Protocol (UDP), which is unreliable. As such, configuration updates can be a delicate task. As UDP limits message size, large configurations cannot be sent in a single datagram. SNMP uses a protocol-specific security mechanism rather than a standard method such as Secure Socket Shell (SSH). This increases administrator workload and complicates the network architecture. Finally, SNMP is rarely used for writing configurations, as it lacks a standard commit operation for individual devices or groups of network elements.

To scale beyond the current situation of network management, service providers should move to a model in which the network – as opposed to the network elements – is directly managed.

The perfect network management system

We can define the functions of an ideal system by looking at the shortcomings of the prevailing network management challenges. The ideal system would accomplish four primary goals: automation, consolidation, standardization, and formalization.

By automating tasks that are repetitive, tedious, and easily mishandled, the system administration organization would gain



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| TELUM 624/628-TEJ | WAN Edge Access I/O, 4 or 8 port T1/E1/J1, ITDM option | • | |
| TELUM 1001-O12M/S | WAN OC-12 module | • | |
| TELUM 1001-O3 | WAN OC-3 module | • | |
| TELUM 1004-O3M/S | WAN OC-3 module | • | |
| TELUM 1001-DE | WAN DS3/E3 module | • | |
| TELUM 1204-O3 | WAN intelligent AMC.2 multi-service 4-port OC-3 module | | • |
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| AT-AMC2 | AdvancedTCA® carrier for 2-4 AMC.2 modules | | • |
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flexibility, reliability, and efficiency. Consolidation would be achieved via a central management point such as a Network Management System (NMS) or Operations or Business Service System (OSS/BSS). The use of a standard script each time a network element is added, retired, or upgraded would provide standardization.

A formalized system model would rely on the management server for most tasks, such as implementing and checking network configurations and policies. For example, in the router replacement scenario mentioned earlier, the required updates would be accomplished by the server rather than manually.

The new IETF protocol for device management, NETCONF, offers a powerful solution to the problem of network management, as it satisfies all four criteria of an ideal management system.

All about NETCONF

The IETF formed the NETCONF Working Group to standardize network configuration due to the wide range of configuration mechanisms currently in use, each with its own specifications for session establishment, user authentication, configuration data exchange, and error responses.

The Working Group received initial approval of its proposed documents in March 2006. The documents are posted on the

official NETCONF Web page at www.ietf.org/html.charters/netconf-charter.html.

The NETCONF protocol provides the mechanisms for all basic network management tasks, such as installing, querying, manipulating, and deleting the configurations of network devices. Additionally, a management system can use NETCONF to configure or troubleshoot a network element.

NETCONF offers a number of advantages over other approaches to network management. It relies on a standardized programming interface, eXtensible Markup Language (XML), for the configuration of switches, routers, and other network devices, rather than the device-specific scripts used by CLI.

NETCONF offers secure network management: The XML requests and responses are always sent over a persistent, secure, authenticated transport protocol, such as SSH. The use of encryption guarantees that the requests and responses are confidential and tamper proof.

In addition to a secure communication system, NETCONF requires devices to track client identities and enforce permissions associated with identities. Devices can thus be managed over an unsecured Wide Area Network (WAN), a distinct advantage compared to other approaches. Configuration over a

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WAN means that network management can be centralized, yet decentralized: All management comes from a central point, but users at multiple sites can participate in the process.

NETCONF is extensible, future proof, and fairly straightforward to implement, which reduces cost and time to market. NETCONF can be inexpensively provided by devices and straightforwardly used by higher-level management tools, making it a suitable base protocol for management servers.

Tail-f Systems announced the first commercial implementation of NETCONF earlier this year. Its ConfD on-device management solution provides full support for the NETCONF protocol. Shown in Figure 1, the ConfD software can be added to any network device to enable network management. ConfD on-device management software can help service providers and enterprises centralize network management functions.

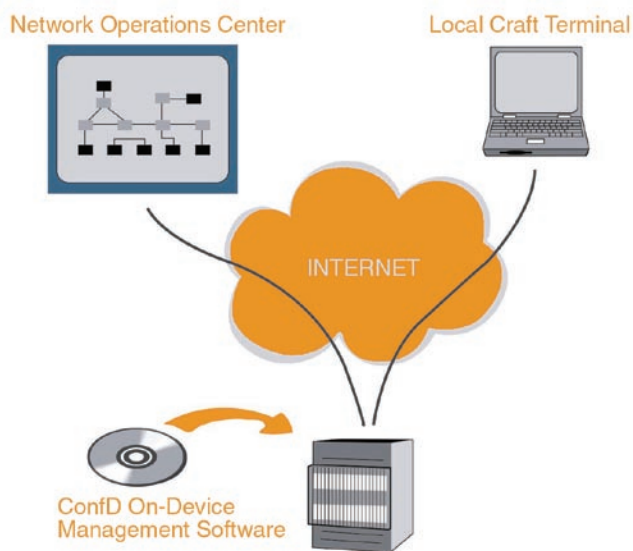


Figure 1

Several top-tier Telecom Equipment Manufacturers (TEMs) are using Tail-f's ConfD on a trial basis. Initial feedback has been positive, especially regarding its flexibility. TEMs may use NETCONF as an add-on with existing products or incorporate it into the development of new products. As standardization of network equipment seems focused on the Linux operating system and MicroTCA/AdvancedTCA hardware, Tail-f's implementation is available preintegrated with the Linux software and MicroTCA/AdvancedTCA hardware of a few key vendors. This production-ready product will allow customers to significantly reduce the costs and risks of network device development.

Conclusion

The current state of network management presents a fragmented landscape in which most network capabilities are embodied in a collection of unique scripts rather than in a data model. As such, network management – a crucial issue for all businesses – relies on costly and high-risk manual configuration.

To equipment vendors, NETCONF is a way to outsource the management interface of network elements. To service providers, NETCONF is a way to optimize the administrative work flow, by moving management intelligence away from the device to a consolidated management function. 🌐



Carl Moberg is vice president of engineering at Tail-f Systems. Prior to joining Tail-f he was the director and cofounder of Product Management at ServiceFactory. Before joining ServiceFactory he worked at Telia, where he was one of the principal architects of the company's Internet service platform. Carl holds a degree in Electrical Engineering from the Royal Institute of Engineering in Stockholm.

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Designing scalable DSP parallelism for AdvancedTCA systems

By *Todd Hiers and Greg Tiedemann*

In the next few years, the overall increase in networking and growth in new services, including video, means that next-generation telecommunications carrier equipment will have to be designed for both high-speed processing and flexibility. High-performance programmable Digital Signal Processors (DSPs) have already demonstrated their value in telecom designs by enabling massive throughput while also being able to handle a variety of protocols, codecs, management tasks, and other types of software with a simple change of code. DSP architectures with glueless high-speed interprocessor communications via the Serial RapidIO bus enable code partitioning and permit a variety of topologies, making it easy and cost-effective to rescale DSP systems through parallelism.

The AdvancedTCA specifications provide an excellent platform for designing parallel multiprocessor DSP systems. Designed for performance, flexibility, and scalability, AdvancedTCA supports these features in multiprocessor DSP designs. Todd and Greg examine how AdvancedTCA, parallel DSPs, and Serial RapidIO reinforce each other in the creation of high-performance scalable designs for next-generation telecom carrier equipment. The discussion will include an example design that can be used directly or adapted by telecom equipment developers.

The trend in delivery of high-bandwidth digital services that began in the last decade continues to grow. Telecom carriers are aggressively offering their business and residential customers new services that add to the overall network load even as they provide the desired revenue streams. Packet-based switching, wired and wireless network convergence, and new delivery methods for voice are just some of the technologies being rapidly deployed, a mix that also includes data and video. These choices have changed

the dynamics of the telecommunications environment. With the combination of new and traditional services and many standards still emerging, there is demand for greater throughput and capacity, and we are also seeing more network complexities emerge.

In this ever-growing, ever-changing environment, telecom service providers and OEMs must look for ways to keep their risks to a minimum as they adopt new technologies. Design criteria that can reduce risks for next-generation infrastructure equipment include:

- Providing greater high-speed processing for more and wider channels
- Supporting multiple products and configurations from a single platform
- Allowing network configurations to be changed efficiently as service offerings evolve

These goals – performance, scalability, and flexibility – can be addressed only through a range of enabling technologies that operate together and reinforce each other from the component to the system level.

Complementary technologies

At the component level, a simple change in the code enables high-performance programmable DSPs to repeatedly demonstrate their value in telecom design by handling both massive throughput and a variety of protocols, codecs, management tasks, and other types of software. More recently, new DSPs have appeared that strengthen their utility in infrastructure designs with telecom-specific architectural enhancements, including integrated Serial RapidIO interfaces that enable greater parallelism through high-speed interprocessor communications. DSP farms that are based on multiple processors support code partitioning for greater throughput, and permit a variety of topologies, making it easy and cost-effective to

rescale infrastructure systems as service demands increase.

A number of Tier 1 telecom OEMs developed the AdvancedTCA specification to provide greater system performance, scalability, and flexibility than existing standard form factors such as CompactPCI afforded. In addition, broad adoption of AdvancedTCA by the telecom OEMs and support from a wide variety of suppliers has provided an industry-wide specification that will drive efficiencies of scale and keep individual manufacturers from repeatedly having to develop ancillary solutions such as cooling. Comprising the PICMG 3.x family of standards, AdvancedTCA includes mechanical, power, thermal, and management connectivity specifications, connector zones, and features, and several fabric-specific subsidiary interconnect specifications, among them RapidIO and Ethernet.

The AMC.x specification that PICMG developed for Advanced Mezzanine Cards (AdvancedMCs) further enhances AdvancedTCA's flexibility by extending its high-bandwidth, multiprotocol interfaces to hot-swappable modules that are directly connected to the system switching fabric through carrier bays. AdvancedTCA carrier bays populated with multiple AdvancedMCs provide an easy method for adding compute processing and modifying system configurations. As a result, telecom equipment OEMs and their customers have a versatile platform for designing, manufacturing, scaling, upgrading, and servicing modular infrastructure systems at a much lower cost.

Designing DSPs for telecom

A high-end DSP architecture that was created for use in AdvancedTCA and other high-end systems is the basis for the TMS320C64+ DSP family from Texas Instruments. The C64+ DSP core is capable of achieving up to 8,000 Million Multiply-Accumulates per Second (MMACS), doubling the multiplication

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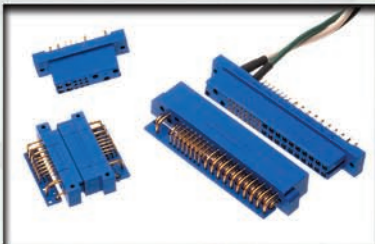
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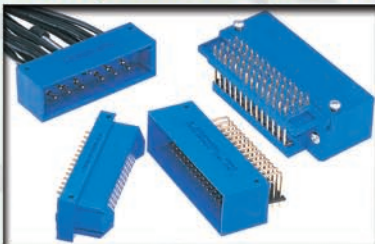


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bandwidth and thus providing a high level of real-time computation for telecom algorithms. The core instruction set includes extensions for telecommunications such as Finite Impulse Response (FIR) filters and Fast Fourier Transforms (FFTs) that can achieve up to 20 percent cycle count reduction over the previously introduced C64 DSP core, while 16-bit instructions and a software pipeline loop buffer can reduce code size by up to 30 percent. (See Figure 1.)

A large 2 MB on-chip memory serves for direct-mapping, or a cache, or both, as controlled by the program. Fast external memory access takes place through a DDR2 interface. An Enhanced Direct Memory Access (EDMA) controller switches up to 64 channels simultaneously with a cumulative data flow of up to 2.4 gigabytes per second (Gbps). The integrated Gigabit Ethernet Media Access Controller (MAC) provides a direct high-speed interface. (The C64+ DSP family also includes video-specific enhancements and peripherals that are opening up the digital video industry by making a new range of media applications more affordable for mass-market production and distribution.)

Texas Instrument's C64+ DSPs were the first to integrate a high-speed Serial RapidIO interface, supplying the means for interprocessor control and data

communications in scalable parallel-processing applications such as DSP farms for telecommunications. With packet-switched data rates up to 10 Gbps in a full duplex bus, RapidIO enables chip-to-chip and board-to-board communications in performance levels scaling to 20 Gbps and beyond. Peer-to-peer connectivity that makes it much easier to implement multiprocessing also helps decrease overall system cost and increases reliability by reducing the need for additional devices used for switching and processor aggregation. The inherent flexibility of RapidIO allows it to be used in ring, star, and mesh topologies. Multiple DSPs can be connected through a switch, with or without local connections to one another and to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs).

DSP programming flexibility enables OEMs and application developers to keep pace with changing standards and, if necessary, to implement multiple codecs in wireless and wireline infrastructure equipment. The C64+ DSP family is code-compatible with earlier generations of C6000 DSPs enabling the reuse of intellectual property. Foundation software, tools, and algorithms are available to speed system integration and the development of new code. Complex telecom infrastructure equipment that makes use of these programmable DSPs meets

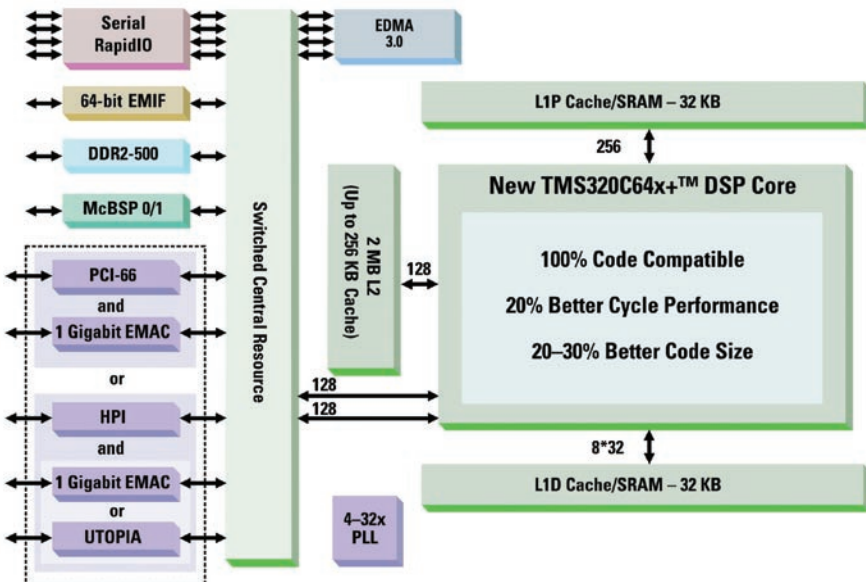


Figure 1

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the processing requirements of high-bandwidth delivery and helps service providers test, deploy, and update new service technologies affordably and with minimal risk.

Bringing technologies together

An example of how AdvancedTCA and DSP technologies complement each other to provide performance, scalability, and flexibility can be found in the Ensemble2 application platform from Mercury Computer Systems. As a standards-based system for developing, prototyping, and deploying applications, the Ensemble2 platform supports a wide variety of AdvancedTCA-based data plane applications that require functions such as:

- Media encoding and decoding
- Channel encoding and decoding
- Protocol termination and conversion

The system scales effortlessly from small-scale MicroTCA solutions to 2-, 5-, and up to 16-slot AdvancedTCA configurations.

Supporting up to 48 AdvancedMC modules, the Ensemble2 platform employs heterogeneous processing and provides a wide range of modular configurations for different types of applications. A hub card with RapidIO fabric switching and Gigabit Ethernet base switching handles up to 80 Gbps of capacity to support inter-chassis and inter-shelf bridging with Serial RapidIO delivering up to 10 Gbps to every processing component in the system. (See Figure 2.) Each carrier bay provides a fabric and base switching connection for up to four full-height, single-width AdvancedMCs in a variety of combinations. Available AdvancedMCs provide DSP and communications processor functionality, FPGAs for I/O, and interchassis connectivity. (See Figure 3.)

The three Texas Instruments designs for AdvancedMC module designs are all based on its 1 GHz TMS320TCI6482 DSPs. The simplest of these, the MTI-101 module, is designed specifically for application developers who want to characterize the performance of the DSP in AdvancedTCA. The MTI-101 integrates a single DSP, Gigabit Ethernet connection for control. It uses a 4x Serial RapidIO data link that is also decomposable to four 1x links. Rescaling this basic design

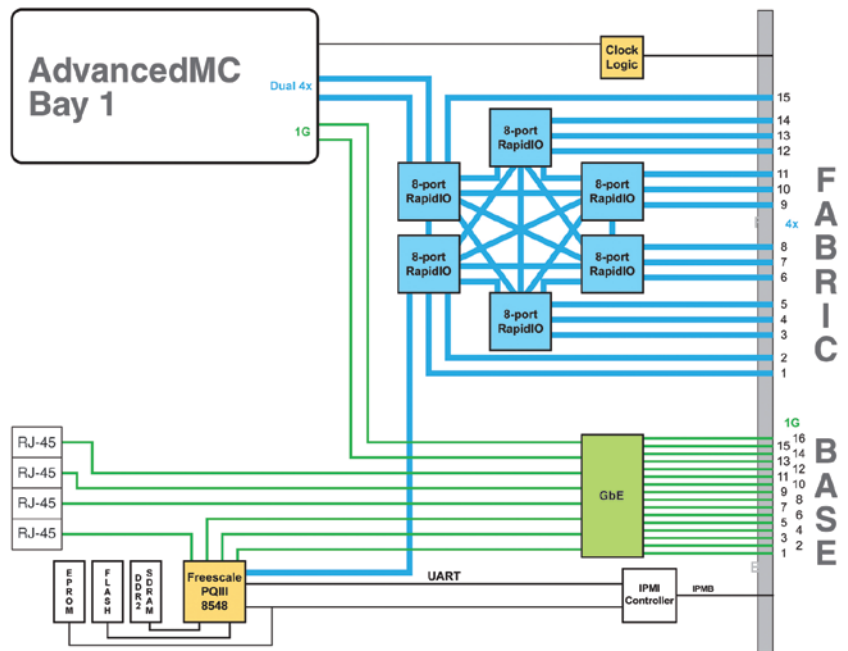


Figure 2

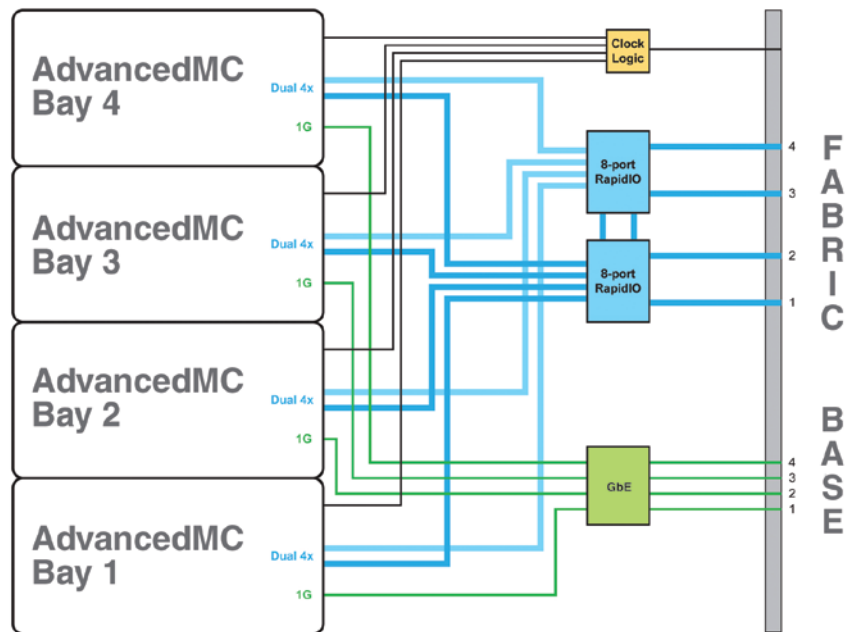


Figure 3

into a DSP farm is the MTI-104 module, which integrates four DSPs, two Gigabit Ethernet connections, and eight 1x Serial RapidIO ports. MTI-104 cards allow the DSP farm to be scaled easily, providing up to 16 devices in each carrier bay. (See Figure 4.) A final DSP-based AdvancedMC, the MTI-203 module, is designed for WiMAX/802.16e wireless infrastructure applications, with three

integrated DSPs, FPGA, dual Gigabit Ethernet, and with 4x RapidIO connectivity to each of the DSPs and the FPGA. (See Figure 5.)

The three DSP cards indicate how effective the combination can be of DSP multiprocessing, RapidIO high-speed interconnect, and AdvancedTCA system technologies. For Mercury, designing the

“Complex telecom infrastructure equipment that makes use of these programmable DSPs meets the processing requirements of high-bandwidth delivery and helps service providers test, deploy, and update new service technologies affordably and with minimal risk.”

single-DSP MTI-101 into the quad-DSP MTI-104 was a straightforward issue of rescaling, and changing the latter into the MTI-203 involved largely software and I/O modification for wireless application. By using TI-supplied foundation software, algorithms, and network stacks, Mercury was able to focus its own software development where its expertise is greatest, on system-level control and integration. Mercury customers, in turn, are able to add value in applications without being concerned about reprogramming the processor or the essential system.

Of interest to application developers, the Ensemble2 platform supports either a heterogeneous or a homogeneous OS environment, such as Linux and OSE among others. A Linux-based system management software suite leverages RapidIO’s robust in-band management features, providing support for features such as real-time performance monitoring, event trapping in the switch complex, and the detection and mitigation of error effects. Shell-based tools offer flexibility in exploiting RapidIO’s maintenance mode, as well as providing a graphical interface to the switch fabric and unique visibility into the configuration and performance of the system. Through both software and hardware, the platform enables developers to quickly and cost-effectively create new types of functionality for telecom infrastructure equipment.

Reduced risk in a changing environment

The fast-paced telecom environment requires technologies that can reduce risk by providing performance for a high level of service throughput, scalability for

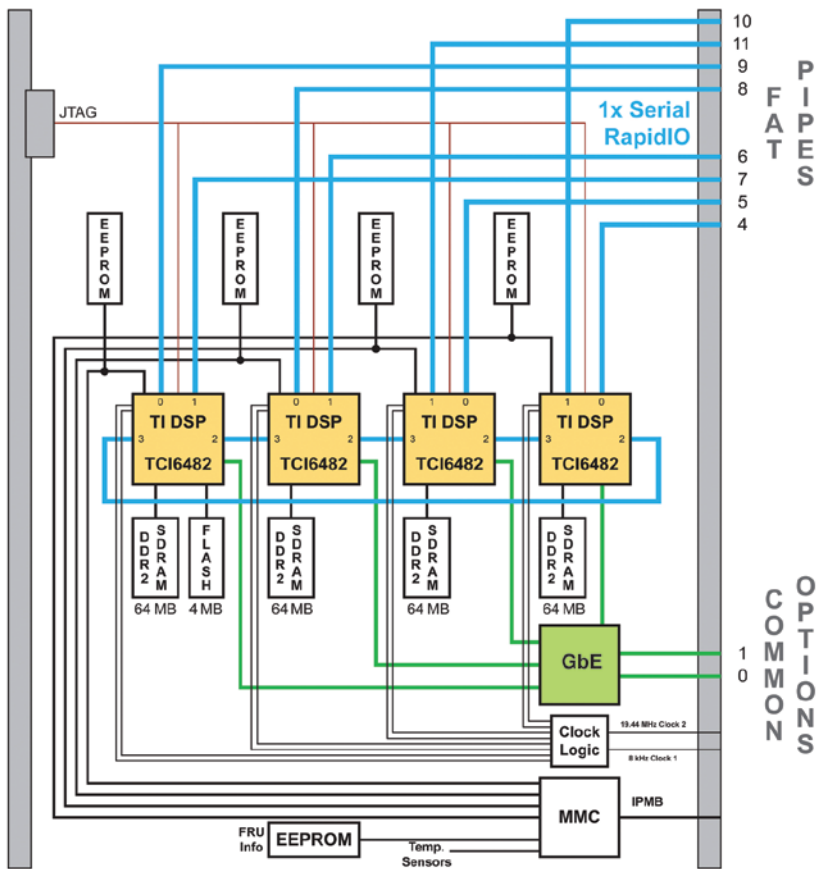


Figure 4

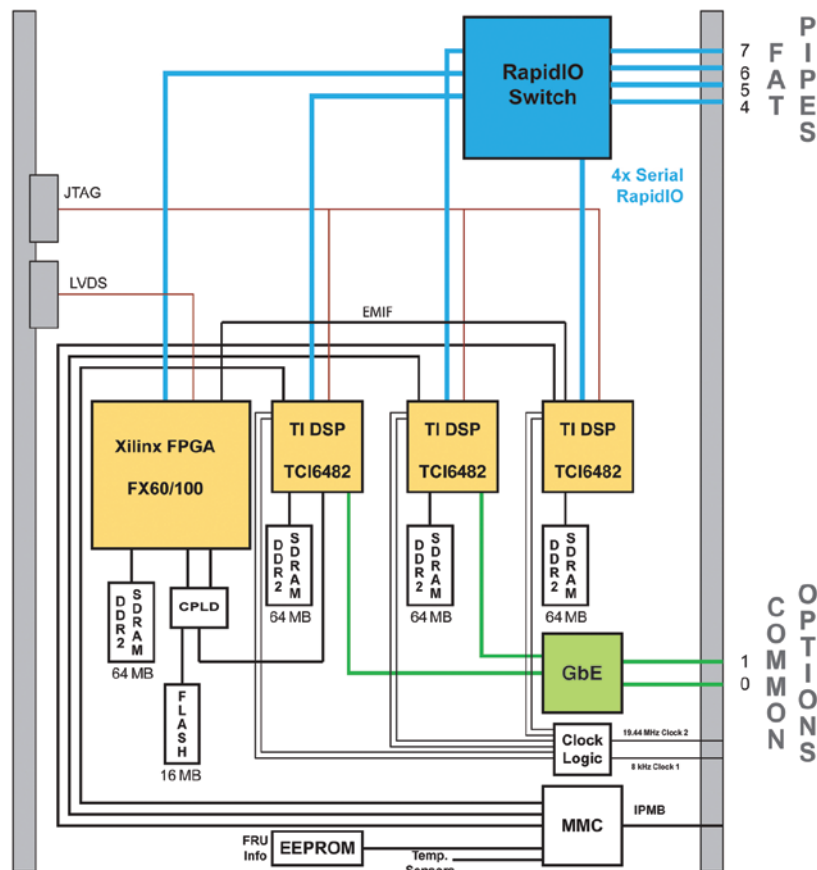



Figure 5

creating different products and applications from the same platform, and flexibility for modifying configurations as network conditions change. No single technology does everything in a complex telecom system, but high-performance programmable DSPs and AdvancedTCA system architectures provide complementary technologies that enable the creation of leading-edge

modular products for network infrastructure. AdvancedMC modules with multi-processor DSP farms communicating via high-speed RapidIO interfaces allow easy system rescaling and reconfiguration that support versatile applications. In tomorrow's networks, AdvancedTCA equipment that leverages DSP parallel performance will be unparalleled. 



Todd Hiers is a senior applications engineer with the Catalog DSP Application team at Texas Instruments focusing on high-speed hardware and

video infrastructure systems. He joined the TMS320C6000 Hardware Applications team as an intern in 1998 and a full-time employee in 2001. He has created technical content for and supported multiple generations of devices in the C64x family of DSPs. He has recently worked on verification and validation of the new C645x devices, including new high-performance modules such as Serial RapidIO. Todd has a BS and an M.Eng. in EECS from MIT.



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Prior to joining Mercury, he spent nearly 10 years with Ericsson. Greg is a member of the RapidIO Trade Association Marketing Working Group and heads the Ecosystem & Interoperability Subcommittee. He has a BS in Mechanical Engineering from Tri-State University, Indiana.

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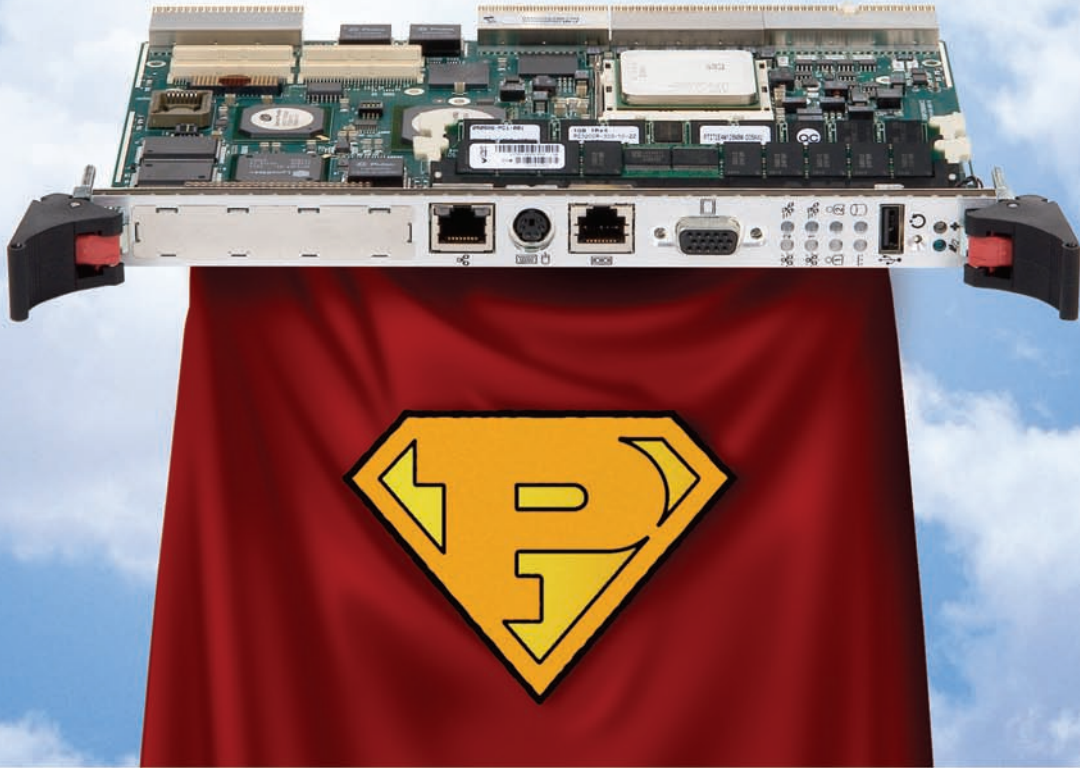
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High performance view: CompactPCI Express

By *Steve Cooper*

The next generation of CompactPCI is beginning to roll out in the form of CompactPCI Express. This upgraded standard includes substantial performance increases, compatibility with both legacy products and the latest office PC technologies, and a unification of backplane buses into a single bus that supports both CPU-to-I/O and CPU-to-CPU communications. The first products based on this new standard, including those in the CompactPCI Express Product Guide that follows, are now beginning to appear, and represent the first look into this powerful architecture of the future.

Historical perspective

The PICMG standards body developed CompactPCI in 1996 as a standard bus structure that combines the cost-effective PC bus architecture (PCI) with the popular Eurocard industrial board form factor. This combination quickly became the world's most popular bus structure for industrial, communications, military, and test systems where PCI is used in a rugged form factor. In 2005, PICMG defined a new CompactPCI specification that replaces the PCI bus with the new PCI Express bus.

The addition of PCI Express to the CompactPCI standard allows CompactPCI Express to utilize the latest PC market components, extending the bus architecture's useful lifespan for at least the next decade.

Products based on the new standard are now becoming available, with many more product announcements anticipated over the next several months and years.

Benefits of CompactPCI Express

CompactPCI Express brings several higher-performance benefits to traditional CompactPCI applications, including:

- Bus transfer speeds increase 10-50 times
- PCI Express connections are all point-to-point, eliminating arbitration delays
- CPU-to-CPU transfers can occur at the full bus bandwidth
- No need to run relatively slow Ethernet through the backplane

Compatibility with legacy boards and chassis

Hybrid systems that include a mix of CompactPCI Express as well as legacy CompactPCI slots are easily implemented. CompactPCI and CompactPCI Express boards are the same form factor and include the same faceplates and other mounting hardware, so existing chassis need only upgrade their backplane to be used in CompactPCI Express.

Low costs through access to the latest commodity components

The latest I/O components that include native PCI Express interfaces can be easily designed into new CompactPCI Express

I/O boards. Figure 1 shows a dual Gigabit Ethernet component with a native PCI Express interface in the new CompactPCI Express form factor.

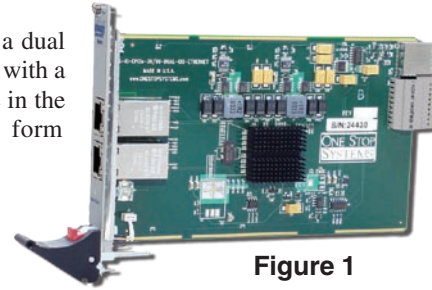


Figure 1

New capability to run PCI Express over cable

The CompactPCI Express architecture enables attached PCs to control a CompactPCI Express subsystem at full speed and with full software transparency.

Bus unification, improved multiprocessing, and fault tolerance

Incorporating Advanced Switching (ASI) extensions to PCI Express, CompactPCI Express supports both CPU-to-I/O and CPU-to-CPU communications over the common backplane, creating a cost-effective upgrade path for PICMG 2.16 applications.

CompactPCI Express basics

CompactPCI Express replaces the P1 and P2 connectors used in CompactPCI with four connectors that provide the new PCI Express bus as well as enhanced power capabilities to each board, as shown in Figure 2. The bottom connector provides high current connections for incoming power; the second and third connectors provide the PCI Express differential pairs for multiple PCI Express buses to be routed from each board to the backplane. The top connector provides utility pins for user-defined rear I/O, PXI extensions for instrumentation, and power input for the low-cost Type II I/O modules.

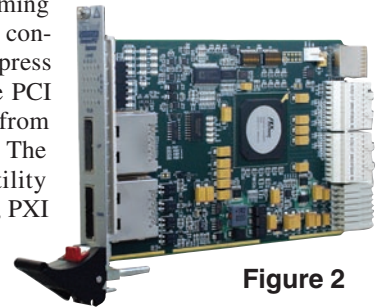


Figure 2

System slot boards within CompactPCI Express drive either two or four PCI Express buses onto the backplane.

This allows the direct connection of up to four I/O slots. For larger configurations, a switch is needed to expand the PCI Express fan out to additional I/O slots. Figure 3 shows an eight-port switch board.

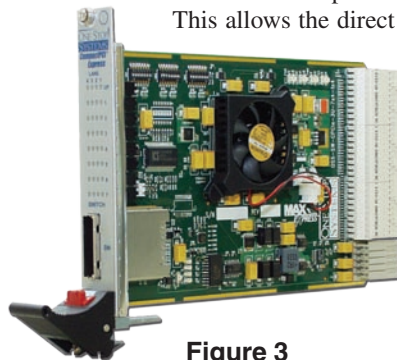


Figure 3

A bridge board can connect one PCI Express port to traditional PCI, enabling hybrid systems that contain a mix of CompactPCI Express and legacy CompactPCI slots. Figure 4 depicts a 6U CompactPCI Express backplane that supports this hybrid architecture.

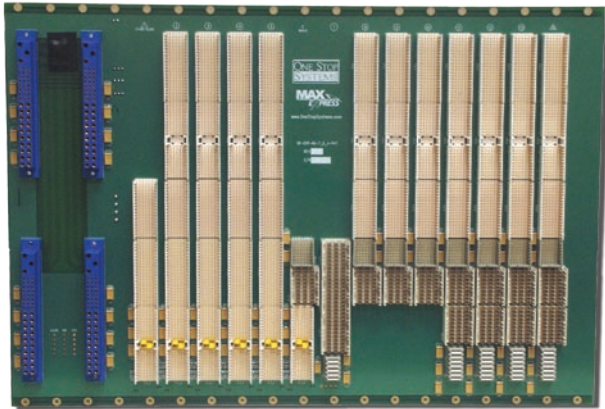


Figure 4

Support for both internal and external CPU

New PCI Express capabilities include running the bus at full performance with total software transparency over a cable as well as a backplane. For CompactPCI and CompactPCI Express systems, this transparency enables system configurations where the CPU element is external from the CompactPCI Express system. For example, it's possible to create a development system for CompactPCI Express that is based on an external PC attached via PCI Express over cable (Figure 5).



Figure 5

Deciding whether to have an attached PC versus an internal CPU involves several trade-offs. Attached PCs are often more robust, offering the latest CPU speeds, memory, and peripherals. Embedded PCs have the advantage of eliminating the second chassis, and providing a more consistent level of ruggedness. Often, designers will choose the convenience of an attached PC for development, and then transition to an embedded CPU board for production.

Tree and network topologies

CompactPCI Express supports both tree and network topologies. A tree architecture includes one CPU element connected to a number of I/O elements. This is the most cost-effective

topology and is suitable for many applications where a single CPU is needed.

CompactPCI Express also supports multi-CPU applications. These applications take advantage of the ASI PCI Express.

ASI within CompactPCI Express

ASI is an extension to PCI Express that allows CPU-to-CPU communication and dynamic I/O mapping to work on top of the basic PCI Express functionality. For multi-CPU systems, this unifies the CPU-to-CPU communications bus and the I/O bus structure. This unification significantly improves performance, system cost, and fault tolerance.

Systems based on ASI within CompactPCI Express utilize the same CPU and I/O boards as tree architecture systems. A different switch board is needed, however, to provide the PCI Express-to-ASI bridges for the CPU boards and the ASI-based switch functionality.

PICMG 2.16 solution for multiprocessing

Both CompactPCI and CompactPCI Express have built-in flexibility via their P3, P4, and P5 connectors that are available for user-defined rear I/O and/or secondary buses or interconnects. Several uses for these connectors have become standardized. One of the most popular is PICMG 2.16, which defines how 1 GbE

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can be routed through the P3 connectors to a special 2.16 switch slot. This mechanism allows multiple CPU boards to intercommunicate via the Ethernet in a network topology. *Split backplane* solutions have extended this concept to allow multiple CPU domains (isolated CPU and I/O slots) to be integrated within a single system, with the CPU boards connected by Ethernet routed via 2.16.

ASI as an upgrade path for 2.16 systems


ASI within CompactPCI Express provides a particularly attractive upgrade path to 2.16-based systems. The advantages of ASI include 10-50 times higher performance, lower costs, and dynamic I/O mapping.

ASI performance depends on the lane width of the underlying PCI Express buses. Typical systems will include two independent x4 PCI Express bus interfaces from each CPU board. Each of these interfaces operates at 10 Gbps. Higher performance is achievable by boards that utilize x8 or x16 interfaces. The move to Gen 2 timing, which is expected to become available in late 2007, will also increase performance.

Combining two buses (PCI and Ethernet in 2.16) into one PCI Express bus that performs both functions lowers costs. CPU boards don't need to drive the extra Ethernet ports into the backplane, and an expensive 2.16 switch board is eliminated. The CompactPCI Express with ASI solution does require its own switch board, but this function provides both the I/O board fan-out and multiprocessor switching functions.

Dynamic I/O mapping allows any PCI Express I/O function to be mapped to any CPU board, with the mapping changeable on the fly. This capability provides greater hardware configuration flexibility and enhanced fault tolerance. If a CPU board fails, a different CPU board can be remapped to take over control of the I/O boards. This type of capability doesn't exist within 2.16 systems. In those systems, if the controlling CPU board goes down, all the I/O associated with that CPU also goes down.

Conclusion

CompactPCI Express provides the advanced features of PCI Express in the CompactPCI form factor. In doing so, it extends the useable lifespan of the architecture for at least another decade. 



Steve Cooper is president and CEO of One Stop Systems, and has more than 18 years of sales, marketing, and general management experience in the standard bus-board marketplace. He began his career with Intel, where he became a technical spokesman for the concept of board-level open bus standards and the Multibus and Multibus II architectures. Steve then joined RadiSys, a company specializing in embedded PC-compatible computers. He also served as vice president of sales and marketing, and later president and CEO, at I-Bus. Prior to founding One Stop Systems, Steve was president and COO for SBS Technologies. He holds a BSEE degree from the University of California, Santa Barbara.

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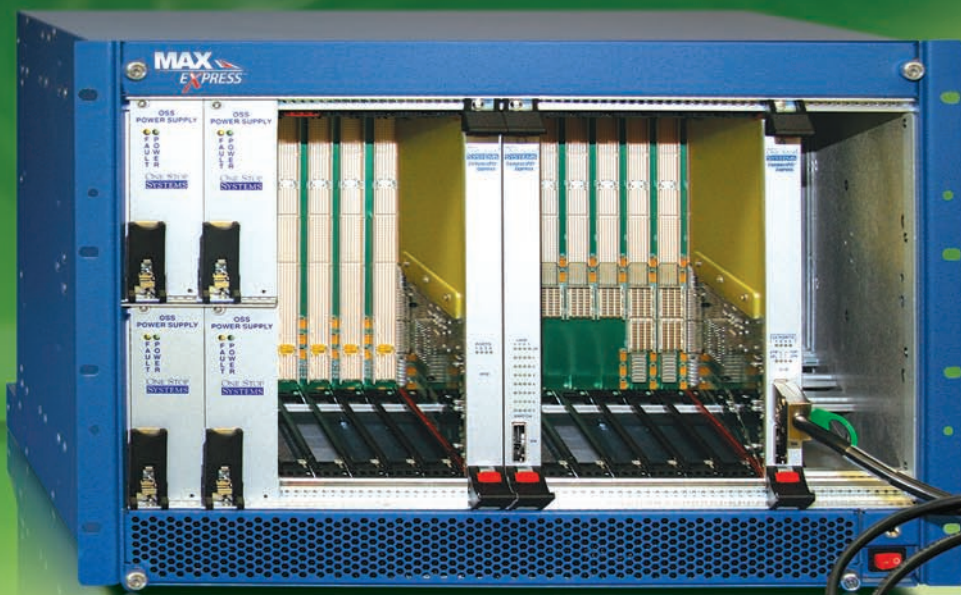
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| MaxExpress Expansion System | A PCI Express or PCI-X host interface board with 20-40 Gbps bandwidth cable link • Available as a copper expansion cable up to 6 meters in length or a fiber optic cable many kilometers in length • 3U or 4U expansion enclosure for PCI Express or PCI add-in boards |
| OSS-ELB-3U/6U | 3U or 6U Expansion Link Board for CompactPCI Express with two x4 PCI Express cable links and autoconfigurable CompactPCI Express backplane connectors • PICMG EXP.0 system slot compliant • x4 PCI Express PCI-SIG-compliant cable uplink • Configurable two x8 or four x4 PCI Express links to the backplane • 10 Gbps cable bandwidth |
| OSS-ETH-MAX-3U | Max Express 3U CompactPCIe dual Gigabit Ethernet controller board • 3U EXP.0 Type 2 form factor • Intel 82571EB Dual Gigabit Ethernet controller • Yellow/Green – Green LEDs on each RJ-45 jack • CAT6 copper interface • 48 kB on-chip packet buffer • Hot-swap compatible • RoHS compliant |
| OSS-HEB-3U/6U | 3U x4 PCI Express cable Host Expansion Bridge board to 3U, 64-bit/66 MHz CompactPCI/PXI with PCI Express cable connector • Operates in a CompactPCI system or peripheral slot • PCIe x4 cable connector • 3U or 6U form factor |
| OSS-HYB-3U/6U | Hybrid bridge board that bridges between CompactPCI Express slots and CompactPCI slots in a single backplane when plugged into a hybrid bridge slot; available in 3U or 6U connectors • Bridges between CompactPCI Express slots and CompactPCI slots • Requires hybrid slot on backplane |

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SHB Express edge-card computing systems merge past, present, and future technologies

By Brad Trent

Some system architectures require option cards in form factors that are not adaptable to the commercial marketplace. The main advantage of designing an SHB Express (PICMG 1.3) system is the ability to take advantage of the huge population of inexpensive, commercially available, off-the-shelf PCI, PCI-X, and now PCI Express option cards. In other words, we let the laws of supply and demand work for us in a PICMG 1.3 system architecture. New PCI Express System Host Boards (SHBs) and PICMG 1.3 backplanes enable the system designer to support multiple option cards with different bus architectures. This allows the designer to take advantage of the plethora of inexpensive PCI/PCI-X option cards as well as the new PCI Express cards. Read on to see precisely how the latest SHB Express developments, including the models in the SHB Express Product Guide that follows, make this all happen.

System host boards

SHB Express system host cards are designed to the PICMG 1.3 industry standard. The standard defines 20 PCI Express lanes or links between an SHB and a PICMG 1.3 backplane. A board designer configures the available PCI Express links in a wide variety of combinations based on the SHB's chipset and the slot support requirements of the backplanes.

PICMG 1.3 SHBs and backplanes fall into two broad categories: Graphics class and server class. A graphics-class SHB can have one x16 and either one x4 or four x1 PCI Express links to the backplane. A typical server-class SHB may have a combination of x8 and x4 links routed to the backplane. Graphics-class SHBs and backplanes should always be paired together. Likewise, server-class SHBs should always be used with server-class backplanes. Doing this allows you to take full advantage of all available option card slots on the PICMG 1.3 backplane. The PICMG 1.3 specification is written

to prevent any unforeseen board damage caused by mixing the two classes of backplanes and SHBs. If a server-class SHB is used with a graphics-class backplane or vice versa, the possibility exists that one or more of the backplane's option card slots might be nonfunctional. Mismatching the SHB and backplane could result in not having enough PCI Express links available to connect all of the option card slots to the system host board.

Multicore processors are finding many applications in SHB Express systems. Multicore processors are processors that have separate execution cores on a single processor die. The most common multicore processors available today have either two or four independent execution cores. These additional execution cores greatly improve overall system performance. These new processor designs are also far more thermally efficient than their predecessors. New PICMG 1.3 system host boards are now available with one and in some cases two dual-core processors. The benchmarks on some of these new SHBs with two thermally efficient, dual-core processors provide outstanding system performance. Figure 1 shows some typical benchmark test results that

compare single- and dual-core SHB performance.

SHB Express backplanes

Today's PICMG 1.3 backplanes support a wide variety of option card slot configurations and form factors. These backplane variations are available in both the server-class and graphics-class categories as well as 14-slot, 20-slot, and new shoebox form factors. When choosing any type of passive backplane ensure that the supported option card slots adhere to the applicable PCI, PCI-X, or PCI Express electrical interface specification. For example, many inexpensive passive backplanes routinely violate the capacitive loading limits of the PCI bus by allowing the system host board to directly drive more PCI slots than allowed by the electrical specification. This situation may result in erratic option card operations, particularly in environments with high ambient electrical noise or fluctuating electrical power.

As stated earlier, one of the unique attributes of SHB Express systems is the capability to support a wide variety of system architectures including older ISA cards. It's been years since a new ISA card has been designed, but a fair

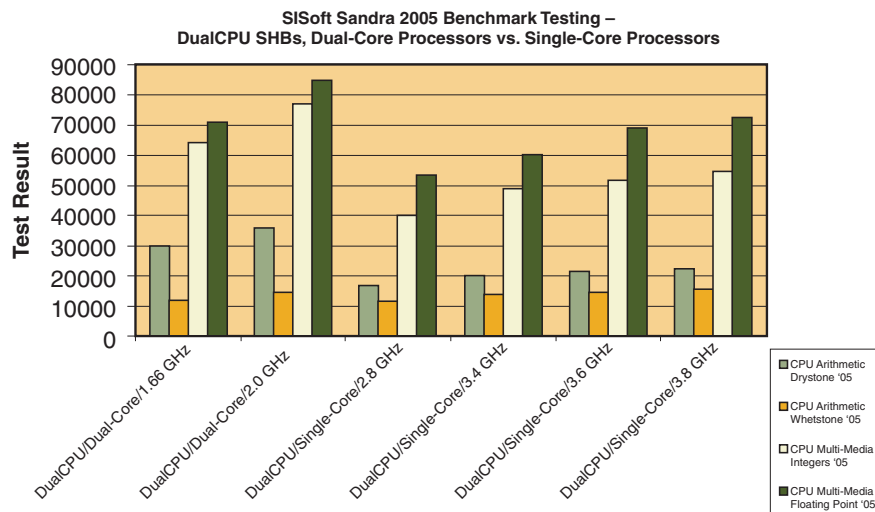
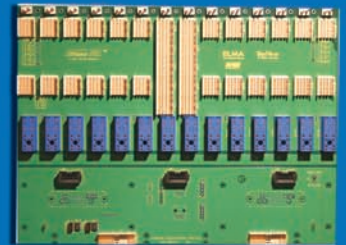
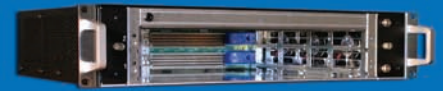


Figure 1



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Your application demands AdvancedTCA, and you demand convenience and flexibility. You can have it all, with Elma's line of A/C powered ATCA system platforms. These chassis are ideal for prototyping, demos, or any application that requires A/C power. Available in 2U and 5U heights, with a multitude of configurations, Elma has an ATCA system to meet your requirements. And nobody is better than Elma in customizing to your exact specifications. When you're ready to plug into success, give Elma a call.

ATCA Chassis

- A/C or D/C versions in 2U, 5U and custom heights
- A/C input option, up to 700W
- Pluggable to a conventional A/C wall outlet
- Pluggable shelf manager options
- D/C versions in 4U, 12U, 13U, 13U ETSI and custom heights

ATCA Backplanes

- 2, 4, 5, 14 & 16 slots
- Dual Star, Mesh or Replicated Mesh
- Compliant to PICMG 3.0 Rev 1.0
- Optimized via signal integrity studies

ATCA Capabilities

- Simulation
- 3D Solid Modeling
- NEBS Certification
- Manufacturing
- Customization
- Integration

ATCA Accessories

- Front Panels
- Handles
- Shelf Management

Enclosures &
Components

Backplanes

System
Platforms

Switches,
Knobs & LEDs

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number of special purpose ISA cards are still being produced. In many cases it is cost prohibitive to design out these older option cards. SHB Express offers a solution that supports older cards as well as new PCI Express cards. The option cards are installed in an SHB Express backplane and controlled by a state of the art PICMG 1.3 SHB. The net result is a system that offers high-speed SHB-to-backplane communications via PCI Express without having to discard the proven and cost-effective option cards of the past. This results in improved data throughput due to the higher bandwidth and increased speed offered by PCI Express while leading to a significant reduction in overall development expense and long-term system support costs. The key to making this all happen is PCI Express-to-PCI-X and PCI-to-ISA bridge technology. Bridge technology on a PICMG 1.3 backplane is cost effective, robust, and reliable with minimal data latency delays. This key technology allows SHB Express systems to cover all your past, present, and future system requirements with PCI Express SHBs and passive backplanes. The block diagram in Figure 2 illustrates how PICMG 1.3 systems can support ISA, PCI/PCI-X, and PCI Express option cards

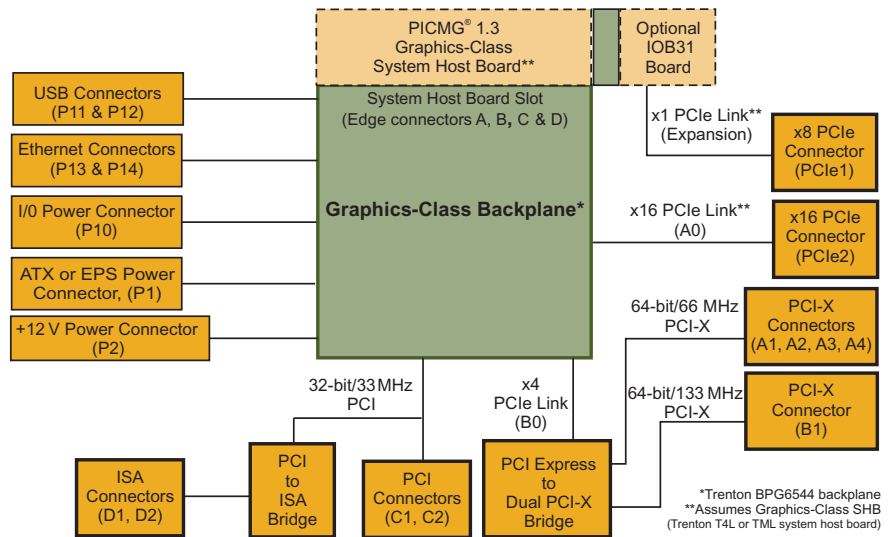


Figure 2

The PICMG 1.3 specification provides enough power pins on edge connector C of the SHB to eliminate the need for auxiliary power connectors. This new feature improves Mean Time to Repair (MTTR) by having the +12 V AUX connector on a backplane instead of the SHB. Figure 3 illustrates the variety of PICMG 1.3 backplanes currently available.

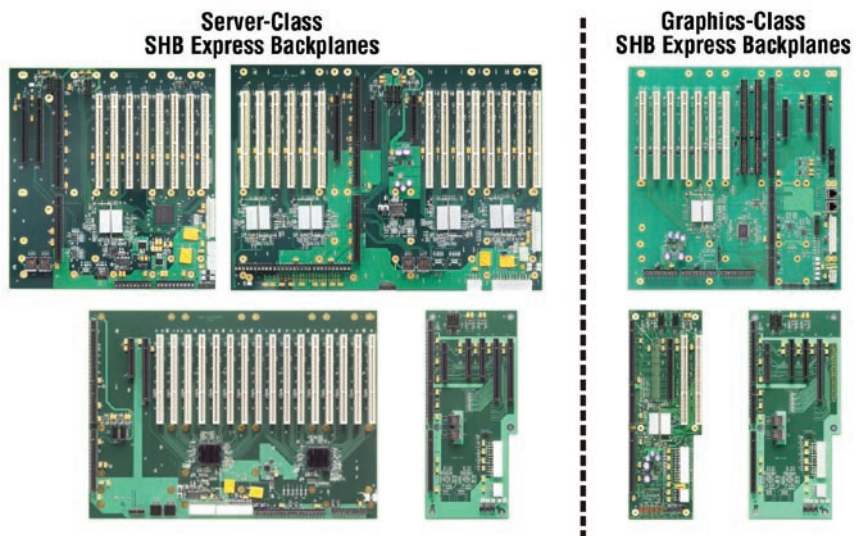


Figure 3

SHB Express chassis

If there is such a thing as a typical SHB Express/PICMG 1.3 chassis it's one that fits in a 19-inch rack (Figure 4). The chassis height is usually 4U, but this is not always the case. The chassis height may be greater than 4U depending on the chassis cooling system type, removable media, and hard drive placements. The SHB could have a low-profile passive cooling solution and a butterfly backplane that allows the SHB to be mounted horizontally rather than vertically. The result is an overall chassis height of 2U or less. New shoebox PICMG 1.3 backplanes accommodate smaller, wall-mount chassis designs. Here is a partial

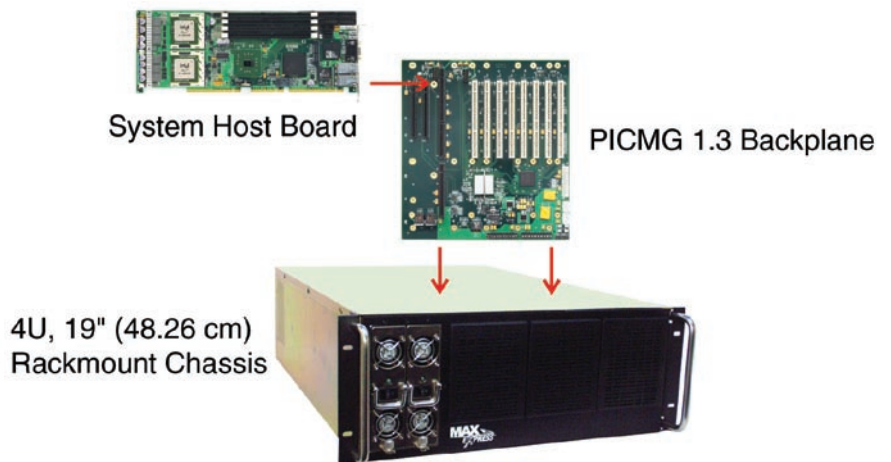


Figure 4

list of key chassis attributes to be considered regardless of the chassis type or vendor:

- Chassis certifications (NEBS, SAIC, Belcore, CE, and Medical Systems [UL544])
- Military requirements/ Certifications (airborne, shipboard, MIL-SPECs)
- Ruggedized requirements and environmental extremes (such as temperature, shock, vibration)
- Fault tolerant
- Airflow/cooling and power delivery requirements

Conclusion

The SHB Express specification was ratified in Q2 of 2005 with an explosion of PICMG 1.3 SHBs and backplanes available from a number of vendors. These boards are being deployed in a wide variety of chassis and in numerous applications to solve a number of bandwidth-related performance issues for system designers. The really nice thing about SHB Express is the ability to support the latest PCI Express board technology, legacy PCI, and even ISA boards. System designers can take advantage of the flexibility built into the specification and supported by a variety of vendors to gain an elegant method for incorporating both leading-edge and legacy technologies in the same design.

The flexibility inherent in the SHB Express specification allows cost-effective migration to PCI Express technology. In other words, unlike other new specifications, SHB Express does not require that the systems designer throw out all previous designs and start over. When developing the SHB Express specification, the PICMG 1.3 Technical Subcommittee took technology advancements such as PCI Express Gen 1 and Gen 2 and advanced switching into consideration.

As a result, SHB Express supports both current and future iterations of PCI Express technology, including advanced switching. SHB Express products support past, present, and future slot board technologies while enabling a seamless and cost-effective transition to PCI Express and advanced switching. 🌐



Brad Trent is director of engineering for Trenton Technology and served as the technical editor on the PICMG 1.3 Technical Subcommittee.

Brad has held various engineering positions in the embedded computing, industrial automation, computer workstation, and process system control industries. Brad holds a BS in Nuclear

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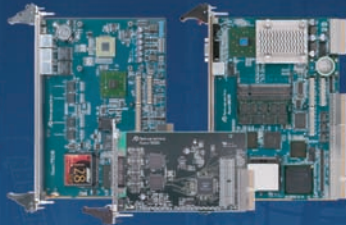
E-mail: btrent@trentontechnology.com

Website: www.trentontechnology.com




CompactPCI Series

- Processor boards (Intel Pentium & PowerPC)
- Memory boards
- EtherNet 10/100 & Gbit boards
- Comm boards: EtherNet, StarFabric
- Fieldbus: CAN/DeviceNet
- I/O boards, DIO & AIO
- Rear Transition Modules
- RTOS Support (Windows, VxWorks)



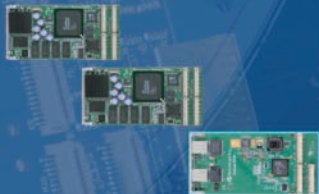
VME Board Series

- CPU boards (Intel x86 & PowerPC architectures)
- Memory boards
- EtherNet 10/100
- Digital & Analog I/O boards
- A/D and D/A conversion boards
- Communication boards (EtherNet, GPIB, CAN/DeviceNet, ARCNET)
- RTOS Support (Windows, VxWorks)



PMC Board Series

- PowerPC G3/G4 CPU boards
- EtherNet: 10/100 & Gbit boards
- PMC-StarFabric Bridge
- D/A & A/D conversion boards
- Memory boards
- VGA & JPEG compression boards
- RS232 & SCSI boards
- PMC carrier boards
- RTOS Support (Windows, VxWorks)



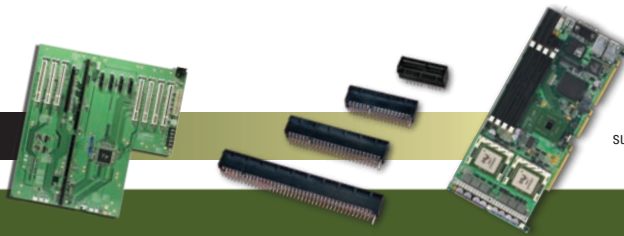
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PRODUCT GUIDE

SHB Express



(From left to right)
The Nexcom 14 Slot PICMG/ISA/PCI backplane
Vertical card-edge connector from FCI supports SHB Express backplane designs
The MAX Express Dual Xeon SHB from One Stop Systems

| Company/ Model number | Description |
|--|---|
| Chassis Plans www.chassis-plans.co | |
| BPX 3/14 | One SHB Express (PICMG 1.3) System Host Board slot • Two x8 PCI Express slots (mechanical) • Two 64-bit/133 MHz PCI-X slots • Twelve 64-bit/100 MHz PCI-X slots • Four USB 2.0 and two SATA/150 backplane I/O connections • Option to add two additional, mirrored SATA/150 ports for RAID applications • Two 10/100/1000BASE-T backplane Ethernet ports • ATX, EPS, and extended-current power connection options • Supports Chassis Plans' and PICMG 1.3 20-slot hole patterns • Seamless support for PCI Express, PCI-X, and universal PCI option cards |
| FCI www.fciconnect.com | |
| Vertical PCIe card-edge connectors | Support manufacturers' backplane designs based on the System Host Board (SHB) Express specification (PICMG 1.3) • Connectors at the interface between the SHB and backplane are defined as x8 and x16 PCI Express connectors • The backplane slots to interface with PCI Express peripherals can be supported with x1, x4, x8, or x16 PCI Express connector links • Complete range of PCI Express connector sizes with through-hole solder-to-board or press-fit termination options • Press-fit termination offers processing advantages when backplane thicknesses exceed 2.36 mm (0.093") • Solder and press-fit connectors are available in standard x1, x4, x8, or x16 link widths • Each serial PCI Express lane is comprised of differential transmit and receive signal pairs that support 2.5 Gbps data rate in each direction • All connectors fully support SHB Express or PCI Express signal and power requirements, as well as the auxiliary signals at the interface between the system board and add-in card |
| Global American www.globalamerican.com | |
| 3301520 | Full-size PICMG 1.3 supporting PCI Express x16 bus • Intel LGA775 Pentium D/Pentium 4 CPU, FSB up to 1,066 MHz • Intel 945G and ICH7R chipsets • Two 240-pin DIMM sockets supporting up to 2.0 GB 533/677 MHz DDR2 SDRAM • Intel GMA950 PCI Express x16 Integrated Graphics supporting CRT/LCD • DUAL RC82573L PCI Express Gigabit 100/1000 LAN • RoHS compliant • Four SATA ports • Eight USB ports, version 2.0 • AC'97 Audio |
| iBase Technology www.ibase-i.com.tw | |
| IB868 | Socket 479 Intel 915GM PICMG 1.3 SHB Express full-size CPU card with 10/100 LAN • Supports Pentium M/Celeron M processors • Two DDR2 SDRAM DIMM, max. 2 GB • Onboard 10/100BASE-T, optional Gigabit Ethernet • Intel 915 Express VGA for CRT/LVDS • Six USB 2.0, two COM, watchdog timer, digital I/O • Optional backplane with three PCI Express (x1), one PCI Express (x16), four PCI slots |
| IEI Technology USA www.usa.ieiworld.com | |
| PCIE 9450 | PICMG 1.3 and RoHS compliance • Intel LGA775/ Pentium D processor CPU support up to FSB 1066 MHz • Dual channel DDRII-400/533/667 MHz support up to 4G • High-performance PCI Express Gigabit Ethernet controller • Four SATAII • Seven USB 2.0 (6 by pin header) |
| NEXCOM International www.nexcom.com | |
| NBP-14570-BX | 14-slot PICMG/ISA/PCI backplane • Slots in system: Seven PCI, one PICMG 1.3, 4 PCI Express x 1, One PCI Express x 16 slots, Seven PCI/1 x PICMG/Four PCI Express x1 lane/One PCI Express x16 lane • Size: 317 mm x 328 mm • Supports ATX power supply • RoHS compliant |
| Peak 870VL2 | Fully RoHS compliant single board computer • Full-size PICMG 1.3 product supporting socket LGA775 processors up to Pentium 4 at speeds up to 3.8 GHz • The product uses hyperthreading technology and incorporates the Intel 945G and ICH7 chipsets, which support Intel's new dual core processors • Based on advanced PCI Express architecture • Suitable solution for a large number of high-end industrial computing applications • With one PCI Express x16 and four PCI Express x1, the Peak 870VL2 increases data transfer rates, enabling it to support high-end graphics peripherals via a graphics card • With the new PICMG 1.3 standard, backwards compatibility for PCI and PCI-X is also possible • I/O ports, include eight USB 2.0 ports, four Serial ATA ports supporting SATA RAID 0.1 function, and two PCI Express x1 interfaces for Gigabit Ethernet • IPMB to monitor CPU running temperature, voltage, and fan rotational speed |
| One Stop Systems www.onestopsystems.com | |
| MAX Express Dual Xeon System Host Board (SHB) | Dual Intel Xeon processors with the Intel E7520 chipset • Provides PCI Express interfaces to the backplane • Compatible with the SHB Express (PICMG 1.3) specification • Operates in x1, x4, and x8 modes (PCI Express), 32-bit/33 MHz mode (PCI) and 64-bit/66 MHz mode (PCI-X) • Dual Gigabit Ethernet |
| OSS-EBP-2001 | Eighteen PCI Express x4 slots with x8 connectors • One PCI Express x8 slot • One SHB slot supports expansion adapter board • Two ATX power connectors, two SATA connectors, two Ethernet connectors, and four protected USB ports |
| OSS-EBP-2002 | One SHB system slot • One x16, one x8, four PCI-X/PCI (64/66), and four PCI (64/33) slots • Power connections: ATX, EPS, screw terminals • USB 2.0 (four ports) and 10/100/1000BASE-T Ethernet (one port) |
| OSS-ELB-SHB | PCI Express x4 Expansion Link Board that fits into the system slot of an SHB Express (PICMG 1.3) compliant backplane in a downstream expansion chassis • Two x4 PCI Express (10 Gbps) connectors on slot cover • Upstream/downstream lane active LEDs on slot cover • Two x8 and one x4 PCI Express links through the PICMG 1.3 card edge connector • Power acceptable LEDs on board • Optional power connector for embedded applications without a backplane |
| Pentium D/Pentium 4 System Host Board | A graphics-class, PICMG 1.3 SHB • Pentium D dual core processor • Provides one x16 PCI Express link and one x4 PCI Express link • Direct connect video option via the chipset's Intel Graphics Media Accelerator 950 • Supports dual channel DDR2-667 memory, 4 GB maximum • Dual Gigabit Ethernet ports plus one 10/100BASE-T backplane interface • Integrated RAID 0, 1, 5, and 10 implementation support via four SATA/300 ports • Part number: OSS-SHB-PD-XX |
| Trenton Technology www.trentontechnology.com | |
| Bpx3/8 – SHB Express Backplane | Backplane that supports all full-length SHB Express-compatible system host boards • One x16 and one x8 PCI Express slot • A PCI Express-to-PCI/PCI-X bridge chip supports four 64-bit/66 MHz PCI-X or PCI option card slots and a PCI-to-PCI bridge provides support for four additional 64-bit/33 MHz PCI cards • The BPX3/8 supports the Trenton 14-slot backplane and the SHB Express (PICMG 1.3) 13-slot backplane mounting hole patterns • Input power options for the backplane include ATX, EPS, and screw terminals for extended-current applications • This is the first in a series of planned SHB Express backplanes from Trenton • Trenton also offers custom backplane engineering and manufacturing services |

| | |
|--|--|
| BPX6571 | A server-class backplane that provides electrical connections for one x8 and one x4 PCI Express card and sixteen 64-bit/66 MHz PCI-X option cards • Enables a System Host Board (SHB) Express, such as the NLT or NLI, to support PCI Express, PCI-X, and PCI option cards |
| NLT SHB Express System Host Board/NLI SHB Express System Host Board | Dual Intel Xeon processors with an 800 MHz system bus, including Intel EM64T to offer support for both 32-bit and 64-bit applications • Intel E7520 chipset • Dual channel DDR2-400 memory capable of supporting 8 GB of memory with a maximum memory bandwidth of 6.4 GBps • Edge connectors on the NLT provide two x8 PCI Express links, one x4 PCI Express link, and five PCI Express reference clocks on edge connectors A and B • PCI Express links support communication to x1, x4, x8, and x16 PCI Express boards as well as PCI/PCI-X option cards via a PCI Express-to-PCI/PCI-X bridge chip on an SHB Express-compatible backplane • Dual SATA/150 interfaces • Quad USB 2.0 connections • Dual 10/100/1000BASE-T Ethernet ports • Onboard video • Optional I/O expansion board for legacy I/O support |
| SLT SHB/SLI SHB | A server-class PICMG 1.3 SHB that features two, dual core Intel Xeon processors and the Intel E7520 chipset • The two dual core Intel Xeon LV Processor 2.0 GHz CPUs operate at about half the power as previous CPUs enabling the SLT's low-profile passive heat sink cooling solution • The SLI is a single processor version of Trenton's SLT • This server-class PICMG 1.3 SHB has a single dual core Intel Xeon LV processor 2.0 GHz providing two processor execution cores per SLI with a low-profile passive heat sink |
| T4L System Host Board | A graphics-class SHB with direct support for x16, x4, and x1 PCI Express links to a PICMG 1.3 backplane • Pentium 4 Processor 651 with the Intel 945G chipset • Dual core processor options supported (Intel Pentium D) • Supports x16 video and graphics cards or ADD2 cards • Direct connect video option via the chipset's Intel Graphics Media Accelerator 950 • Compatible with the SHB Express (PICMG 1.3) specification • Supports dual channel DDR2-667 memory, 4 GB maximum • Dual Gigabit Ethernet ports plus one 10/100BASE-T backplane interface • Integrated RAID 0, 1, 5, and 10 implementation support via four SATA/300 ports |
| TML | Graphics-class SHB has a feature set similar to the T4L system host board • The TML uses the Intel 945G chipset with the Intel ICH7R I/O controller and offers Intel Core Duo, Intel Core Solo, and Intel Celeron M processor options |

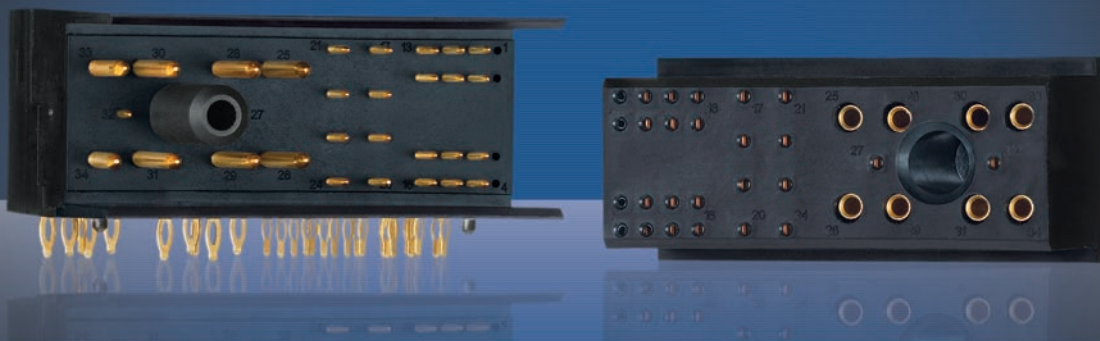
WIN Enterprises

www.win-ent.com

| | |
|-----------------|--|
| MB-06048 | A PICMG 1.3-style Single Board Computer (SBC) that can be powered by one or two single or dual core AMD Opteron processors • Small board size: 13.330" x 4.976" (33.86 cm x 12.64 cm) • Single, dual core, or two dual core CPUs requiring low to high power (30/55/95 W) • Onboard video integration: ATI 64 MB M9 graphics • Three 10/100/1000 Gigabit Ethernet LAN ports • Four USB ports • NVIDIA nForce Professional 2200 chipset • 4X SATA with RAID 16-lane PCI Express slot, PCI-X 64-bit/133 MHz • 2 memory slots with up to 8 GB • Standard IDE interface • Supports Linux Debian 64 and Windows XP 32- and 64-bit operating systems |
| MB-06049 | PICMG 1.3 form-factor design • AMD Opteron processor • Enables both 32- and 64-bit computing • Passive backplane systems design with plug-in high performance • Suitable for demanding environments, including industrial automation, military, medical, and telecom • NVIDIA nForce Professional 2200 chipset designed for AMD Opteron • A HyperTransport interconnect system provides leading-edge I/O by enabling the additional integration of one or two dual core processors on stackable boards • 20-lane PCI Express slot • Supports low to high power (30/55/95 W) • Single or dual core CPU • Leading-edge, stackable HyperTransport interconnect system enables quad core designs • Two memory slots with up to 8 GB and two additional slots with an optional CPU adapter card yield total of 16 GB memory • Standard IDE interface • Four SATA with RAID, 1 Gigabit Ethernet, and four USB 2.0 • Supports Linux Debian 64 and Windows XP 32- and 64-bit operating systems |

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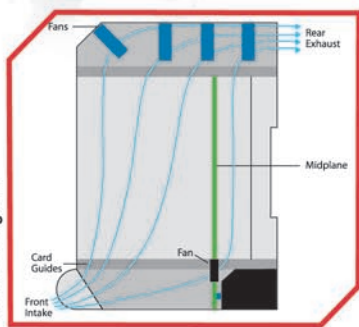


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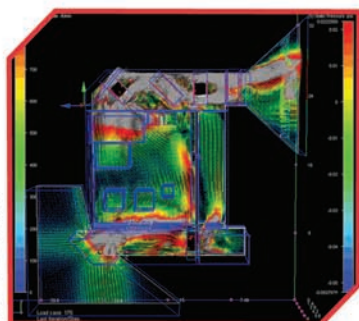
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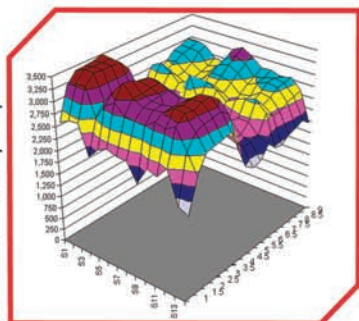
Airflow Diagram



CFD Simulation



Chassis Slot Velocity Map



HYBRID SERIAL PARALLEL COOLING DELIVERS 99.999% HIGH AVAILABILITY

The Schroff Hybrid Serial-Parallel (HSP) cooling scheme uses axial fans in an innovative way to optimize shelf availability while minimizing downtime. Traditional fan trays contain rectangular combinations of serial and parallel fans with the goal of providing adequate bulk airflow to cool electronic components – at the design point. Fan failure conditions can compromise that ability, particularly in individual slots or regions.

Serial fan configurations, which boost air pressure, are subject to sharp pressure losses in the case of a fan failure. Such failures can cause power supplies and chips with high-fin-density heat sinks to overheat. Parallel fan arrangements push large volumes of air across multiple open surfaces – until a fan fails and recirculation occurs, substantially reducing the cooling to multiple slots.

Schroff's HSP design staggers the fans and arranges them at right-angles to the boards. The staggered fan distribution draws air from slots below and adjacent to each fan, but without the risk that a dedicated sealed channel presents. When a fan fails, the next fan upstream or downstream will continue to draw air with a marginally reduced cooling capacity until the fan is replaced. The end result is a dependable shelf with uniform slot-by-slot and front-to-rear airflow.

FEATURES

- Patented Hybrid Serial-Parallel (HSP) fan arrangement
- Multiple arrays of offset fans provide fault-tolerant cooling
- Inexpensive axial fans deliver high-availability (99.999%) airflow
- Low-profile fan trays distribute air uniformly across the shelf, even with plug-in modules present
- High efficiency configuration draws less fan input power.

Innovative Engineering



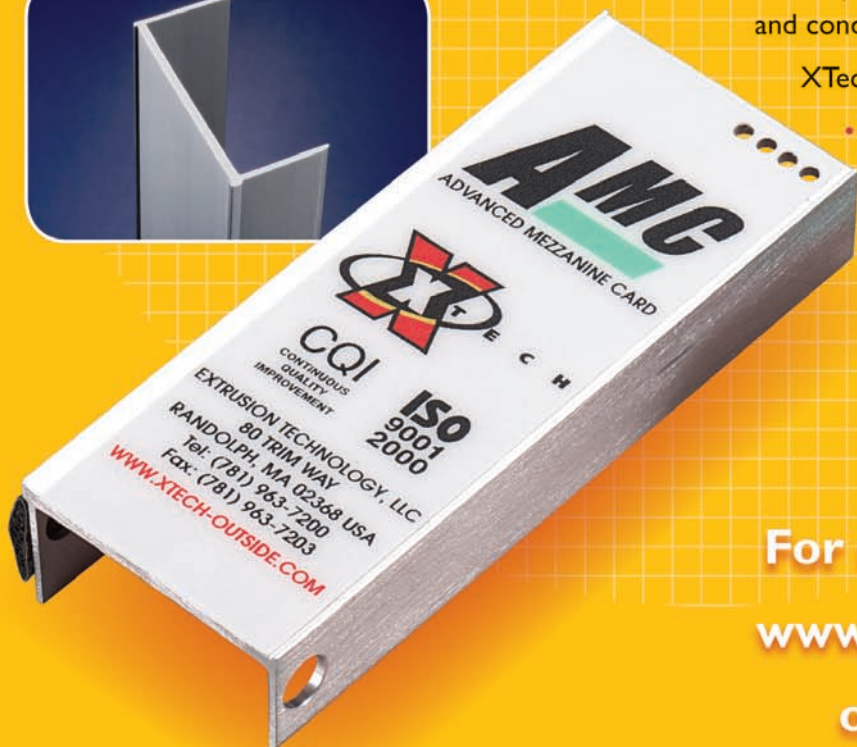
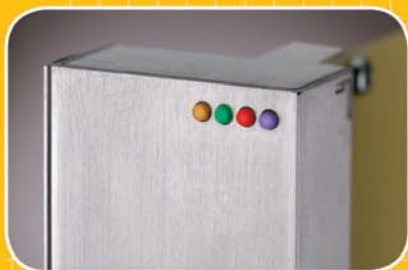
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AdvancedMC solutions



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XTech's rugged, robust aluminum AMC design includes an integrated, self-retaining light pipe and latch, an improved, 3-position latch system, top block with LED housing with quad light pipe, and printed label.

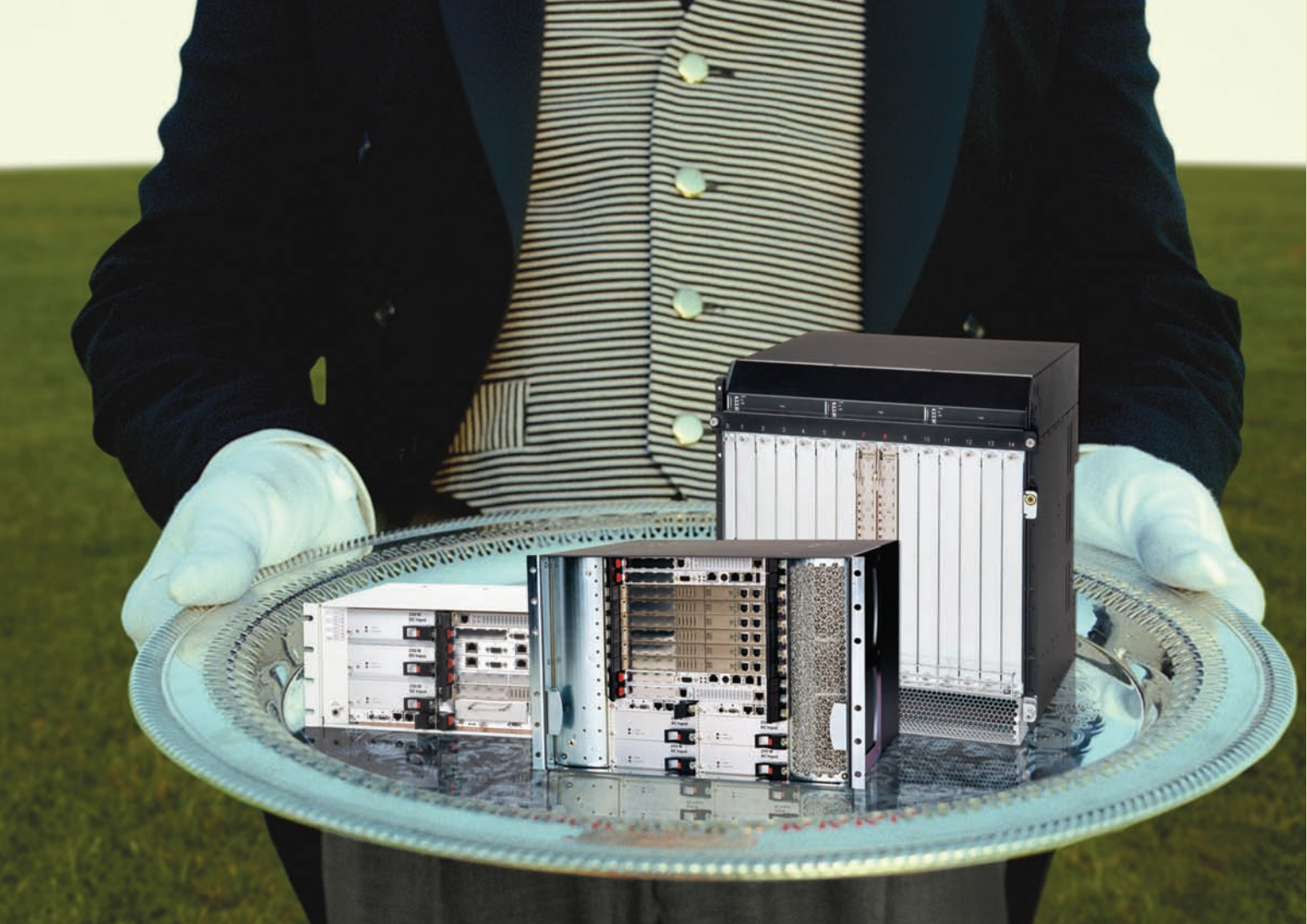


Like all XTech systems, we configure AMC modules to fit your specific requirements for circuit board mechanical assemblies—for prototype, pre-production or full production applications. They are available in a variety of sizes, and also in sheet metal and conductive plastic.

XTech AMC module features also include:

- Recessed EMI shielding to prevent gasket rollout
- Chamfered edge on shielding leg to ease insertion and prevent gasket snag
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