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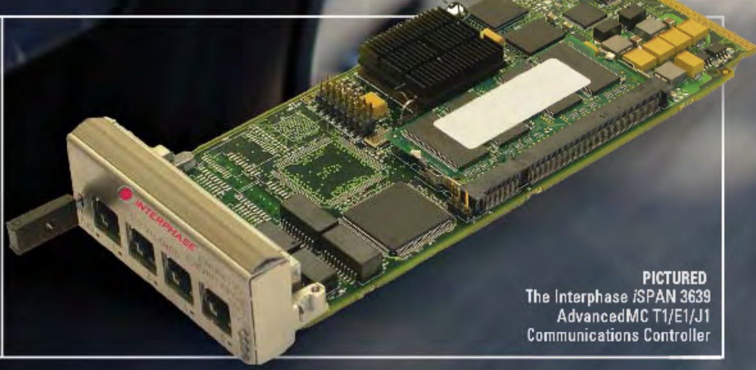

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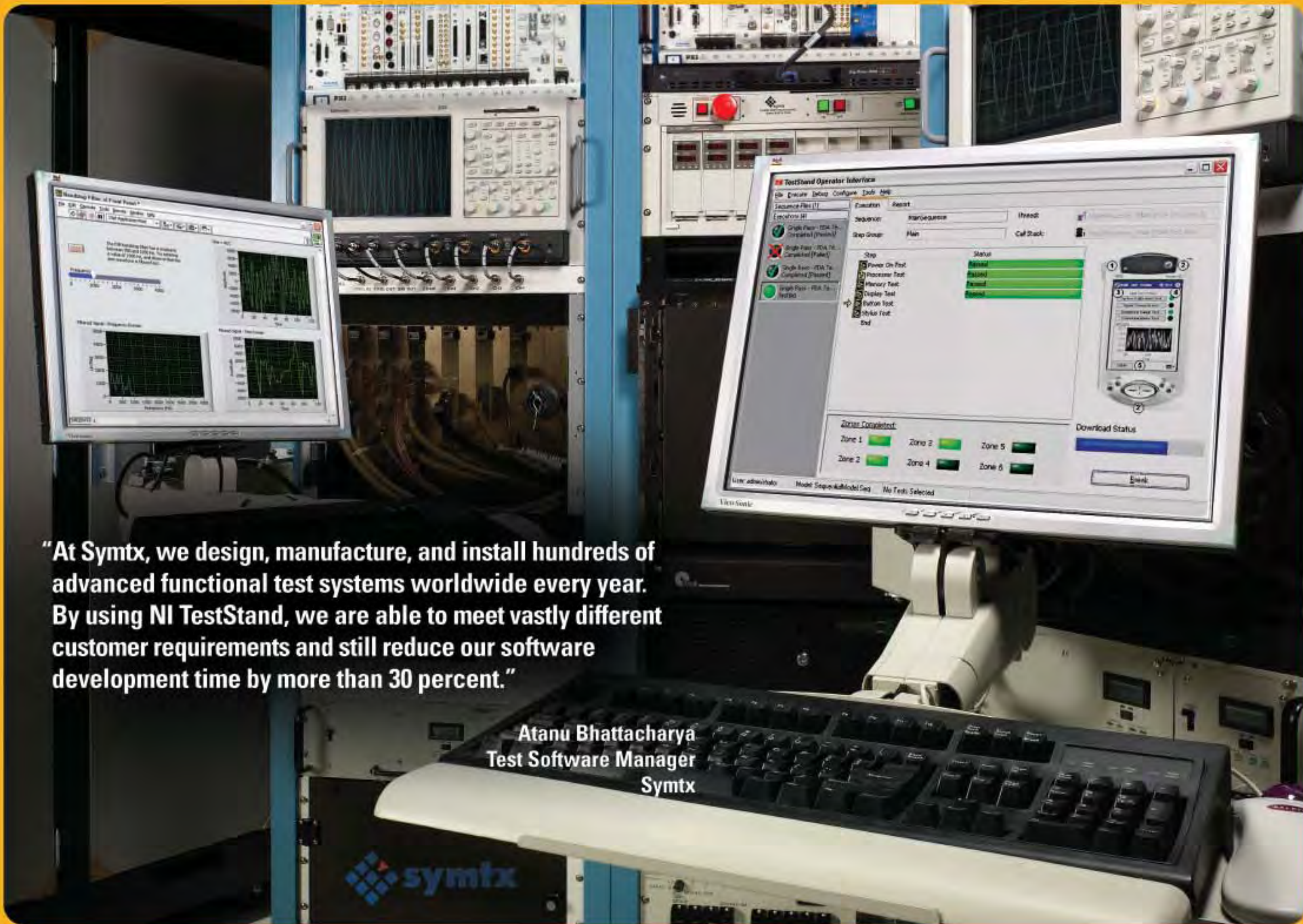

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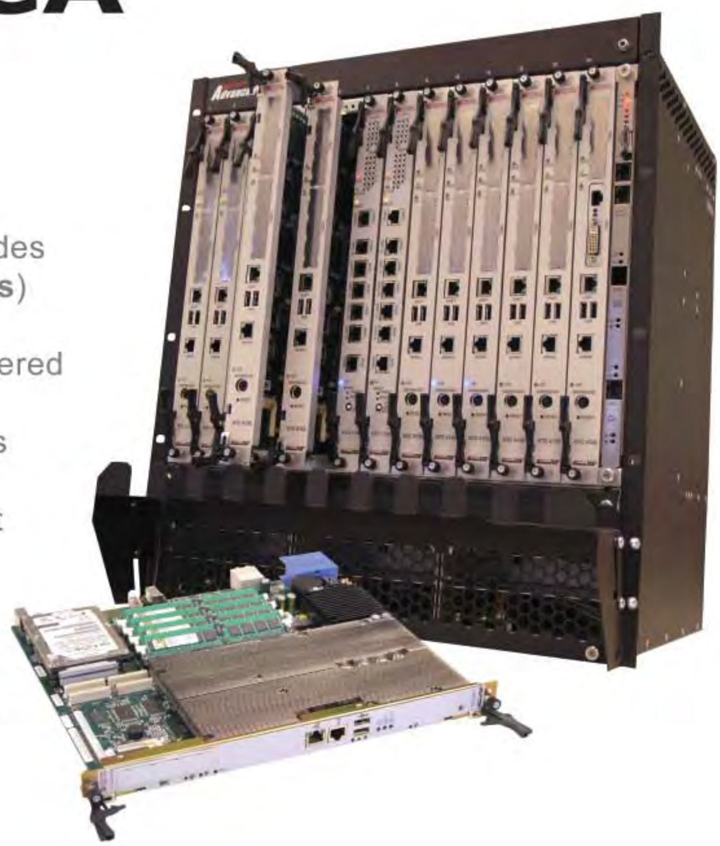

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Editor's Foreword

By Joe Pavlat

Is lead dead?

In an effort to reduce contamination of the environment associated with the disposal of electronic and electrical equipment containing harmful heavy metals and other contaminants and carcinogens, the European Union passed, in February of 2003, the Reduction of Hazardous Substances Directive. Commonly known as RoHS, this Directive requires mandatory compliance in products produced in, or shipped to, the EU beginning in July of 2006. Other countries, including Japan and China, are moving aggressively to adopt the Directive, and similar laws have passed in a number of US states, including California. It will apply to a wide range of electronic and electrical equipment, including:

- Large and small household appliances
- IT, telecommunications equipment, computers, embedded computers, and storage arrays
- Consumer electronics
- Lighting equipment
- Electrical and electronic tools
- Automatic dispensing equipment

Known for mandating lead-free solders, RoHS covers five major categories:

- Lead – found in solders, terminations coatings on components and PCBs, paints, and as a stabilizer in PVC
- Cadmium – used in electroplated coatings, electrical contacts, relays, switches, and some types of solders, pigments, and substrates
- Mercury – used in lamps, sensors, switches, and relays
- Hexavalent chromium – found in corrosion-resistant coatings and passivation coatings on metals
- Polybrominated Biphenyls (PBB) and Polybrominated Duphenyl Ethers (PBDE), which are used as flame retardants in some plastics

To date our indusry's primary concern has been the move towards lead-free solders. These behave, before and after soldering, in somewhat different ways than the tin-lead solders used for the last hundred years. Pure tin is seen to be a cost-effective soldering material. Among several concerns with pure tin is tin's higher melting temperature. With tin's soldering temperature 30-40 degrees Celsius higher than previous tin-lead alloys, a variety of problems can crop up, including:

- Damage to heat sensitive components, including integrated circuits, capacitors, and optoelectronics
- PCB warping that could result in damaged components, misalignments, and cracks
- Delamination of multilayer PCBs
- Thermal fatigue of solder joints
- Damage to plated through holes: Narrow holes in thicker laminates seem to present the worst case. (This is an issue as sophisticated, multilayer high-speed backplane technologies become mainstream.)
- "Popcorn" failures: Rapidly applying heat to molded components causes moisture to gather and when it exceeds 100 °C, the resultant gas expansion can break the component.
- Reduced solder wetting: Reduced as soldering temperatures increase, it can result in poor joints.
- A requirement for cleaner surfaces prior to soldering

Tin whiskers and dendrites

Pure tin can produce long, thin "whiskers," which can grow to 10 mm in length, come loose, and short out circuits. The causes of these are not well understood. The US Naval Air Warfare Center has documented what they believe to be at least six satellite failures since 1985 due to whiskers. Although this problem has been with us for a while, a recent article in *Aviation Week & Space Technology,* notes that pure tin whiskers grow at a rate of up to 0.09 mm per year, which is about an order of magnitude faster than tin-lead mixtures. This may have serious implications for equipment lifetimes. Dendrites are fern-like growths that develop along a surface rather than outward from it, like tin whiskers. These dendrites, a form of metal migration, can cause shorts and, as with tin whiskers, appear to be a bigger problem with lead-free solders.

There are some exemptions to the RoHS rules, including the somewhat surprising one of lead in batteries. Many industries have applied for a wide range of exemptions, with some granted, especially in the lighting and lamp industries. For lead, most exemptions have come in the form of an extension of the deadline, and the fate of many others is up in the air. RoHS is of great concern to military electronics vendors and customers, and worry particularly that while some exemptions have been granted, the contract manufacturers building so much equipment for a wide range in industries, including the military, won't maintain separate tin-lead and pure tin manufacturing lines. Also, some countries, notably China, are refusing any deadline extensions. No reprieves appear to be available as US manufacturers, especially in the telecom industries, seek to increase their exports to these countries.

Alternative materials are emerging in order to meet RoHS, but many have issues of their own. Silver/tin oxide can be used in electrical contacts, replacing silver/cadmium oxide. It works fine at low voltages but tends to wear out faster at higher voltages. Gold can replace mercury in switches, but only mercury delivers a "bounce-free" contact, and its operational life, measured by number of operations, is significantly longer. Numerous alternatives to chromate passivation exist, but most resist corrosion less effectively.

So, is the sky falling? Key industries, especially the military, have serious and legitimate concerns, especially in the military. Painful and unexpected surprises will occur over the next decade, but I am not joining the Chicken Little Chorus just yet. I have abundant faith in the continuing ingenuity, resourcefulness, and talent of the members of our industry. Collectively we've overcome other mandates in the past, although admittedly most of these have came from customers and not governments. I wonder which is worse.

Joe Pavlat
Editorial Director

3U CompactPCI Board based on Intel® Pentium® M Processor with 855GME Chipset

TThe cPCI-3840 is a 3U CompactPCI 1.6GHz Pentium® M processor board. Combined with embedded chipsets 855GME and 6300ESB, the cPCI-3840 offers up to 2GB DDR 333 memory with XVGA and flat panel graphics, dual Gigabit Ethernet ports and several I/O features. It delivers higher computing power but at low-power consumption. The cPCI-3840 is specially designed for industrial automation and control system applications.

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6U CompactPCI Highly Integrated Pentium® M Processor PCI-X Universal Blade

The cPCI-6840 is a 6U cPCI Pentium® M/Celeron® M SBC with 855GME and 6300ESB long-life embedded chipset. It complies with PICMG 2.16, 2.9, and 2.1 hot-swappable specifications. It supports up to 2GB DDR and its rich I/O features include three GbE ports, AGP graphics, four USB 2.0, two UART, two IDE, two Serial ATA ports, and a watchdog timer. The local PCI-X bus is optimized for maximum bandwidth and includes two 64-bit/66MHz PMC sites, dual GbE ports for 2.16, and PCI-X on a universal cPCI bus. Working with the cPCI-R6840 rear I/O module, the cPCI-6840 provides CompactFlash storage, S-ATA, optional SCSI over PMC rear I/O, and optional LVDS graphics.

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The cPCIS-6230R/64 is a 2U-height three-slot CompactPCI chassis. It is equipped with a PICMG 2.1 hot-swap compliant 64-bit 6U CompactPCI backplane with P3 and P5 rear I/O. It supports one dual-slot system board and two peripheral slots. The cPCIS-6230R/64 also features a built-in 300W AC-input power supply, slim type EIDE CD-ROM, floppy drive, and internal space for drive bays for one 2.5" HDD and one 3.5" HDD.

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By Curt Schwaderer

Ethernet switch technology increases performance and flexibility, lowers latency

As Gigabit Ethernet performance continues to increase beyond one gigabit per second (Gbps), another nagging issue arises: latency. Evident especially in data centers where applications are distributed among clusters of servers and storage equipment, latency and data delays cause problems with synchronization of the overall applications. Latency issues can degrade data center applications to the extent that the data center's architecture becomes disjointed, as shown in Figure 1. The compute elements of the data center use specialty switches that might use low-latency communication technologies such as InfiniBand. Storage within the data center may be connected via Fibre Channel. Finally, the enterprise is connected with the inexpensive, scalable topology of Ethernet.

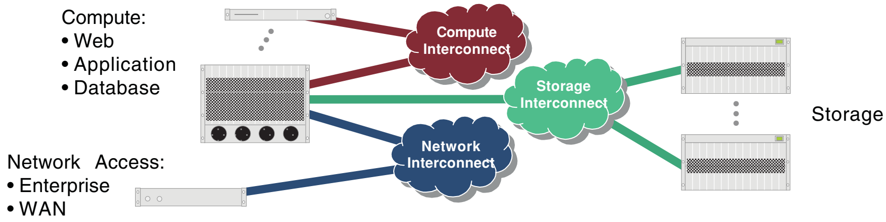

Figure 1

If you're thinking that these data center challenges have nothing to do with AdvancedTCA systems design, think again. These performance and latency issues extend beyond the data center into the heart of the Advanced Telecom Computing Architecture. AdvancedTCA backplane and switching give rise to exactly the same performance and latency issues. Many common AdvancedTCA systems have storage, compute, and network interconnect functions all using the AdvancedTCA backplane to pass data and control information. AdvancedTCA systems are specified to deliver the same kind of data center services, creating significant risk that AdvancedTCA will not be able to meet backplane switching latency requirements for these kinds of applications.

At the Network Systems Design Conference (NDSC) I ran across a new Ethernet switching technology that provides latency characteristics for one and 10 Gb systems that fall well within the latency threshold for data center applications. This new technology from Fulcrum Microsystems enables data centers to adopt a unified, 10 Gb data center architecture with latencies low enough to rival the special compute interconnect topologies of today. It also has the possibility of enhancing AdvancedTCA backplane switches to meet more stringent latency requirements between AdvancedTCA blades as multimedia applications become more prevalent in these systems.

Unified data center

Fulcrum Microsystems uses two key internally developed components to provide low latency, high performance Ethernet switch chips called Nexus and RapidArray. The technology's main objective is to enable unified data center architecture through the use of 10 Gigabit Ethernet. So, with 10 Gigabit Ethernet switching technology that meets performance and latency requirements of the data center, the infrastructure simplifies to that shown in Figure 2.

Nexus is a fully nonblocking terabit crossbar switch. The crossbar itself is benchmarked at three nanoseconds to transport data across chip, which includes arbitration, setup, and tear down of the connection through the switch. So, this fundamental building block enables system-level latency that rivals low-latency technologies such as InfiniBand, yet leverages less expensive, more widely deployed Ethernet topology.

RapidArray is high performance Static Random Access Memory (SRAM), with special features that enable it to run up to twice as fast, yet offer the same yield and density as standard SRAM. One additional feature of asynchronous RAM is that the RapidArray's overall power consumption is typically significantly lower, with consumption taking place only when there is activity through the switch. For example, under full 10 Gb traffic load through the Ethernet switch products using this technology, the products use about 150 mW per port.

Latency

So, what is the data center latency threshold? Figure 3 compares topologies with Fulcum's Nexus plus RapidArray 10 Gb Ethernet switch products called FocalPoint.

The typical data center latency threshold is around 200 to 300 nanoseconds. Fibre Channel provides storage interconnect characteristics that just meet this threshold. The standard 1 and 10 Gb Ethernet products available come with latencies far outside the acceptable bounds, 1 Gb being benchmarked in the low microseconds, and 10 Gb still being more than 500 ns. This issue relegates Ethernet switching to

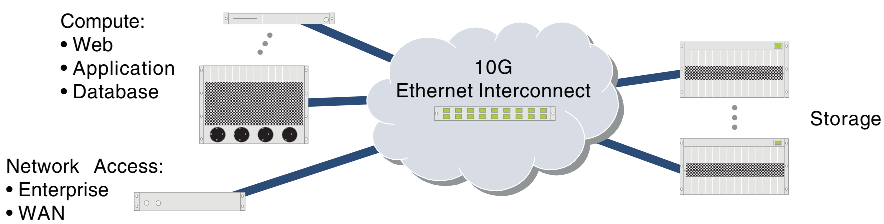

Figure 2

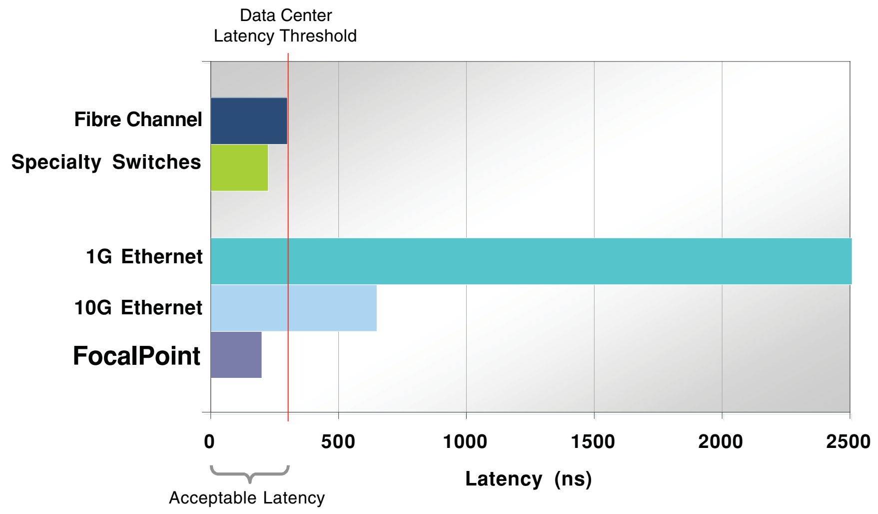

Figure 3

the network interconnect, and specialty switches using InfiniBand technology take care of the actual compute interconnect. Specialty interconnects offer comparable latency to FocalPoint, around 200 ns. The FocalPoint Ethernet switch product that incorporates the Nexus and RapidArray technologies benches well within the latency threshold, making Ethernet once again a viable solution as a compute interconnection within the data center.

Performance

Once the latency issue is resolved to enable a unified, 10 Gb interconnected data center, the architecture simply rides the performance advances of standard Ethernet technology. The simple fact is most data centers and network providers are still an order of magnitude or two from standard Gigabit Ethernet. Therefore, viable technology up to 10 Gbps provides more than enough performance road map for the vast majority of applications involving Ethernet.

AdvancedTCA applications

So what does this have to do with AdvancedTCA? Well, the entire purpose of the AdvancedTCA standards is to create standards and interoperability between components within an AdvancedTCA system that ultimately drives low cost, high reliability equipment for a wide variety of applications. But the backplane fabric interconnect remains open to a variety of standards. PICMG 3.1 through PICMG 3.5 define the use of Ethernet/Fibre Channel, InfiniBand, StarFabric, Advanced Switching, and Serial RapidIO. The reason is very similar to the data center issues already described. But this also has the potential to be the *weak link* in the interoperability chain that is AdvancedTCA. Lack of interoperability in any area of AdvancedCTA runs the risk of slowing adoption and limiting interoperability.

The reason why Ethernet isn't always the obvious choice for the high speed backplane is congestion management. Ethernet link layer flow control can be used at Layer 2 for congestion management, but there is no resolution into the flows riding on top of the link layer. For example, one particular flow may be able to be throttled, allowing all the other flows using the link layer to resume normally. The IEEE 802.3 Working Group is currently adding additional congestion management features to Ethernet in order to solve this shortcoming. In the meantime this is the main issue blocking an interoperable AdvancedTCA backplane solution.

Fulcrum's Ethernet chip has some capability to identify unique flows within the first 16 bytes of the packet. By identifying these flows, the chip can use its flexible port logic to implement some degree of throttling lower priority data on a link in congestion management situations. Furthermore, the flexible port logic allows the ability for the chip to switch based on this unique 16 bytes as programmed. So, these chips provide the ability to add flexibility by including congestion management and proprietary header switching within an AdvancedTCA system.

Programming the device

Software that enables easy integration into the platform and OS used is key to successfully incorporating sophisticated switch chips that support port switching and configuration. Figure 4 shows

Fulcrum Microsystems' software architecture for the device.

As Figure 4 depicts, a device driver implements calls to control and configure the device. A device access API exposes all the services available from the chip. From there, the device would typically be integrated with a Layer 2 switching protocol stack. Fulcrum has used the device access API to create the adaptation layer to the LVL7 switch stack. Fulcrum has also implemented the software using an operating system abstraction layer to facilitate porting to other operating systems. Thus far, the software environment has been ported to Linux and VxWorks running on the PowerPC processor, although this model can very easily be migrated to other processor platforms as needed.

The following services are provided through the device access API:

- Initialization: Device initialization and configuration for operation
- Switch management: Setting switch attributes, setting switch to active/inactive, and getting a list of switches
- Virtual Local Area Network (VLAN) management: Configuration and management of port-based VLAN
- Port management: Port enable/disable and attributes
- Address management: MAC address insertion, removal, and set table aging characteristics
- Link aggregation management: Setting up link aggregation groups from a set of ports and managing characteristics of those port groups
- Quality of Service (QoS): QoS global management for the device, per port, per VLAN, or per MAC address
- Statistics: Access statistics at multiple levels, the switch chip, per VLAN, and per port
- Packet transmission and reception characteristics: Customize the header switching characteristics of the device
- Event reporting: Reports for anomaly situations or activity through the device including switch and per port state, VLAN access violations, and transmission and reception characteristics

The Fulcrum driver is also implemented using a buffer management API that expects to be able to get and free a buffer, set a buffer length, and set the content offset in the buffer. These are standard services provided by UNIX *mbuf* and Linux *zbuf* facilities, so implementing the buffer management API is straightforward.

For a flavor of the API, Figure 5 shows an API call in the Fulcrum services API that gets the attributes from the switch chip.

Using the port aggregation API, users can set up and control transmission of a set of input ports through the switch chip. Link aggregation groups can be configured to have packets from the group dropped, sent to the CPU, or passed through to an output port.

The QoS and queue management API provides a very robust set of facilities that allow per port and global management of receive and transmit port queues. High and low watermarks can be set up globally and/or on a per port basis to implement up to eight queue priorities per port for the implementation of IEEE 802.1P.

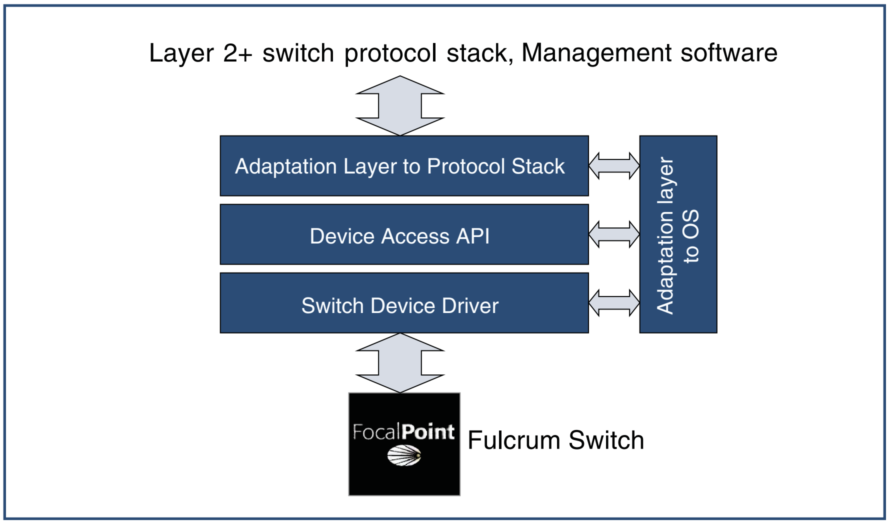

Figure 4

```
fmDriverGetSwitchInfo ()
Synopsis:     fm_status fmDriverGetSwitchInfo (fm_int switch, fm_switch_info *argv);
Description:  Get information about this switch.
Inputs:       switch: Switch number
              argv: Pointer to a location to store the information
Outputs:      *argv: Information about this switch
Returns:      FM_OK: Success
              FM_FAIL: Cannot access the switch

The fm_switch_info structure is:
struct {
    fm_int model;           // The model of this switch
    fm_int env;             // The environment for this switch
    fm_int32 info[32];      // Information about the environment
                            // around this switch:
                            // info[0] = Control CPU clock
                            // info[1...8] = EPL clocks
fm_int physicalPorts[FM_MAX_PORT];
                            // Map of logical port to physical port
                            // physicalPort[0] = 0 (CPU)
                            // physicalPort[1] = X
                            // ..etc..
} fm_switch_info
```

Figure 5

Products

The Fulcrum Microsystems product line consists of the PivotPoint family of SPI-4.2 line card switch chips and the newly announced FocalPoint device, a backplane switch chip specifically targeted for applications such as AdvancedTCA backplane switching. The FocalPoint FM2112 is an eight port by 10 Gb plus 16 port by 1 Gigabit Ethernet switch. The eight ports are XAUI interfaces. Each interface supports quad Serializer/Deserializer (SERDES) and single SERDES modes. Each 10 Gb port can be overclocked up to 12.5 Gbps. The FocalPoint FM2224 is a 24 port by 10 Gigabit Ethernet XAUI switch.

Both FocalPoint devices include eight priority level queue management with programmable Weighted Random Early Discard (WRED) algorithms to support IEEE 802.1P priority queuing specifications. The part can be programmed for either strict priority or weighted round robin scheduling algorithms. Jumbo packet support is also included. MAC tables within the part are 16K entries and provide configurable hardware aging and the ability to lock entries in the table. For switch fabrics passing Ethernet on top of proprietary headers, the parts can also be configured to bypass the proprietary header by adjusting an offset into the packet or use the proprietary header to make switching decisions. In addition, the parts gather multiple statistics for RMON and SNMP instrumentation and incorporate VLAN recognition for port-based VLAN processing.

Fulcrum Microsystems also offers the FocalPoint FM2224-EP 10 Gigabit Ethernet interconnect evaluation platform. The platform has options for a variety of connectivity options, an embedded Linux operating system, and commercial Layer 2 control plane software from LVL7. The part itself comes with drivers and software to ease integration with operating systems and control plane software. The API provides a simple interface for controlling the flexible port logic within the chip, and the adaptation layer makes it possible to port the software to a number of operating systems.

The current PivotPoint products include the FM1010 and FM1020. These parts feature a SPI-4.2 interface that is quickly becoming the de facto standard for communications chip interfaces. SPI-4 is used by multiple NPU manufacturers, security coprocessor, and interface chip developers. The FM1010 features six SPI-4.2 interfaces; the FM1020 provides three SPI-4.2 interfaces in a smaller package.

All these parts are manufactured using a 0.13 micron process for a high level of integration in a small footprint. For example, the FM1010 product is a 1232-ball Ball Grid Array (BGA) geometry with the FM1020 being half that size.

Conclusion

Standardization and ubiquity in data centers and AdvancedTCA alike drive easier to maintain, lower cost architectures for a wide variety of applications. Ethernet switching products that address latency and congestion management issues look like enablers to extend Ethernet topologies far into the data center and into the heart of the AdvancedTCA backplane.

For more information, contact Curt by e-mail at cschwaderer@opensystems-publishing.com.

By Hermann Strass

European events promise bright future for AdvancedTCA and CompactPCI

European events

The Storage Networking World (SNW) trade fair is Europe's largest exhibition and conference for storage-related equipment and software. The event was held September 5-6, 2005 in Frankfurt, Germany. Some blade-based systems use CompactPCI and will use AdvancedTCA boards for reliable storage networking.

Messe Muenchen, a large trade fair held in Munich, Germany is organizing LASER China 2006 (March 21-23). This event will be co-located with Electronica China, productronica China, and Semicon China at the New International Expo Center in Shanghai, China. For a report on LASER2005 held in Munich, Germany see the October 2005 issue of *CompactPCI and AdvancedTCA Systems,* Technology in Europe column (available online at www.compactpci-systems.com).

The Embedded Systems Show (ESS), UK's largest event for systems engineering and embedded software development, was held October 19 to October 20, 2005 at the National Exhibition Centre (NEC) in Birmingham, UK (Figure 1). Major topics discussed were bus-based modules, FPGA, the embedded micro developer forum, signal integrity, test, communications, and software design. The exhibition space was 50 percent larger than 2004.

The European Conference on Optical Communication (ECOC), held September 25 to 29, 2005 in Glasgow (Scotland, UK), attracted 3,000 visitors and 1,000 conference delegates to the Scottish Exhibition and Conference Centre (SECC) from all major worldwide players in its 31st year (Figure 2). It provided up-to-date information for telecom network builders and operators. ECOC is Europe's largest conference and exhibition devoted to fiber-optic communication technologies. Researchers from the Heinrich-Hertz-Institute (HHI), part of Fraunhofer Gesellschaft (FhG) (Germany), broke a five-year old record by sending 2.56 Tbps through a 160 km (100 miles) long glass fiber at ECOC. The HHI researchers broke two more world records by sending 1.28 Tbps through a 240 km (150 miles) long fiber and by sending 160 Gbps through 4,000 km (2,500 miles) of fiber. Bell Labs (US) demonstrated the first reported transmission of 100 Gbps Ethernet traffic over optical fiber using duobinary signaling.

The Ministry of Information and Communication of the Republic of Korea presented detailed information about their IT839 Strategy plan at European trade fairs. The plan calls for the rapid development of eight services including Telematics, RFID, W-CDMA, Terrestrial Digital TV, VoIP, Digital Multimedia Broadcasting, and others, three infrastructures, such as IPv6, and nine growth engines, including, to name just two, Intelligent Robot and Next-Generation Mobile Communications. The goal is to develop competitive technology and increase production of goods, employment, and exports from $85 billion in 2005 to $110 billion in 2007 and more in the following years.

Figure 1

Figure 2

The presentations and exhibits on several of these telecom oriented events indicate that substantial data traffic will be transported and distributed locally. Any available transportation capacity will be used up sooner or later. Therefore there will be a need for supporting switches and other communications equipment, many of which could be supplied by future AdvancedTCA and CompactPCI systems.

European applications

SMA Technologie AG (Germany) supplies CompactPCI systems into many highly automated industrial projects and transportation systems. All these systems require watchdogs in addition to many other components. A CPU watchdog is a hardware component for monitoring software. This is nothing exotic. However, an important feature is how the watchdog is integrated into the hardware and software concept. SMA has developed intelligent and practical watchdog solutions, with special focus on the requirements of modern real-time operating systems. Watchdog triggering has to be carefully planned, otherwise chaos might result from frequent and erratic triggering in or out of nested subroutines or subfunctions. Deterministic watchdog triggering is required for systems operating on a higher Safety Integrity Level (SIL). The watchdog included in CompactPCI-based CPUs (CompactMAX series) from SMA is equipped to simply and effectively integrate it into demanding real-time applications.

European products

Acqiris (Switzerland) is using its proprietary, extreme high-speed single, dual, and quad channel 10-bit digitizers for CompactPCI, PXI, PCI, and VXI applications. The boards using these Analog-to-Digital Converters (ADCs) offer sampling at a rate of eight GSps with 10-bit accuracy and 1 Gigapoints of acquisition memory at up to 3 GHz input bandwidth. Their 6U CompactPCI streamer analyzers, such as the SC240 or SC210, provide streaming rates of up to 25 Gbps using a high-speed Optical Data Link (ODL), compliant with the Serial Front Panel Data Port (SFPDP) protocol in applications such as Synthetic Aperture Radar (SAR), using LabView software from National Instruments (NI) to analyze the data.

Artesyn Communication Products, Inc. in Edinburgh (Scotland, UK) develops and supplies the communications software, such as SIGTRAN/SS7, to all parts of Artesyn Technologies, Inc. (US). The Communication Products Group's Spiderware product line comprises two primary types of protocol software: control software and data software. Both types of software are bundled with different interface boards to provide a subsystem for customers' communications infrastructure applications.

The new 3U CompactPCI CPU card F11 from MEN (Germany) uses several innovative concepts for highly effective CompactPCI and PXI applications. The CPU part of this card is actually located on the plug-on mezzanine EM07. CPU performance, electrical power, and functionality can be optimized or upgraded by just changing the mezzanine. An FPGA further enhances the modularity with field-programmable functionality and I/O options. This provides an endless combination of I/O options without the need for individual option boards fixed by initial hardware assembly. The required connectors for the various I/O options, including CAN and other non-PC serial I/Os, may be located on front panels up to seven slots wide. FPGA updates may be entered into the Boot flash during operation. They will be automatically loaded during the next boot cycle.

The EM07 is a member of the growing number of Embedded System Module (ESM) mezzanines from MEN. ESM modules were one of the first System-On-Module (SOM) or Computer-On-Module (COM) products when they were introduced in early 2004. Due to their success on the market, MEN opened the design guidelines of ESM technology to interested users. ESM technology is not just another mezzanine variant. ESMs can be used as standalone computers with I/O functions and connectors. The onboard FPGA is just another PCI device in the ESM architecture. MEN can integrate their own or third-party IP cores. Starter kits are available for all types of ESM modules. For a copy of the MEN design guidelines visit www.men.de.

Rittal (Germany) and its Kaparel (Canada) subsidiary have developed a *cube* style enclosure for up to 16 Advanced Mezzanine Card (AdvancedMC) boards with front and rear access. The cube can be rack- or wall-mounted. The AdvancedMC draft standard (developed by PICMG) will standardize AdvancedMC modules for use as mezzanines on AdvancedTCA carrier cards. The cube cage from Rittal is a variant of the proposed MicroTCA enclosure standard, where AdvancedMC boards are used on a backplane instead of on a carrier card.

For more information, contact Hermann at: hstrass@opensystems-publishing.com.

By Shyam Chandra and Cleo Mui

Low-cost monitoring and control of AdvancedMC management signals

The AdvancedTCA standard ratified by the PICMG 3.0 R2.0 subcommittee states that a carrier card AdvancedTCA Field Replaceable Unit (FRU) can support up to eight Advanced Mezzanine Cards (AdvancedMCs) plugged in from its front panel. Each AdvancedMC connector on the carrier provides for management interface, power feed, fabric interface, clocking, and control plane interface. This article examines the signal generation for the management interface.

The carrier's Intelligent Platform Management Controller (IPMC) controls the management interface of the AdvancedMC. The AdvancedMC management interface on the carrier card should be able to recognize AdvancedMC card insertion and extraction, enable AdvancedMC, and communicate with the AdvancedMC through an isolated Intelligent Platform Management Interface Bus (IPMB). Management signals control all these functions.

Management interface implementation

The block diagram in Figure 1 illustrates the implementation of the management interface recommended by the PICMG 3.0 committee. The management interface consists of the following signals:

- PS0# – This pin extends a ground signal to the AdvancedMC module. This signal is used to detect insertion of the AdvancedMC module.
- PS1# – The AdvancedMC module returns the ground signal received from PS0#. A ground on this signal indicates that the AdvancedMC has been plugged in.
- Enable# – A signal generated by the carrier to enable the management interface of the AdvancedMC. This signal becomes active when the AdvancedMC PS1# is detected and is used to reset the AdvancedMC.
- Isolated IPMB-L – This is a copy of the local IPMB bus on the carrier. Each IPMB-L copy must be isolated from the carrier IPMB-L by means of an isolator IC or a FET. The enable signal generated by the IPMC controls the isolator mechanism that prevents a faulty AdvancedMC from locking up the IPMB-L bus of the carrier.

Figure 1 illustrates up to 8 copies of the AdvancedMC management control interface implemented in a carrier. This implementation requires 8 isolator ICs, 16 control signals, 8 gates, and 8 inputs.

Integrating management control functions on the carrier board

Typical candidates for the integration of all AdvancedMC management control functions are the IPMC microcontroller or an FPGA.

Integrating management interface control into the IPMC microcontroller

Integrating AdvancedMC management hardware functions into the IPMC microcontroller uses its I/O port pins to provide all management control signals. Usually, the number of I/O ports in standard and off-the-shelf microcontrollers are limited (around 24 to 32). Most of those microcontrollers will be used for implementing other standard IPMC functions. Consequently, to implement the entire AdvancedMC management control interface using the microcontroller I/O port pins, designers must use either a larger, or additional, microcontroller. Further, the software should poll for these signals continuously to recognize AdvancedMC card insertion or extraction. Since different carrier boards require a different number of AdvancedMCs and have different LED drive requirements, the IPMC software for each board should be debugged and tested. It is preferable that the standard functionality be implemented in every board the same way. In this case, modifying the standard design to accommodate unique AdvancedMC interface designs will force additional testing and debugging of the IPMC design for every board, increasing its time to market. Furthermore, the design must also use additional IPMB isolator ICs and NAND gates.

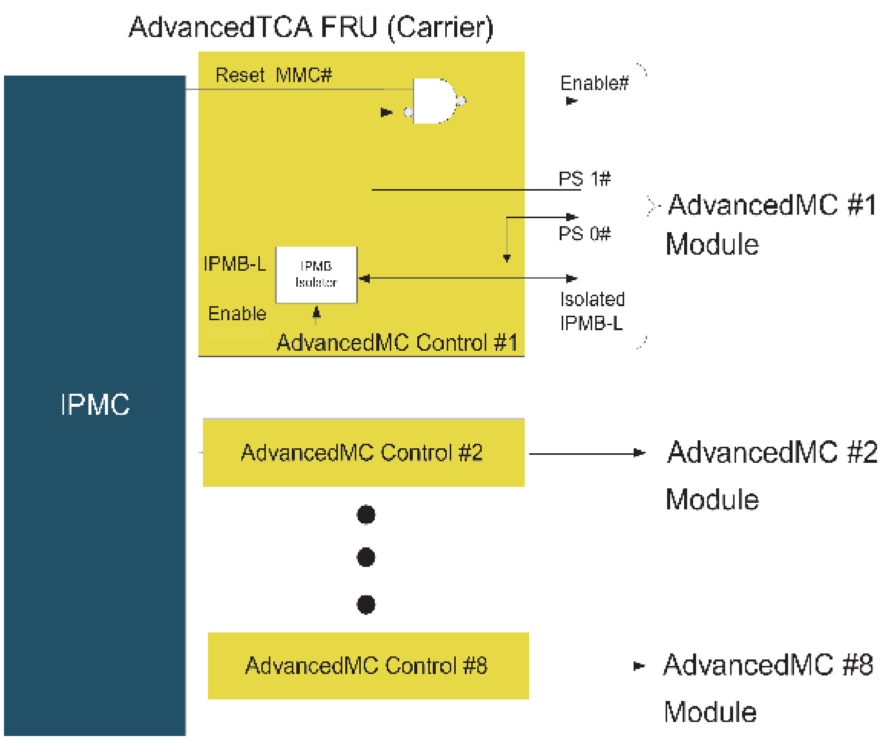

Figure 1

Integrating management interface control into the existing onboard FPGA

If the carrier had an FPGA with free pins and free logic that could be used to implement the entire management control interface, it would be possible to save all the I/O port pins on the IPMC. If all the IPMB isolator functions also were implemented within the FPGA, it would require 18 more pins (nine IPMB interface with two pins each), for a total of 42 pins. FPGAs on AdvancedTCA carriers often have high-performance I/O interfaces; using high-performance pins to implement slow card scan functions can be an expensive technique. In addition, each carrier design will require a different methodology, depending on FPGA resource availability. Consequently, implementing the AdvancedMC management control interface in an FPGA is more expensive than the discrete counterpart. In some cases, the increased number of pins required for IPMC management will require an FPGA in a much larger package. That means a larger and more expensive FPGA that occupies a larger area of the circuit board.

Monitoring and control of AdvancedMC management signals using a low cost, nonvolatile PLD

The use of a low cost Programmable Logic Device (PLD) will reduce both the processing load on the IPMC and the number of circuit board interconnections.

One such device is the nonvolatile, instant-on MACHXO, a new class of *crossover* PLD that supports applications traditionally addressed either by high density CPLDs or low capacity FPGAs. By using 130 nm nonvolatile embedded Flash process technology, and an industry-standard four-input Look-up Table (LUT) approach for logic implementation, these new devices combine the desirable features of both Complex PLDs (CPLDs) and FPGAs.

Figure 2 illustrates how the Lattice MACHXO device can be used to implement all of the management signal interface functions.

Block diagram description

Starting from the bottom left of the block and proceeding clockwise, the MACHXO device interfaces to the IPMC carrier via the IPMB-carrier pins. The AdvancedMC card interrupt signal is generated whenever any AdvancedMC module is inserted or extracted. The AdvancedMC Enable# 0-7 signal generation logic satisfies the standard specification. These signals also respond to the reset signal loaded by the IPMC through the IPMB-carrier interface. The AdvancedMC Present# 0-7 signals are monitored by the MACHXO, and are used to generate the corresponding AdvancedMC Enable# signal as well as the generation of the AdvancedMC card interrupt signal to the IPMC to signal the change in status. The AdvancedMC IPMBL #0-7 is the IPMB-L bus for each of the AdvancedMCs.

Functionally, the block diagram can be split into four blocks. The I2C bidirectional Mux/Demux block replaces the eight IPMB isolators shown in Figure 1. The I2C slave with Programmable Address provides a slave I2C interface to enable the IPMC to:

- Read the AdvancedMC Present signals
- Generate Reset signals for the AdvancedMC
- Enable the generation of logic through the I2C input and output interface block

The Input Port Status Change Interrupt Generator monitors the AdvancedMC present signals. When any of the AdvancedMC Present# 0-7 change, the AdvancedMC Card interrupt signal becomes active, interrupting the IPMC. In response to the interrupt, the IPMC can read the AdvancedMC Present register through the I2C slave block and take appropriate action.

The IPMC can control and monitor the AdvancedMC using the following sequence of instructions as shown in Figure 3.

Additional AdvancedMC management functions

Implementing these additional functions can enhance the design.

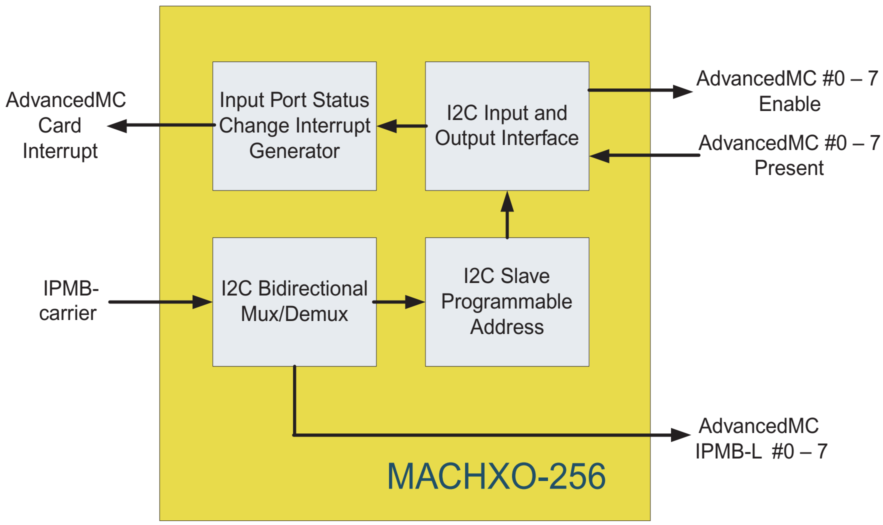

Figure 2

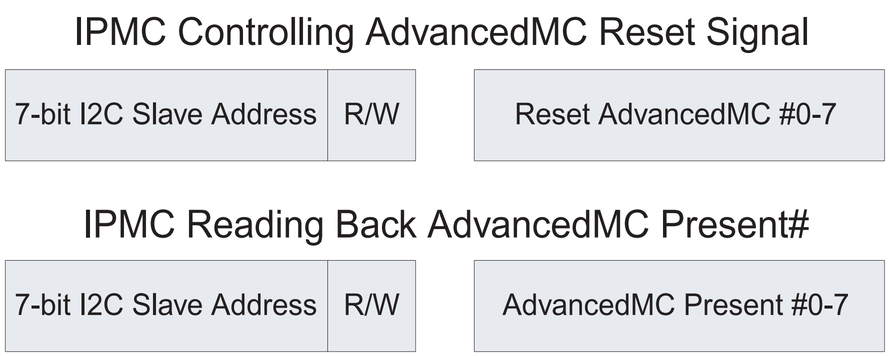

Figure 3

I2C timeout

One limitation of a shared serial bus like the I2C bus is that if any of the devices on the I2C bus pulls either clock or data bit low, it prevents any of the I2C devices from taking control of the I2C bus. In this case, if an AdvancedMC develops a fault and pulls one of the I2C bus bits low, it affects all IPMB-L related operations. Implementing a timeout feature in the Mux/Demux block will automatically turn the faulty input port off, freeing the IPMB-L bus.

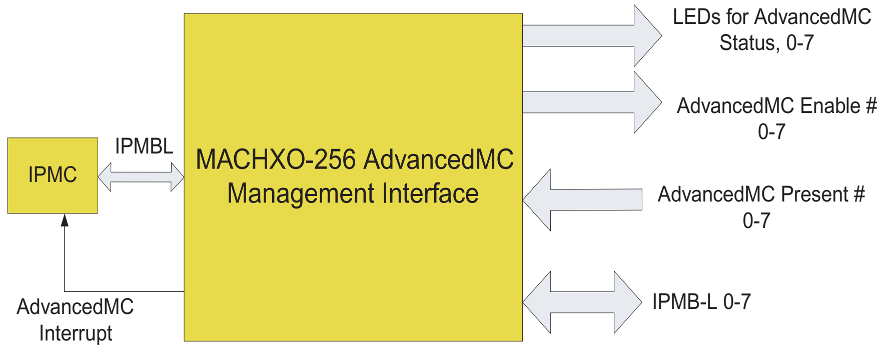

Figure 4

Additional control ports for the LED drive

PICMG 3.0 R 2.0 specifies that the carrier card should implement Blue LED to indicate that the AdvancedMC can safely be extracted. Since up to four LEDs per AdvancedMC card may be required for various indications, the MACHXO device can further reduce the cost of implementation by accommodating multiple LED control ports for each AdvancedMC

Note that Figure 4 is illustrating the interconnection arrangement with IPMC managing all the AdvancedMCs using the MACHXO.

Advantages of using a nonvolatile PLD for AdvancedMC management

Integrating the management interface and IPMBL isolation into a MACHXO device results in a lower cost, a smaller circuit board area, and a reduced component count. The number of I/O ports for AdvancedMC management is now reduced from 34 to 2 (eight IPMB Enable, eight Reset, eight AdvancedMC Present, eight Blue LEDs, and two for I2C port).

Additional features, such as the timeout mechanism that protects the board from a faulty AdvancedMC, can be added by simply modifying the code on the MACHXO device.

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Building better VoIP solutions

By John Brandte

Voice over IP (VoIP) is being talked about everywhere today, but the implementations often leave something to be desired in terms of robustness and serviceability. Getting the application layer right is only part of the answer.

What's still missing? Often it's a sound implementation of the physical layer Wide Area Network (WAN) access. Getting this critical Layer 1 foundation wrong can mean anything from support problems to a product that isn't viable. Layer 1 interfaces aren't just connective elements, the T1/E1, T3/E3, or SONET/SDH physical layer interfaces require sophisticated features and management capabilities.

In addition to having to provide all the same capabilities of a traditional WAN telephony environment, developers of VoIP physical layer interfaces must often deal with more than one carrier and transport technology as they cross the WAN. The result is that isolating faults and fixing them cost-effectively can become problematic.

The challenge

Converged voice and data networks have always been challenging, as the two information types have significant differences in latency tolerances and in their requirements for accuracy of content and delivery. (See Figure 1.) Although VoIP protocols are now able to address these issues more effectively than before, there is still room for improvement.

Line jitter, end-to-end latency, and round-trip delays have always affected voice transmission quality. VoIP often adds to the problem by using packets, thus introducing new types of jitter, new sources of delays, and transmission integrity issues associated with packets. Adding new sources of quality degradation increases complexity exponentially. If accepted limits are exceeded, they will negatively impact the quality of VoIP application, or even cause it to fail completely.

Overcoming the challenges

The place where the required robustness and signal quality begin is at the physical layer. Solid Layer 1 WAN engineering optimizes packet transmission integrity, while minimizing any delay and jitter issues. End-to-end line monitoring and control enables predictive fault management and provides an early alert of potential problems – giving the VoIP traffic an optimal environment for accurate transmission, minimal delays, and increased uptime.

A list of problem areas in the engineering of VoIP Layer 1 interfaces would have to include:

- Flawed timing and signaling implementations
- Inadequate understanding of the applicable standards and regulatory issues
- Insufficient management capabilities, particularly as it pertains to the WAN

The bottom line is that most engineers approach these interfaces from the data network perspective, with the result that their VoIP physical layer interfaces often lack the management, troubleshooting features, and robustness of carrier class voice networks.

Physical layer interfaces – where functions reside that are critical to monitoring line health and isolating/resolving line problems after a hard failure – tend to lack key features, resulting in products that are not carrier grade.

These missing features not only impair predictive problem identification and resolution, they reduce the ability to isolate, avoid, and/or rapidly repair hard failures. Carrier grade call quality is difficult to establish and maintain when intermittent line interference disrupts signal quality.

Timing is everything…

VoIP WAN interfaces are high speed and require high bandwidth. And that means that hardware engineers working on these interfaces need to thoroughly understand regulatory issues embodied in the FCC rules and T1/T3 standards, not to mention carrier environmental considerations, and high-speed signal design, required to address VoIP's faster clock rates.

High-speed signals require careful planning during the design phase and throughout the implementation phase. The more quickly interfaces send and receive packets (that is, the faster the clock rate), the faster the hardware has to be in order to handle both the data and overhead. This means that hardware must tolerate high frequencies.

The higher the frequency of the signal, the more "fragile" it will tend to be. High frequency signals are more sensitive to nearby signals and can even become a source of noise that disrupts other signals. High frequency signals are also prone to greater power loss over distance.

Meeting the standard

Of all the problems in VoIP implementations, one of the most serious lies in the

	Data	Voice
Delay Tolerance	High	Low
Error Tolerance	Low	High

Figure 1

omission of critical aspects of the alarm, Performance Monitoring (PMON), and signaling code needed for management. In contrast to the traditional telephony networks that we all know and love, the VoIP physical layer interface is – more often than not – feature-poor and not nearly reliable enough to qualify as "carrier quality."

When key features are omitted, the ability to isolate and correct problems prior to a hard failure is severely impacted, and it becomes difficult to establish and sustain stable calls with intermittent, hard-to-diagnose line problems disrupting call quality.

When physical layer interface code doesn't meet regulatory requirements and isn't compliant with ANSI, CCITT, ITU, and numerous de facto carrier standards, problems are inevitable and interoperability is jeopardized. And, if keeping up with all of today's standards wasn't difficult enough, these regulations and standards are continually changing and new ones are being formulated to address emerging application requirements.

The primary standard for us to consider in North America is the ANSI T1.231 family of standards, which applies to the physical layer of T1, T3, and SONET. T1.403 and T1.404 deal with T1 and T3, while T1.105 applies to SONET. VoIP WAN interface technology is also defined by additional international standards.

Just by understanding and correctly implementing needed features in compliance with these standards, developers will go a long way towards ensuring that their products are robust and interoperable. Too often, engineers don't fully research and understand the standards that apply to the alarm processing, performance monitoring, and signaling functions until it's too late.

Layers of complexity

Traversing multiple networks – as VoIP calls tend to do – adds complexity. A VoIP call might originate on a private Ethernet network, enter the WAN via another provider's T1, move into a Central Office switch, and get groomed as SONET OC-48, before being handed off to another carrier's leased network for cross-country transport.

The leased bandwidth is really managed by a different long distance carrier. Another provider might receive the OC-48, extract the T1, and encapsulate it in a T3 packet for delivery to a major corporate campus where the Ethernet/VoIP is extracted and delivered to another VoIP phone. Figure 2 shows where the two networks meet or collide, depending on the implementation of the physical-layer interfaces

Or the VoIP call may go through a gateway where the call is translated into traditional telephony. In this case, the call set-up from VoIP must be converted into a traditional signaling method like Robbed Bit or Channel Associated Signaling, so the far end thinks it is talking to a conventional caller.

The ability to segment the network to isolate problems in this environment is critical, as is the ability to pinpoint the location of service failures in an environment of back-to-back-to-back SLAs, owned by different providers. Without

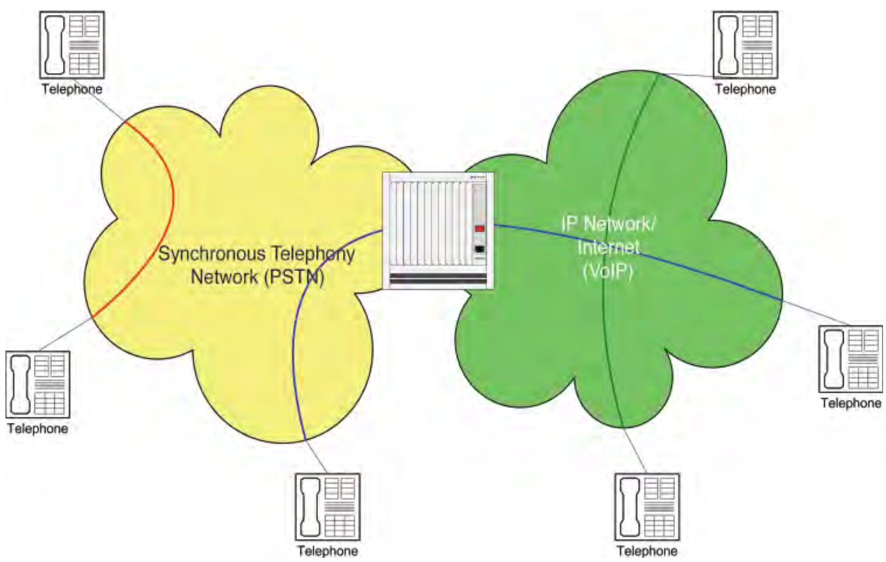

Figure 2

intelligent, standards-compliant alarm functionality and performance monitoring, customers won't know if they are getting what they're paying for, service providers won't understand where their failures are, and overall VoIP service levels won't be objectively managed.

> "Of all the problems in VoIP implementations, one of the most serious lies in the omission of critical aspects of the alarm, performance monitoring (PMON), and signaling code needed for management."

Carrier-quality management

Three physical layer management functions are critical here: alarm processing, PMON, and signaling.

Alarm processing

Alarms are needed to ensure reliability, isolate faults, and resolve problems quickly in the event of hard failure.

Alarm processing is triggered on the appearance of a fault, which evolves over time into an alarm. A fault or defect may generate an immediate alarm indication (integration time = 0) or may continue for a specific time period before an indication is raised (integration time > 0). An integration time > 0 recognizes that some noise on the line or "glitches" are normal and should not generate alarms until they exceed certain tolerances.

The T1.231 standard defines a series of alarms, including Loss Of Signal (LOS). Alarm software must handle multiple events, be able to deal with concurrent faults, and be capable of transmitting alarms when necessary.

Voice applications are typically more complex than their data counterparts. When brief, intermittent line problems occur, phone calls in progress must be sustained, through the freezing of signaling bits in their last known viable state. If signaling bits are not "frozen," a LOS will garble the signaling bits, with the result that the system interprets this as a change-of-call state.

When LOS is found, the integration timer must be initiated and signaling states frozen while the system determines whether the fault is momentary or persistent. If the LOS never becomes a failure, call states aren't altered, and no calls are lost. If a LOS failure does occur, all calls are terminated, and the Remote Alarm Indication (RAI) is transmitted.

Performance Monitoring (PMON)

PMON is the capability designed mostly to provide warning of problems prior to hard failures or it can give the physical layer network the information it needs to do automatic rerouting. Performance data is also valuable in pinpointing the exact location of failures after they occur. Documenting performance is important to providers to verify service levels.

PMON functions also include loop-backs. Loop-backs are an important tool used to test lines and the stages inside transceivers. Threshold Crossing Alerts (TCAs) are an often-omitted feature, but they're important for enabling network managers to set their alert levels and fine-tune the defect reporting.

PMON provides the detail carriers need to support remote troubleshooting and avoid costly truck rolls when they're not really necessary. Faults that occur as a result of badly configured systems and poorly provisioned services can be isolated and resolved more quickly through the use of PMON data.

Signaling

VoIP gateway signaling functions handle different signaling modes. North American networks alone have more than 40 different types of signaling, and problems can occur if signaling models are incompatible, with the result that calls can fail completely.

VoIP has two competing signaling methodologies, Session Initiation Protocol (SIP) and Media Gateway Control Protocol (MGCP), which augment telephony voice signaling protocols in VoIP applications. Both SIP and MGCP are Layer 3 protocols, but in gateway applications they must talk to the physical layer signaling on the public network side to ensure accurate translation both into and out of the VoIP network.

Developing solid VoIP interfaces on both sides of the gateway

Designing the physical layer interface can be more challenging than other aspects of VoIP development. The VoIP side of the interface generally uses a traditional WAN (T1/E1, T3/E3, SONET/SDH) circuit for IP packet transmission.

Other considerations come into play on the PSTN or public network side of the VoIP gateway. This is where call setup signaling from the IP side is translated into signaling recognized by the traditional telephony network. The same WAN platform can be used with the addition of the appropriate signaling capability. As we discussed earlier, bit freezing must be properly implemented to ensure call integrity. As Figure 3 illustrates, the stability and robustness of each layer depends on all the underlying layers. A flawed Layer 1 equals an unstable VoIP application.

Beyond the physical

And as important as the Layer 1 foundation is, there are serious issues to be addressed throughout the entire VoIP network.

One of the primary reasons that prior attempts at converged voice and data networks have failed is the opposing accuracy and latency requirements as mentioned earlier. Improvements have been made to prioritize voice traffic to minimize delay problems, but VoIP today is often of noticeably poorer quality than traditional telephony.

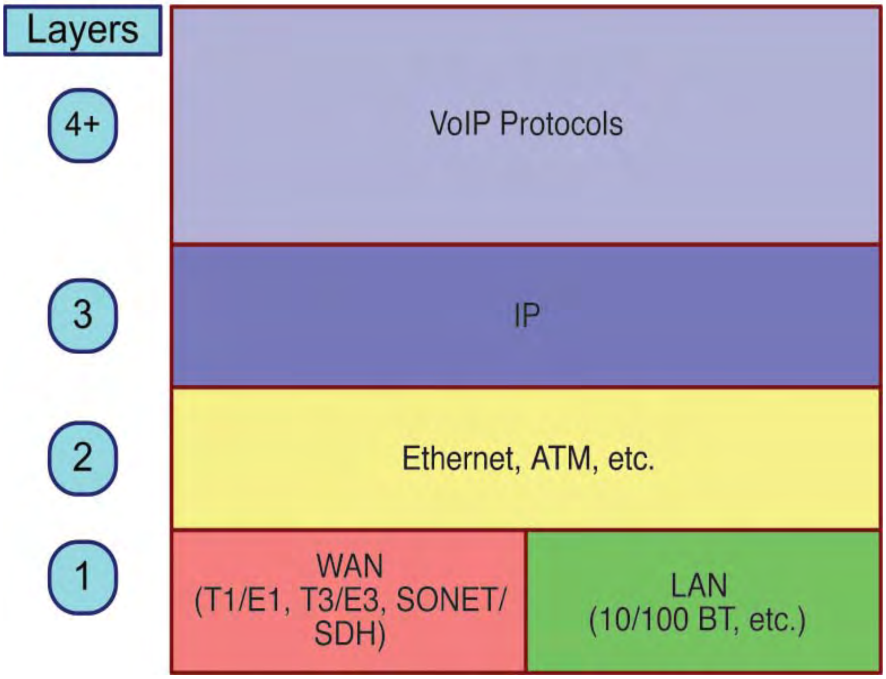

Figure 3

In mixed environments of VoIP and traditional telephony, the consistency of Caller ID and Call Completion often fails to meet customer expectations. These issues have impacted both customer satisfaction and adoption rates, despite VoIP's advantages from a cost perspective.

Among other potential issues is security. Packet-based traffic is inherently less secure than its circuit-based counterpart. Intercepting Ethernet traffic including voice transmissions is relatively easy. The difficulty of decoding the intercepts is directly related to the security/encryption schemes employed. Although this is improving, there is still reluctance in some applications to allow people without specific authorization to access packets – no matter how encrypted they are.

Another issue to be considered is network interference. Physical layer Ethernet is beginning to have embedded OAM capabilities like those available in traditional WAN networks. As these networks utilize in-line devices to aid in segmentation and troubleshooting, there is a risk that unauthorized people will be able to manipulate alarms and loop-backs, which would result in the equivalent denial of service attacks.

Like the physical layer issues we discussed earlier, none of these issues at higher layers in the VoIP stack is a "deal breaker" as long as it is resolved. There is no doubt that these and other issues are and will continue to be addressed in vendor organizations and standards bodies.

But in the final analysis–no matter what evolves at other layers of VoIP or what happens in terms of regulating IP-based telephony – having a solid, well-implemented physical layer is what provides the foundation for everything that comes after it. Its design and implementation should not be an afterthought.

***John Brandte** is vice president of marketing and business development at NComm, a provider of wide area networking source code, software and custom consulting. John is the co-author of* The Communications Developer's Handbook.

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AdvancedTCA, AdvancedMC, and MicroTCA power next-generation telecom equipment

By Stuart Jamieson

The future looks bright for telecom. Service providers are building out their broadband packet networks to offer enhanced wireless, data, video, and VoIP services. And Telecom Equipment Manufacturers (TEMs) are working overtime to provide the equipment that service providers need to deploy these networks and services.

As TEMs formulate their design and platform strategies, they must grapple with the age-old question of what to build in-house, and what to outsource. Historically, TEMs have built virtually everything in-house. More recently, though, deregulation has made the service and equipment landscape increasingly competitive, making it difficult to deliver homegrown equipment in a timely, cost-effective fashion.

Component and subsystem suppliers are eager to help TEMs with their outsourcing efforts. Utilizing open platforms like AdvancedTCA, AdvancedMC, and MicroTCA, OEM suppliers now offer a wide range of system level hardware and software that makes outsourcing both convenient and cost-effective.

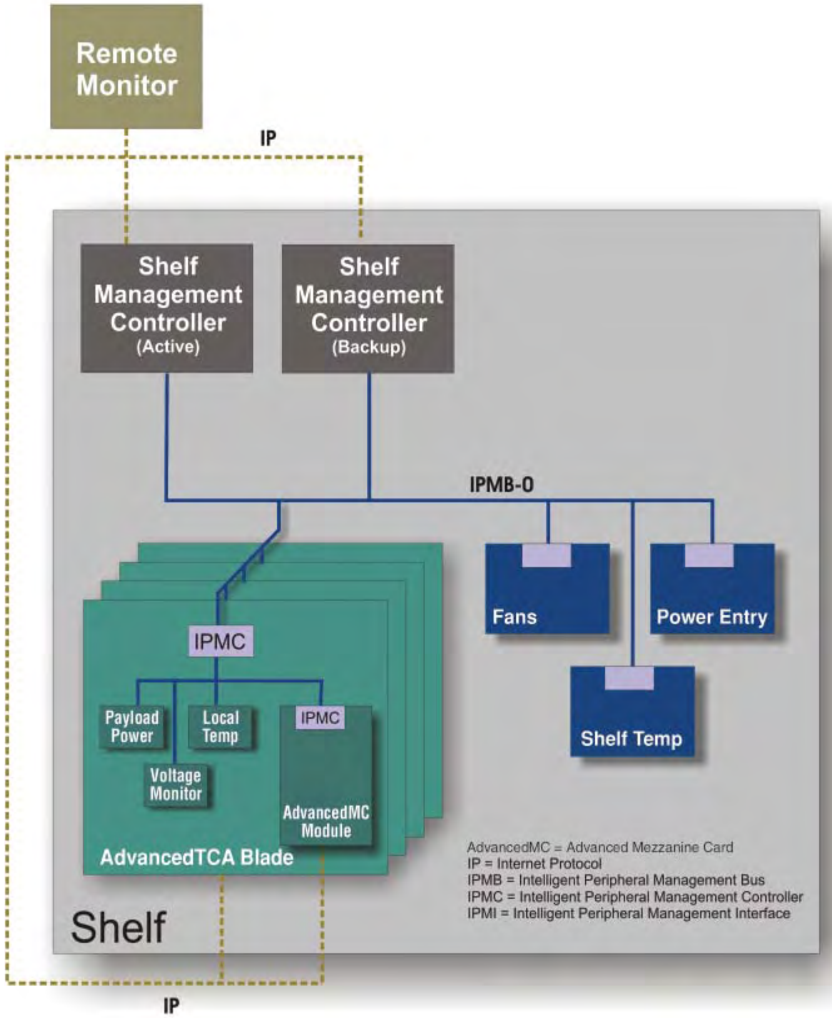


Figure 1

CAPEX and OPEX savings

One of the greatest contributors to overall CAPEX and OPEX savings in AdvancedTCA systems is AdvancedTCA's redundant Intelligent Platform Management Interface (IPMI) system control framework, as shown in Figure 1, which facilitates active monitoring of and control over individual AdvancedTCA blades. The IPMI includes an Intelligent Peripheral Management Bus (IPMB) and an Intelligent Peripheral Management Controller (IPMC). This capability is especially important for high-density systems utilizing large numbers of high-performance processors, where thermal control and power management are major concerns.

IPMI utilizes the I2C-based physical interface, the IPMB, to link chassis management with board-level Field Replaceable Units (FRUs). IPMI can be used to monitor physical system health characteristics such as voltages, fan speeds, temperatures, and power supply status. It can also be used for automatic event notification and remote shutdown/restart. Together, these facilities give system engineers and administrators flexible, interoperable access to a broad range of platform information. This information simplifies system design by enabling TEMs to monitor, test, and diagnose systems at the blade level during the development phase. It also enhances availability by enabling IPMI technicians to isolate problems faster with a finer degree of granularity, thereby reducing Mean Time To Replacement (MTTR).

AdvancedMC provides optimal telecom mezzanine interface

AdvancedMC is a field-replaceable mezzanine interface that enhances AdvancedTCA flexibility by extending AdvancedTCA's high-bandwidth, multiprotocol interface to individual hot-swappable modules. The resulting fabric gives TEMs a versatile platform for building modular telecom systems that can be outsourced, designed, manufactured, stocked, and spared at lower cost. Modular AdvancedTCA/AdvancedMC fabrics also reduce operating costs by enabling service providers to scale, upgrade, provision, and service their systems with a finer degree of granularity. One example of an AdvancedMC module that allows communication equipment manufacturers to add modular and upgradeable compute functionality to their AdvancedTCA is Artesyn's KosaiPM (Figure 2). Adding such functionality supplied the localized horsepower necessary for applications such as:

- Protocol processing
- Packet processing
- Data management
- I/O management

Figure 2

AdvancedMC provides a high-speed, protocol-agnostic, serial packet interface with up to 21 I/O channels, each supporting data transfer rates of 10 Gbps per channel. AdvancedMC modules are hot swappable, enabling service providers to replace individual modules in the field without taking entire AdvancedTCA blades offline. They offer high power handling capability (currently up to 60 W per module), which enables TEMs to implement complex functions at the module level. And they provide an IPMI interface, which enables shelf management to monitor and control individual modules residing on AdvancedTCA blades.

AdvancedTCA carriers can be equipped with up to eight AdvancedMC modules, which currently come in four sizes:

- Half-height single-width
- Half-height double-width
- Full-height single-width
- Full-height double-width

The modules have escalating power limits of 20 W for the smallest module to currently 60 W for the largest module. This mechanical flexibility enables designers to partition their blades for maximum scalability, upgradeability, and field serviceability.

AdvancedTCA/AdvancedMC reduces carrier CAPEX and OPEX

AdvancedMC facilitates a Lego-like approach to AdvancedTCA blade design that greatly reduces time to market and cost. AdvancedMC eliminates the need to develop a custom blade for each application, enabling TEMs to create application-specific blades by combining a generic AdvancedTCA carrier with generic AdvancedMC components such as network interfaces, control processors, network/signal processors, and mass storage devices. Because the AdvancedTCA blade and modules are generic, they can be reused across multiple applications, thereby reducing design time and production cost. The generic nature of the blades and modules also makes them easier to outsource or purchase off-the-shelf, further reducing design time and cost.

Easier and less expensive to scale and updgrade, modular, field-replaceable AdvancedTCA/AdvancedMC systems help reduce equipment costs by enabling carriers to deploy the minimal hardware needed to service their subscriber base. The modularity of AdvancedTCA/AdvancedMC blades also reduces cost by reducing the number of unique blades and modules that TEMs have to purchase and stock. With AdvancedTCA/AdvancedMC, TEMs can stock a single generic carrier board that spans several products, along with the handful of generic I/O, mass storage, control, and signal processing modules needed to configure that carrier for specific applications.

Once they are deployed in the field, modular AdvancedTCA/AdvancedMC platforms also offer substantial opportunity for long-term Operational Expenditure (OPEX) savings. Because they are field replaceable, AdvancedTCA/AdvancedMC systems can tolerate failures to individual blades/modules with minimal disruption to overall service. Modular AdvancedTCA/AdvancedMC blades also reduce provisioning cost by enabling service providers to scale and provision their systems according to actual demand.

MicroTCA tackles small form factor applications

The same capabilities that make AdvancedMC attractive as a mezzanine architecture make it equally attractive as a blade-level specification for MicroTCA systems. Its hot swap capability enhances availability by enabling live systems to be serviced and upgraded in the field. Its large form factor and high power capability make it ideal for implementing complex functions. Its high-bandwidth, protocol-agnostic packet interface provides an ideal interconnect for linking multiple modules in a chassis. Its IPMI interface facilitates centralized, fine-grain monitoring and control. And its flexible form factor makes it possible to create mechanical MicroTCA chassis packaging options that are optimized for particular applications.

PICMG performed the first physical MicroTCA demonstration at SUPERCOMM 2005 using a 2U/300 mm/19-inch rack-based system equipped with four Artesyn Pentium M-based KosaiPM modules (Figure 3). The system simulated a wireless application servicing millions of subscribers. Final approval for the specification is expected in May 2006.

Figure 3

MicroTCA is in some respects a repackaging of modular AdvancedTCA/AdvancedMC blades for small form factor, cost-sensitive applications. AdvancedTCA's large form factor, though ideal for building high-density central office telecom infrastructure equipment, precludes its use in many outside plant and enterprise applications with tight size constraints. High cost also hampers the use of AdvancedTCA solutions in many outside plant, enterprise, and customer premises applications. AdvancedTCA carriers equipped with AdvancedMC modules have an added cost premium, as the carriers must be equipped with expensive card-cage-style connectors in order to house field-replaceable AdvancedMC modules.

MicroTCA reduces size and cost by eliminating the AdvancedTCA carrier and enabling AdvancedMC modules to be used directly in a variety of compact, low-cost enclosures, from standalone pico cells, to standard rack-mount systems. The OEM production price for a baseline MicroTCA system, including a MicroTCA chassis, switching hub, and power module, is projected to range from $1,500 to $2,000.

To accommodate a broad range of applications, MicroTCA is designed with scalability in mind. In addition to its scalable packaging and power options, MicroTCA provides scalable aggregate bandwidth from 1-650 Gbps, and scalable availability ranging from 3-nines (.999) to 5-nines (.99999).

MicroTCA's compact format, low cost, and low power consumption make it a perfect complement to AdvancedTCA for small form factor central office and outside-plant applications, including:

- Wireless base stations
- Digital loop carriers
- Optical ADMs
- Fiber to the Curb optical network units

Some also see a role for MicroTCA in enterprise networking applications such as workgroup routers, modular servers, and SAN storage boxes.

Virtual carrier environment

A MicroTCA enclosure acts as a virtual carrier, emulating the AdvancedTCA carrier environment. The virtual carrier provides the interconnect, power conversion, clock distribution, and system management functionality need to support up to 12 AdvancedMC modules. Some of this functionality may be implemented using components integrated as part of an active backplane. However the most cost-effective approach is to implement this functionality using a dedicated Virtual Carrier Management (VCM) module. Systems requiring high availability would deploy these VCM modules in redundant pairs in order to eliminate the VCM as a single point of failure.

The virtual carrier interconnect fabric provides the main connectivity among AdvancedMC modules in a MicroTCA enclosure. The VCM module acts as a dual-star hub, providing a central switch and high-speed lanes to each module. The half-duplex, serial lanes provide a scalable bandwidth ranging from 3.125 Gbps to 12.5 Gbps per channel, compatible with the data rates supported by individual AdvancedMC modules.

Versatile packaging options

The MicroTCA specification suggests a number of packaging options, but does not define one as part of the spec. The suggested 19-inch rack-mount MicroTCA chassis, for example, would range from 2U to 6U and measure just 300 mm deep (including cabling), a key requirement for many optical applications.

MicroTCA chassis can accept any standard AdvancedMC module, including half-height/single-wide, half-height/double-wide, full-height/single-wide and full-height/double-wide modules. Figure 4 shows a MicroTCA concept shelf. A typical high-availability shelf would combine redundant VCMs and power modules with up to 12 AdvancedMC modules. The chassis would take power from an AC main or traditional ±24, –48, or –60 VDC source, and convert it to 12 V for delivery to individual modules.

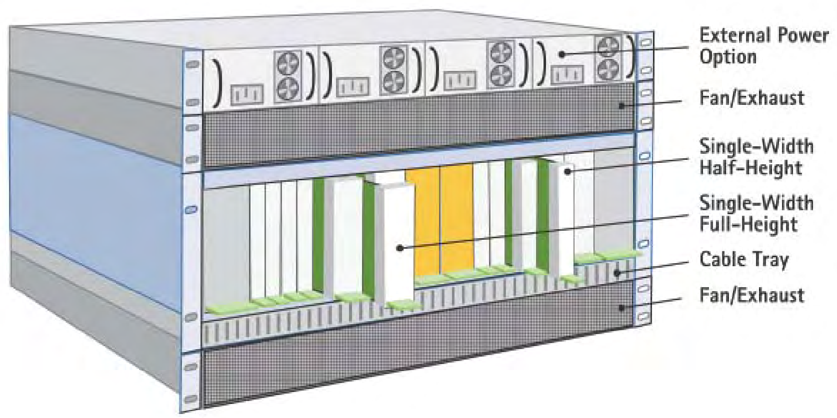
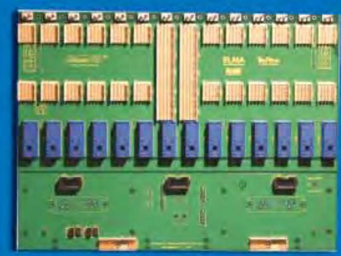


Figure 4



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To accommodate more irregular outside plant, pole-mounted environments, work is underway to make the MicroTCA chassis available in a cube configuration (Figure 5), which measures eight inches wide by eight inches high by 200 mm (roughly eight inches) deep. System designers can use cubes in a standalone mode or assemble them into two-dimensional arrays and install them in standard racks.

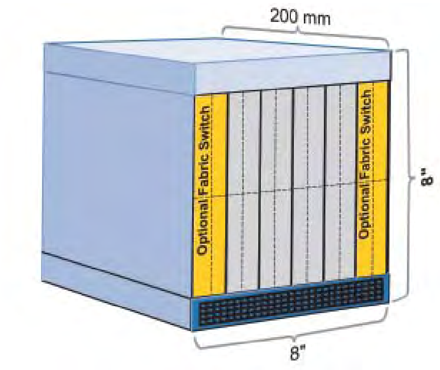

Figure 5

MicroTCA enclosures are not limited to standard shelves or cubes. These are popular options, but AdvancedMC's compact size enables MicroTCA enclosures to be used in a variety of space-constrained applications where only a few modules (pico assemblies) are needed to complete a system. Alternatively, MicroTCA enclosures can also be used to build large-capacity systems with hundreds of AdvancedMC modules.

MicroTCA's small size, low cost, field replaceablity, and scalable performance, coupled with its ability to utilize off-the-shelf AdvancedMC modules and AdvancedTCA/AdvancedMC infrastructure, make it an ideal platform for low- to mid-range telecom applications. Together with AdvancedTCA and AdvancedMC, MicroTCA provides an end-to-end framework that addresses the full spectrum of high-availability telecom applications, from core routers and WDMs to converged customer premises equipment.

Stuart Jamieson, *director of advanced technology with Artesyn Communication Products, has more than 15 years of experience developing embedded software, and has played a key role in the development of the technology central to Artesyn's bundled networking solutions.*

Stuart graduated from the Heriot-Watt University in 1989 with a first Class Honours degree in Electrical and Electronic Engineering and again in 1992 with an IBM-sponsored Master of Philosophy. He is currently the draft editor for the MicroTCA PICMG standard.

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AdvancedTCA: The effect beyond telecom

By Todd Etchieson

Telecom Equipment Manufacturers (TEMs) and service providersare realizing the benefits of incorporating standards-based, off-the-shelf components and systems into their designs. Improved time-to-market and economies of scale, reduced development costs, long life support, and a strong supply chain are benefits that could transfer to market segments including medical imaging, security appliances, industrial automation, and military applications. This article will outline issues faced by TEMs developing products for these segments and how AdvancedTCA can help.

In 2005 and 2006 many companies will conduct large-scale lab testing and in many cases begin commercial deployment, gearing up for broad deployment in subsequent years. Supporting this thinking are estimates from many sources that shipments of AdvancedTCA-compliant products could reach $60 million in 2006 and hit the $1 billion mark by 2009.

Some consider development of the standard, and availability of products, as further proof that the convergence of telecom and computing, which the industry has talked about for so many years, is finally happening. Designing the standard from the ground up has required TEMs and others involved in the process to do an incredible amount of heavy lifting.

Rigorous design and development schedules followed by painstaking testing have led to a variety of standard-compliant products being delivered today. In light of this, can companies developing products used in medical imaging equipment, security appliances, and military applications (among others) benefit from the pioneering efforts of the telecom industry? With the convergence clearly underway, the lines between computing and telecommunications products and applications have blurred. For example, today medical imaging equipment produces digital images, which are then uploaded to a computer and transmitted to a specialist for diagnosis. It is not a big leap to imagine this same process being done from a single machine (medical image, image processing, and communications). Are there other industries that could, or should, be part of the AdvancedTCA innovation wave?

A new revolution?

It's no surprise that if you modularize components – and standardize across modules – you end up with multiple vendors that provide compliant, interoperable solutions. AdvancedTCA could be compared to the PCI standardization that revolutionized the PC market. Companies such as IBM standardized on the PCI bus, and Microsoft followed suit with their plug-and-play drivers and interfaces. Today, users can use a variety of VGA cards from different vendors and be assured compatibility with their PCs.

AdvancedTCA defines the mechanics, interconnects, and management of implementing very highly compute- or I/O-intensive applications, or a blend of both. Equipment based on the architecture offers increased flexibility with an environment that allows expansion as needed. Developers can use a "mix-n-match" approach combining various functions, allowing a choice of best-of-breed components including chassis, blades, and Advanced Mezzanine Cards (AdvancedMCs). AdvancedMCs make modular multiprocessing possible by supporting modular computing features such as hot swap and board management, among others. And they can increase power and provide a broader range of high-bandwidth interconnect options.

Figure 1 shows an AdvancedTCA reference model that could be modified for a variety of applications at the platform level. For example, in military products the platform would include CPUs and data acquisition modules. For medical equipment, image processing and compute modules, and for telecommunications, the platform would include line cards, packet processing engines, and compute modules.

Capacity can be added to the platform during operation by adding or replacing existing hardware with more advanced, higher density blades. The form factor and variety of modular AdvancedMCs available today enables complete advanced applications on one card. Equipment manufacturers can use the same architecture to construct a variety of products, improving economies of scale.

From telemedicine to aerospace

Telemedicine can offer huge advantages, allowing medical professionals to quickly and accurately diagnose and treat serious conditions remotely. Today, high-quality images can be transmitted over networks, enabling real-time interaction between doctors in different locations. Doctors can address medical problems and treat patients more efficiently. Keeping up with technology advancement is a challenge, but by standardizing on AdvancedTCA, manufacturers could avoid a complete re-engineer of existing medical imaging equipment. With slight modifications to existing products, during manufacturing or in the field, equipment could be updated with the latest technology to accommodate advancements that meet users' evolving needs.

Enterprise security is another area where AdvancedTCA can have a positive impact. Network security appliances are growing in popularity. And whether they address an enterprise with a growing mobile workforce or one that incorporates government intelligence centers housing highly sensitive material, securing proprietary data is a challenge. Spam, hackers, viruses, worms, and packet sniffing keep IT managers awake at night. As security threats increase in speed, complexity, and volume, IT managers need to efficiently and cost effectively implement technology network wide. And, IT organizations are under extreme pressure to maximize the space these appliances need. Again, in an AdvancedTCA environment security appliances can easily be updated to address new, more complex security threats by simply adding or switching blades as needed. Its form factor allows blades to be installed horizontally,

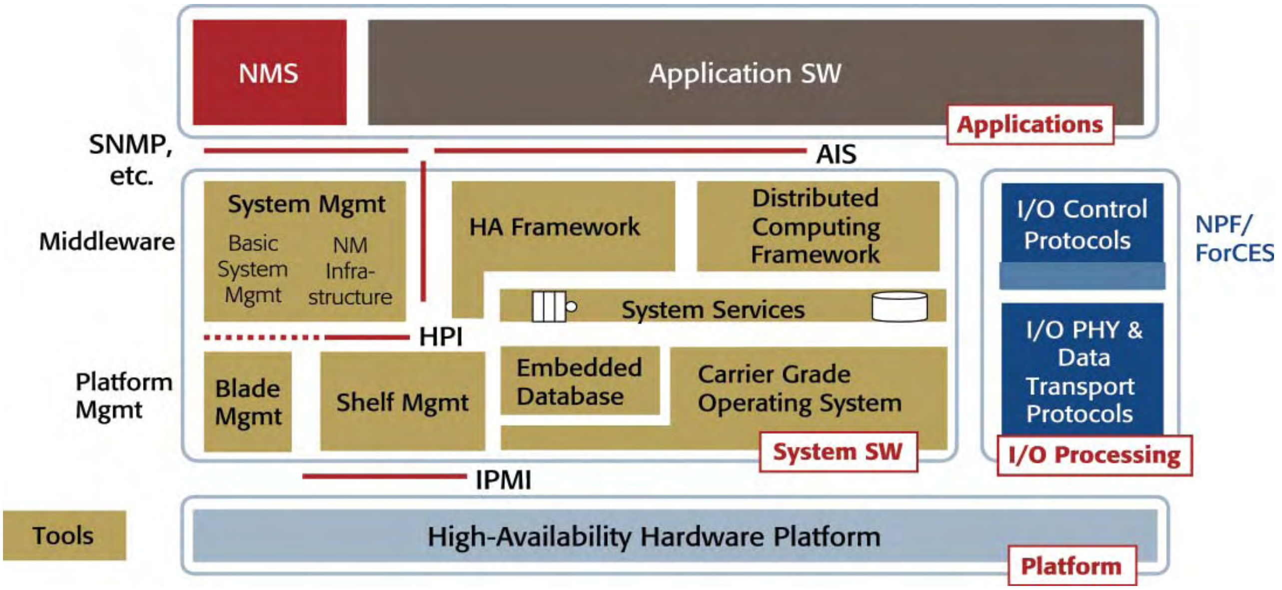

Figure 1

so that functionality that would typically reside in a 12U rack can fit into a 2U-4U configuration.

The military/aerospace market is a candidate for AdvancedTCA and would be a natural progression from VMEbus, the current standard used. While VMEbus has served the market well, there are limitations. The mil/aero world is known for producing rugged, reliable products that require significant processing power and are in the field for years. This long life cycle means this equipment needs to be easily upgradeable as processors and interconnect technologies evolve. AdvancedTCA can offer the same functionality the military/aerospace market has grown to love with VME, but also allows them to upgrade to next-generation technology as needed.

In each case, keeping up with ever-changing technology can test even the most advanced organizations. What is clear is that most market requirements are driving faster processors, communications, and lower prices.

Continuing forward with proprietary technology to meet these rapidly developing market requirements is no longer sustainable. Using proven, interoperable, off-the-shelf components from compliant vendors allows manufacturers to easily adapt products to changing requirements faster and more cost effectively.

Design teams working on next-generation computing products and applications should have a basic understanding of the benefits a common architecture for product development. Especially as the convergence continues, what operates as a standalone product today could become dependent on the network tomorrow.

Standards play an important role, ensuring interoperability and stimulating economies. Multivendor solutions also allow expansion into related markets enabling vendors to gain new customers and ultimately more revenue. For example, firms producing AdvancedTCA components and systems for the military/aerospace market may use this as a path into the medical equipment market.

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Where the rubber meets the road: AdvancedMC in AdvancedTCA – translating from standards to products

By Ian D. MacMillan

AdvancedTCA has rapidly emerged as the platform technology of choice for the delivery of innovative telecommunications infrastructure solutions. Standards enable delivery of high performance and high throughput solutions, as well as defined reliability and management architecture. The AdvancedTCA integration framework allows ease of mixing and matching functional modules, and has resulted in AdvancedTCA's adoption as the common platform framework for telecommunications equipment manufacturers to deliver advanced system solutions. AdvancedTCA is enabling developers to meet the global needs of 3G wireless and IP Multimedia Subsystems and to access broadband network deployment. AdvancedMC hot-swap capability has enabled AdvancedMCs to emerge as a key ingredient for the delivery of highly functional and robust systems. Ian discusses the status of the critical choices and issues systems developers should address as they look to deliver AdvancedTCA/AdvancedMC solutions.

Building useful telecommunications platforms for next generation networks requires a critical mass of AdvancedTCA and AdvancedMC building block products and capabilities. However, as with any new standard, issues need to be addressed in the development of new products, and AdvancedTCA and AdvancedMC are no exceptions. The standards provide a plethora of choices for implementation and design of the individual boards and modules. Hence, the system integrator has to clearly define the system architecture and the key interfaces in order to ensure ease of development and delivery of the solutions. In addition, the industry and vendors have recognized that ease of integration and interoperability is the key to enable further adoption of standards and market growth.

AdvancedMC building blocks for telecommunications

A typical AdvancedTCA platform will contain a number of base functions including the AdvancedTCA shelf, processor blades, switch blades, and element management. Depending on the capacity of a given system, these functions may be implemented in various ways, ranging from separate AdvancedTCA blades to a single set of redundant blades.

I/O interfaces and specialized components must populate the platform depending on the application. The key AdvancedMC building blocks required are:

- Telecom Interface processing modules
  - T1/E1/J1
  - OC-3/12
- Communications processing modules for channelized OC-3/DS3/T1/E1 interfaces
- Digital Signal Processor modules
- Network Processor modules
  - General purpose
  - Security flow through and coprocessors
- Gigabit Ethernet interface modules

AdvancedTCA allows the flexibility of deploying the AdvancedMC building blocks on multipurpose blades such as Single Board Computers (SBCs) or on carrier blades designed to support typically up to four AdvancedMCs. Other special purpose blades/AdvancedMCs would include disk drive AdvancedMCs for storage.

Taming the flexibility beast

The AdvancedMC building blocks and the flexible AdvancedTCA infrastructure allow for the development of highly reliable and highly functional network platforms. However, system designers face a number of choices in the actual AdvancedMC implementation:

- Port usage
- I/O options
- Form factor (such as full-height, half-height)
- Support for TDM (voice) and multimedia data
- Port density
- Front access versus rear access
- Support for APS and EPS

Port usage

The AdvancedMCs in each of the building block groups outlined previously have different requirements to complete their functions. The AdvancedMC dot specifications were created to define AdvancedMC port usage optimized to the different AdvancedMCs' functions. However, these AdvancedMC dot specifications make conflicting use of AdvancedMC ports.

AdvancedMCs provide 21 full-duplex high speed serial ports, three clocks, and other control, test, and power connections. The AMC.0 base specification (Figure 1) provides usage guidelines, but does not make firm assignments of the ports. AdvancedMC dot specifications assign specific uses to some of the ports:

- AMC.1 PCI Express and Advanced Switching
- AMC.2 Ethernet
- AMC.3 SATA and SAS
- AMC.4 Serial RapidIO

Each dot specification defines multiple legal configurations. The dot specifications necessarily make conflicting use of some ports.

As noted, AdvancedMCs may be used on AdvancedTCA processor blades, AdvancedMC carrier blades, and other host environments. No single AdvancedMC port usage model is optimal for all environments.

The carrier and the AdvancedMC must align in their use of the AdvancedMC ports. It is not economically viable to build multiple variants of the AdvancedMCs to support all the applicable options. This requires developers to select optimized AdvancedMC port usage models for processor blade and carrier card environments in the context of the overall system architecture. Figures 2 and 3 show some AdvancedMC port usage options.

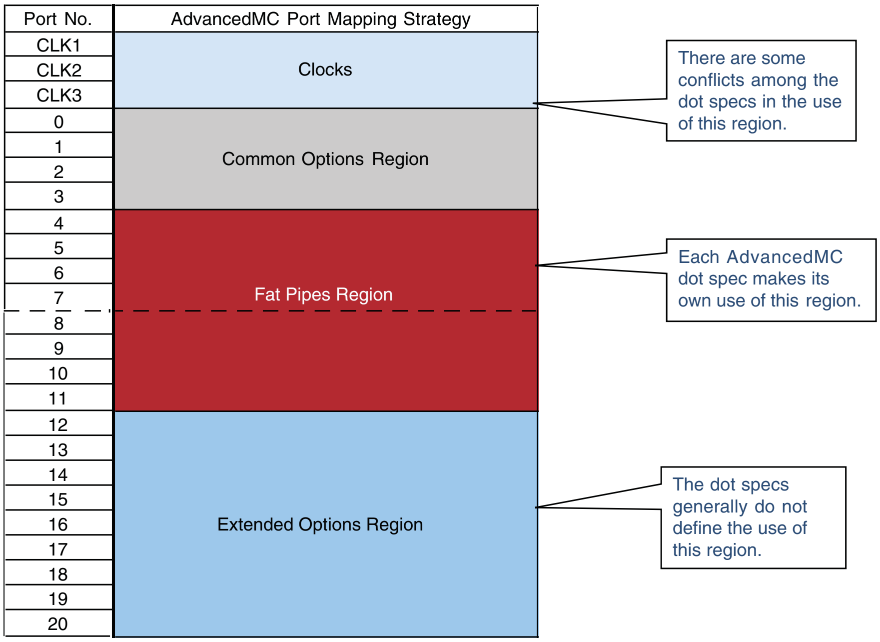

Figure 1

To further complicate the port usage issue, MicroTCA has some additional port configurations (Figure 4), which the AdvancedMC developers need to consider.

Internal I/O

The parallel I/O standards have reached their physical limitations and are viewed as not being capable of providing a reliable and cost-effective means for data rates greater than 1 gigabit per second (Gbps). Serial I/O appears to provide the path forward and has propagated waves of new serial interface standards development.

Serial system interfaces such as PCI Express, Advanced Switching, Serial RapidIO, InfiniBand, 1 Gb Ethernet, 10 Gb Ethernet XAUI (10 gigabit attachment unit interface), Fibre Channel, Serial ATA, SxI-5, and TFI-5 are all available today. AdvancedTCA and AdvancedMC in particular have support for PCI Express, 1 Gb Ethernet, 10 Gb Ethernet XAUI, Advanced Switching, and Serial RapidIO for internal communications.

Limits on the AdvancedMC form factor in terms of size and ports can make it difficult if not impossible to support more than one of these internal communications standards. Speculation continues on whether Ethernet will ultimately emerge as the preferred internal communications solution by adapting to meet the specific needs that drove the development of the other standards.

Form factor

The initial AdvancedMC specification defined half-height and full-height form factors. However, early products have shown issues with both form factors. It is possible that there may be a third height defined. In addition, with implementation experience and testing there are a number of changes being considered in the standards to add improvements to such elements as mechanical robustness and front panel design. The standards committees are paying careful attention to ensure that these changes have only an incremental impact on the many existing products to prevent any further delays in adoption of AdvancedMC solutions into end products.

Support for TDM

TDM voice is not going away. In March 2005, PICMG announced final ratification of the Internal TDM specification (PICMG SFP.1), also known as iTDM. See "Legacy telecom hits the 21st century: TDM circuits on AdvancedTCA switch fabrics" in the May, 2005 issue of this magazine for an extensive discussion of iTDM. Unfortunately, iTDM is not the only mechanism for transporting TDM in AdvancedTCA. Other options such as a proprietary TDM backplane using the undefined Zone 3 connectors or TDM over IP have also been suggested.

In addition, iTDM needs to address the larger system context. For example, if a redundant system is required, then are redundant Gig E links on AdvancedMC Ports 0 and 1 used, and how does the redundancy scheme work? iTDM itself defines a number of options that may make it more difficult to achieve interoperability. Given the continuing importance of TDM traffic, it's critical that the industry coalesces around a single standard such as iTDM and incorporates iTDM in the interoperability initiatives.

Port density

Gigabit Ethernet and optical interfaces can increase their capacity by simply moving to the next throughput level and the physical interface remains the same.

However T1/E1/J1 interfaces remain ubiquitous and must also be supported in AdvancedTCA platforms. The AdvancedMC, in particular, presents challenges with the front plates' limited real estate for connectors. As the capability of AdvancedMCs increases, the fan-in problem will be exacerbated.

The most common T1/E1/J1 connector is the RJ-45 style. It's possible to fit four RJ-45s on an AdvancedMC faceplate. Also the RJ-45 has sufficient pins to sup-

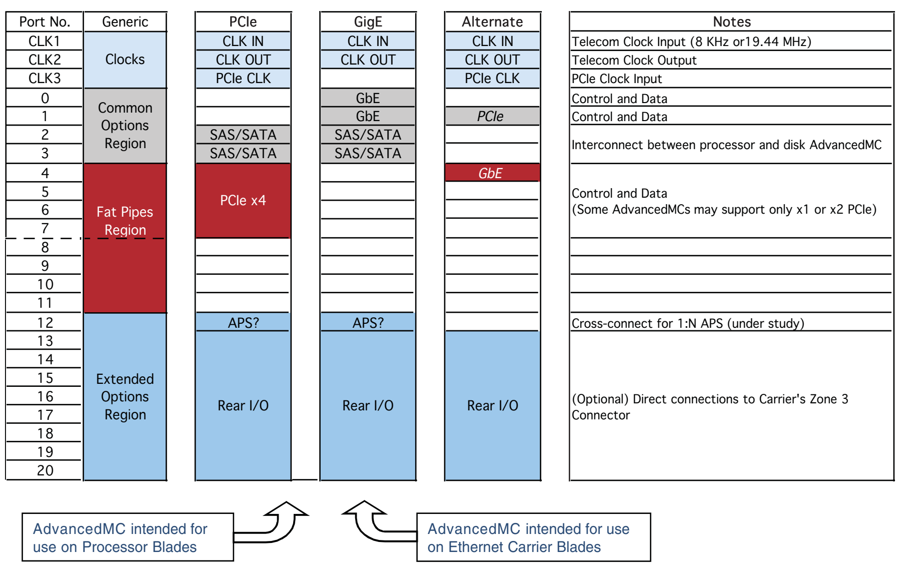

Figure 2

port two T1/E1/J1s, although this not a standard configuration. For signaling applications, this suffices. However, for media gateway applications, 16 and even 32 ports would be very desirable. Possible solutions include using a more dense front panel connector or using an RTM with more RJ-45 connectors.

The use of RTMs presents the challenge of passing RTM signals through an AdvancedTCA carrier (that is, the challenge of determining which ports are routed to the backplane). It's not clear if a standard solution will emerge. Hopefully the industry will adopt a de facto solution for this configuration.

Front access versus rear access

On systems with limited needs for port connectors, front access has been a common approach for many platforms such as CompactPCI. With optical interfaces, front access is the standard. The optical signal needs to be connected directly to the interface card, given there is no support in the standards for routing optical signals within the chassis.

However, with electrical interfaces and particularly T1/E1/J1 as noted earlier, rear access may be important in systems that have to support large numbers of ports. Alternatively, low-bandwidth signals could be muxed up in an external box in order to avoid the problem. Another approach is to use a dense connector on the front side and an external breakout panel.

Support for APS

Automatic Protection Switching (APS) is a requirement for many telecommunications network platforms. It is fairly easy to support APS on a single AdvancedTCA blade or AdvancedMC. However, to eliminate single points of failure, implementing APS over two cards helps.

AdvancedTCA and AdvancedMC standards don't address APS across cards. Therefore developers are creating their own solutions for APS. Where AdvancedMCs are used, the AdvancedMC carrier card must also support the APS solution.

Summary

AdvancedTCA and AdvancedMC products are rapidly coming to the market, representing telecommunications products' future. One clear sign of the progress that the industry is making is the identification of these types of interoperability issues as developers come closer to having real products based on AdvancedTCA and AdvancedMC.

Port No.	Generic	iNAV31K	Notes
CLK1	Clocks	CLK IN	Telecom Clock Input (8 KHz, 19.44 MHz TBD)
CLK2		CLK OUT	Telecom Clock Output
CLK3		PCIe CLK	PCIe Clock Input to AdvancedMC
0	Common Options Region	GbE	GigE connection to onboard switch
1		GbE	GigE connection to onboard switch
2		SAS/SATA	Interconnect between Bay B4 (PrAMC) and Bays B3, B2 (Disk AdvancedMC)
3		SAS/SATA	
4	Fat Pipes Region	PCIe x4	Optional PCIe x4
5			
6			
7			
8			
9			
10			
11			
12	Extended Options Region		
13		Rear I/O	Direct connections to Carrier's Optional Zone 3 Connector (Bays B1, B2, B3, B4)
14			
15			
16			
17			
18			
19			
20			

Figure 3

Port No.	Generic	MicroTCA	Notes
CLK1	Clocks	Clock In/Out	VCM 1/2 - Bussed Clock
CLK2		Clock In/Out	VCM 1/2 - Radial Clock
CLK3		Clock In/Out	VCM 1/2 - Bussed Clock
0	Common Options Region	GbE 0	VCM 1 - Fabric[A]
1		GbE 1	VCM 2 - Fabric[A]
2		SAS/SATA	SAS/SATA Host/Disk
3		SAS/SATA	SAS/SATA Host
4	Fat Pipes Region	Fabric	VCM 1 Fabric[D:G]
5			
6			
7			
8		Fabric	VCM 2 Fabric[D:G]
9			
10			
11			
12	Extended Options Region		Not Specified
13			
14			
15			
16			
17			
18			
19			
20			

Note: JTAG Interface is not shown

Figure 4

The challenge is to achieve consensus around the solutions to these issues as quickly as possible. Every new telecommunications standard has resulted in the creation of an industry forum focused on making the standard useful by driving common applications and interoperability. Look for the same to happen with AdvancedTCA and AdvancedMC.

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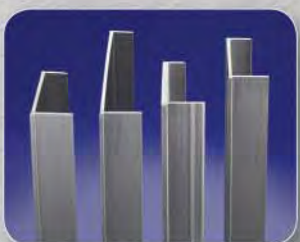

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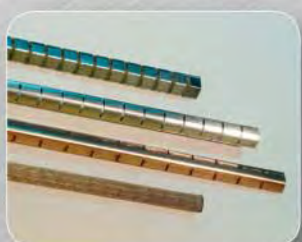

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