TELECOM S/W CRUNCH ... IMS ... LIQUID COOLING

CompactPCI® and AdvancedTCA® Systems

The Magazine for Developers of Open Communication, Industrial, and Rugged Systems
www.CompactPCI-Systems.com • www.AdvancedTCA-Systems.com

OCTOBER 2006 VOLUME 10 NUMBER 8

Real-world MicroTCA

Product Guide
MicroTCA

SPECIAL
INCLUDED WITH THIS ISSUE:
RadiSys
Product and Application Guide
Fall 2006

Advancing the Power of Embedded Computing

Emerson Network Power's new Embedded Computing business is anchored by recently acquired Artesyn Communication Products. It enhances Emerson's global capabilities to offer more comprehensive, highly integrated and reliable platform solutions.

Artesyn Communication Products' rebranding as Emerson Network Power's Embedded Computing business builds on the company's innovative work in the open architecture telecom platform industry. The formation makes it possible for telecom equipment manufacturers (TEMs) and network equipment providers (NEPs) to reduce their development cost and time to market.

The new business will offer telecom components, blades, software and systems to equipment markets in a broad range of telecom infrastructure applications, including network access, soft switches, signaling systems, and media gateways. These products, based on industry standards make it easier for TEMs and NEPs to outsource their platform design and focus precious engineering resources on value-added applications and services.

Just another reason why Emerson Network Power is the global leader in enabling Business-Critical Continuity™.

- AC Power Systems
- Connectivity
- DC Power Systems
- **Embedded Computing**
- Embedded Power
- Integrated Cabinet Solutions
- Outside Plant
- Power Switching & Controls
- Precision Cooling
- Services
- Site Monitoring
- Surge & Signal Protection

US Toll Free: 1-800-356-9602 ▪ Voice: +1-608-831-5500

www.artesyncp.com

EMERSON™ Network Power

Formerly Artesyn Technologies

EMERSON. CONSIDER IT SOLVED™

RSC# 3 @ www.compactpci-systems.com/rsc

CompactPCI® and AdvancedTCA® Systems

VOLUME 10 • NUMBER 8
OCTOBER 2006

www.compactpci-systems.com
www.advancedtca-systems.com

The Magazine for Developers of Open Communication, Industrial, and Rugged Systems

COLUMNS

EVENTS

AdvancedTCA Summit
October 17-19
Santa Clara, CA
www.advancedtcasummit.com

SDR Forum Technical Conference
November 13-17
Orlando, FL
www.sdrforum.org

COVER:
A general purpose computing and software development platform, a WiMAX basestation, a 3G/4G basestation, and a quadruple/triple play IP Multimedia System (IMS) platform are among the working MicroTCA systems CorEdge Networks is developing, with particular attention to clock and fabric interaction. See page 38.

MicroTCA Carrier Hub (MCH) photo courtesy CorEdge Networks.

Published by: OpenSystems Publishing™

FEATURES

E-LETTER

October: www.compactpci-systems.com/eletter
MicroTCA: Modular and scalable
By Volker Haag, Schroff

November: www.compactpci-systems.com/eletter
A top-down perspective of IMS, AdvancedTCA, and blade servers
By George Kontopidis, NMS Communications

WEB RESOURCES

Subscribe to the magazine or E-letter at:
www.opensystems-publishing.com/subscriptions

Industry news:
Read: www.compactpci-systems.com/news
Submit: www.opensystems-publishing.com/news/submit

Submit new products at:
www.opensystems-publishing.com/vendors/submissions/np

OpenSystems Publishing

Advertising/Business Office

30233 Jefferson Avenue
St. Clair Shores, MI 48082
Tel: 586-415-6500 ■ Fax: 586-415-4882

Vice President Marketing & Sales
Patrick Hopper
phopper@opensystems-publishing.com

Business Manager
Karen Layman

Sales Group

Dennis Doyle
Senior Account Manager
ddoyle@opensystems-publishing.com

Tom Varcie
Account Manager
tvarcie@opensystems-publishing.com

Doug Cordier
Account Manager
dcordier@opensystems-publishing.com

Barbara Quinlan
Account Manager
bquinlan@opensystems-publishing.com

Andrea Stabile
Advertising/Marketing Coordinator
astabile@opensystems-publishing.com

Christine Long
E-marketing Manager
clong@opensystems-publishing.com

Regional Sales

Jane Hayward
Regional Manager – California
jhayward@opensystems-publishing.com

Phil Arndt
Regional Manager – East Coast
parndt@opensystems-publishing.com

Richard Ayer
Regional Manager – West Coast
rayer@opensystems-publishing.com

International Sales

Stefan Baginski
European Bureau Chief
sbaginski@opensystems-publishing.com

Dan Aronovic
Account Manager – Israel
daronovic@opensystems-publishing.com

Reprints and PDFs

Call the sales office: 586-415-6500

CompactPCI® and AdvancedTCA® Systems

AN OPENSYSTEMS PUBLICATION

Communications Group

- CompactPCI and AdvancedTCA Systems
- CompactPCI and AdvancedTCA Resource Guide
- CompactPCI and AdvancedTCA E-letter

Editorial Director Joe Pavlat
jpavlat@opensystems-publishing.com

Assistant Managing Editor Anne Fisher
afisher@opensystems-publishing.com

Senior Editor (columns) Terri Thorson
tthorson@opensystems-publishing.com

Technology Editor Curt Schwaderer
cschwaderer@opensystems-publishing.com

Associate Editor Jennifer Hesse
jhesse@opensystems-publishing.com

European Representative Hermann Strass
hstrass@opensystems-publishing.com

Art Director Steph Sweet

Senior Web Developer Konrad Witte

Graphic Specialist David Diomede

Circulation/Office Manager Phyllis Thompson
subscriptions@opensystems-publishing.com

OpenSystems Publishing

Editorial/Production office:
16872 E. Ave of the Fountains, Ste 203
Fountain Hills, AZ 85268
Tel: 480-967-5581 ■ Fax: 480-837-6466
Website: www.opensystems-publishing.com

Publishers John Black, Michael Hopper, Wayne Kristoff

Vice President Editorial Rosemary Kristoff

Embedded and Test & Analysis Group

Editorial Director Jerry Gipper
Editorial Director Don Dingee
Technical Editor Chad Lumsden
Associate Editor Jennifer Hesse
Special Projects Editor Bob Stasonis
European Representative Hermann Strass

Military & Aerospace Group

Group Editorial Director Chris Ciufo
Assistant Editor Sharon Schnakenburg
Senior Editor (columns) Terri Thorson
European Representative Hermann Strass
European Bureau Chief Stefan Baginski

CompactPCI and AdvancedTCA Systems (USPS 019-288) is published nine times a year (Jan, Feb/March, April, May, June, July/Aug, Sept, Oct, Nov/Dec) by OpenSystems Publishing LLC, 30233 Jefferson Avenue, St. Clair Shores, MI 48082. Print ISSN 1098-7622, Online ISSN 1550-0381. *CompactPCI and AdvancedTCA Systems* is free to qualified engineers or management dealing with or considering open system technologies. For others, paid subscription rates inside the US and Canada are $63/year. For first class delivery outside the US and Canada, subscriptions are $90/year (advance payment in US funds required).

Periodicals postage paid at St. Clair Shores, MI, and at additional mailing offices. Canada: Publication agreement #40048627. Return undeliverable Canadian addresses to: WDS, Station A, PO Box 54, Windsor, ON N9A 615.

POSTMASTER: Send address changes to *CompactPCI and AdvancedTCA Systems* 16872 E. Ave of the Fountains, Ste 203, Fountain Hills, AZ 85268

AdvancedTCA | CompactPCI | PCI/ISA | Small Form Factor | Custom Design

AdvancedTCA®

ATCA Blades

Nodes and Hubs

ATS0020

ATS1160

ATS2148

- Daughter Board Free Fabric Options
  - Better NEBS Vibration Characteristics
  - Better Fabric Eyes
  - Better Thermals
  - Lower Cost
- Modular Ethernet Management Software
  - Free From Open Source Issues
  - Clear Path to IPV6
- Design History
  - NEBS Compliant designs since 80486
  - Anechoic Chamber, Vibration and Thermal Prescreen On Site
- Third Generation of ATCA Switch Blades
- Committed to Interoperability

Diversified Technology® An Ergon Co.

Over Three Decades of Embedded Solutions

intel Communications Alliance Associate | CP-TA Interop Delivered 3.0 Certified, Communications Platforms Trade Association | SCOPE | PICMG | Member VITA Open Standards, Open Markets | BSI Registered ISO 9001:2000 FM 65275

1.800.443.2667 • sales@dtims.com • http://www.diversifiedtechnology.com

RSC# 7 @ www.compactpci-systems.com/rsc

By Joe Pavlat

The universe is expanding

The universe of new platform standards for communications and telecom applications continues to grow in depth and breadth. This issue digs deeply into a variety of related topics. Certainly one of the most discussed topics of late is MicroTCA, and here you'll find insiders' perspectives on this new standard, ratified by PICMG in July.

Work on the first open architecture specifically designed for demanding high performance telecom applications, AdvancedTCA, began in 2001. More than 100 PICMG member companies participated, and the standard was ratified at the end of 2002. Next came the challenge to maximize AdvancedTCA flexibility and modularity. A new hot pluggable, managed, fabric-based mezzanine card would be needed, the Advanced Mezzanine Card. Ratified in early 2005, the AdvancedMC specification quickly generated momentum. As many as eight AdvancedMCs can plug onto an AdvancedTCA carrier card, allowing system designers and integrators to easily customize a common base platform configuration. AdvancedMC cards are very powerful, and it wasn't long before system architects began to think about plugging them directly onto a backplane in a small chassis. Doing so would create a physically small, low cost platform with very high performance and scalability. And so MicroTCA was born.

Contributors

Stuart Jamieson of Emerson Network Power provides an excellent introduction to the MicroTCA architecture and its applications. Stuart is a true expert on MicroTCA, as he served as document editor during the specification development. Stuart and his colleagues also provided significant technical contributions and guidance to the standard.

Volker Haag from Schroff provides additional details about MicroTCA in this month's E-letter (www.compactpci-systems.com/eletter). Schroff was also a key player in the development of MicroTCA.

Will Chu of CorEdge Networks explains that by intelligently pairing specific types of AdvancedMCs with MicroTCA Carrier Hubs (MCHs) that support specific networking protocols and clock types, developers can leverage the MicroTCA platform to deploy a wide array of applications.

Lest one think that MicroTCA is just for telecom applications, Rob Persons from Motorola shows us how MicroTCA is being applied to modern military applications. The shift towards the integrated battlefield and *net-centric* warfare has created a need for the same high performance, IP-based systems that are typical of the telecom world. It is expected that PICMG will begin work to formalize a military version of MicroTCA later this year.

In the September issue of *CompactPCI and AdvancedTCA Systems*, the work being done by the Liquid-Cooled Embedded Computing (LCEC) initiative was introduced; in a follow-on article, which begins in this issue and is available in full at www.advancedtca-systems.com, the LCEC's two-pronged development approach of a Static Display Model and a prototype system, developed under a Defense Microelectronics Activity (DMEA) program, is detailed.

Time Division Multiplexing, or TDM, has been the basis of digital voice transmission and handling for a long time. In the new world of IP-based communications, a method is needed to support legacy TDM data over IP networks. Internal TDM (I-TDM) is a new standard developed by PICMG to support TDM traffic on platforms such as AdvancedTCA and MicroTCA. Three industry experts, Robbie Dhillon, Ian MacMillan, and Amir Zmora team to provide us with a tutorial about I-TDM, how it works, and how it is applied.

Venkataraman Prasannan from RadiSys also explores issues of handling voice over the new networks. He describes how AdvancedTCA and MicroTCA can be used to handle Voice over IP traffic.

Michael Christofferson from Enea explains how software development costs exceed those of hardware these days, and the rapid expansion of code isn't being matched by a commensurate increase in the number of programmers. He explains how open architectures in both hardware and software help address this problem, and introduces us to Device Software Optimization, or DSO.

"The shift towards the integrated battlefield and net-centric warfare has created a need for the same high performance, IP-based systems that are typical of the telecom world."

Also addressing the topic of new software development methods, Curt Schwaderer writes in the *Software Corner* about a new concept called Model Driven Development. Curt takes us through high-level concepts and explains how they fit together to create a new software development environment.

Things have been very busy at PICMG lately, and PICMG's Rob Davidson gives us an update on what the organization has been up to of late, which includes ongoing updates and enhancements to existing specifications, as well as new initiatives.

This issue is an essential one for catching up on a quickly expanding universe as we wind up the year. Read on!

Joe Pavlat

Editorial Director

ETXexpress Module with Intel® Pentium® M and Mobile Intel® 915GM Express Chipset

As the first member of the ADLINK ETXexpress family, the ETXexpress-IA533 uses low power Intel® Pentium® M processor 760 at 2.0GHz and the Mobile Intel® 915GM Express Chipset. Both the processor and chipset are part of the embedded Intel® Architecture that ensures a long production life for applications that need extended availability. The ETXexpress-IA533 supports dual channel DDR2 533MHz memory and comes with a single on-board Gigabit Ethernet port. In addition to the on-board integrated graphics, a Graphic PCI Express x16 slot is also available. The board connects up to four additional PCI Express x1 devices. The module has legacy support for 32-bit PCI and ISA through LPC.

For more info, go to:
www.adlinktech.com/products

Full-size Intel® Pentium® 4 (LGA775) Processor SBC

The new NuPRO-851DV has a high-computing capability. It supports an 800MHz FSB and Intel® Pentium® 4 (LGA775) processor with Hyper-Threading technology. It has a large communication bandwidth with two PCI Express x1 Gigabit Ethernet ports. It supports Serial ATA for high-speed storage, USB 2.0 and other generic features including VGA, COM, keyboard, mouse and hardware monitoring.

For more info, go to:
www.adlinktech.com/products

A Compact Multi-Application Computer with New CPU Options, and the Latest Chipset

The GEME-4000 offers multiple CPU choices and USB 2.0 connectors, LVDS support for display and DDR RAM in addition to the standard GEME features. The GEME-4000 comes with an Intel® Ultra Low Voltage Celeron® M 600MHz processor. They can be controlled from remote locations and run continuously in many critical applications such as machine tools and digital video capture. It also comes equipped with anti-vibration features.

For more info, go to:
www.adlinktech.com/products

High-Performance 3U CompactPCI Intel® Pentium® M / Intel® Celeron® M Processor SBC with Dual GbE on PCI Express

The cPCI-3915 CPU board is a 3U 4HP or 8HP system slot single-board computer with up to 2.0GHz for the Intel® Pentium® M CPU. This SBC is based on the Intel® 915GM chipset with 400 or 533 MHz FSB. One SO-DIMM socket carries up to 1GB 400/533 MHz non-ECC DDR2 RAM. The cPCI-3915 offers two Gigabit Ethernet ports, two RS-232 ports, one IDE ATA 100/66/33 port, one CompactFlash socket, two SATA-150 interfaces, quad USB 2.0, and a VGA/DVI interface. The Ethernet ports support PXE remote boot.

For more info, go to:
www.adlinktech.com/products

Choose From A Complete Line of AdvancedTCA Products

Two AdvancedTCA Processor Blades with Dual Intel® Xeon 800FSB

- PICMG 3.4 ATCA Advanced Switching Option3
- Quad ASI x4 Fabric Interface Channels up to 5-Slot Full-Mesh Configuration, 32Gbps
- Dual Intel® 64-bit LV-Xeon 2.8GHz, 1MB L2 Cache, Hyper-Threading Processors
- Dual DDR2-400 REG/ECC Channels with 16GB max.

AdvancedTCA Base/Fabric Switch Blade with 10GbE Uplink Port

- 24-Port 10/100/1000BASE-T Base Interface: 12 Node-Slot, 8 Egress, 2 ShMC Ports, 1 Inter-Switch and 1 Control Plane Port
- 24-Port 1000BASE-BX Fabric Interface: 14 Node-Slot, PICMG 3.0 Option1 Ports, 2 Egress and 8 RTM Ports
- Layer 2/3 Packet Switching and Routing
- Vitesse® VSC7310 GbE Switch-on-a-chip

5U Five-Slot AdvancedTCA Rackmount System

- 19" Rackmount, 15.3" Depth
- Five-Slot Full Mesh Topology Fabric Interface
- Five-Slot Standard Rear Transition Module
- Dual Bussed IPMB

Call us toll-free at (866) 4-ADLINK
or email info@adlinktech.com

PCI INDUSTRIAL PICMG COMPUTERS

intel Communications Alliance Associate

ADLINK TECHNOLOGY INC.
www.adlinktech.com

By Curt Schwaderer

Pioneering model driven development

Since software and systems engineering has been around, so too has systems and software modeling. Modeling delivers benefits that include proving out the system prior to detailed design and implementation so that errors can be detected and eliminated earlier in the development cycle.

Witnessing the operational aspects of system requirements is also beneficial. Modeling provides a proof-of-concept that saves time and money during the development cycle by facilitating the collective agreement of all stakeholders pertaining to the requirements and functional operation of the system.

However, modeling has historically been disjoint from the development cycle. Often the model is discarded once the concept has been proven, as was the situation with CASE tools in the 1990s, and development begins from scratch. This chasm between modeling and the development process leads to design flaws and an implementation that does not behave according to the original model. For many years developers have been striving to make the model a more integral and iterative part of the process. This approach would enable the model to serve as the design and implementation starting point for the development. What's more, the model could be evolved as the development proceeds. In this column, we will explore a development approach called Model Driven Development or MDD. The evolution of MDD has been going on for some time, but recent modeling and development tool innovations are making MDD a viable approach to software and systems engineering.

Proliferating MDD throughout the embedded space

PrismTech, a company whose core competency has historically been software tools and middleware, believes now is the time to make MDD a reality. The company embraces the proliferation of MDD throughout the embedded systems space. PrismTech sees MDD as useful for enterprise, net-centric, and mission-critical applications. They have successfully used the approach to develop real-world embedded software products. (At www.prismtech.com a comprehensive white paper is available that covers the details of the MDD approach.)

What is model driven development?

MDD is a development practice where high-level, agile, and iterative software models (often domain-specific) are created and evolved as software design and implementation takes place. The key defining characteristic of MDD is that the model literally becomes part of the development process. Contrast this with an approach such as the waterfall development process where modeling appears as a separate step in the process and tends to get left behind once the development proceeds to the next phase.

Work in defining model driven development best practice is ongoing by various industry groups, including the Object Management Group (OMG), an organization of end users and software vendors for developing industry standards for the software life cycle. The idea behind MDD is to model an application and use a single repository where the high-level model of that application (and its systems environment) is maintained. This enables non-software-engineering stakeholders (for example systems designers and engineers) to maintain control (well past the initial modeling stage) of requirements and functionality for the system during development. Thus, MDD allows business and technical personnel to help define and maintain the model in a very real and meaningful way, resulting in systems and applications that more accurately satisfy requirements on initial deployment.

MDD's component architecture together with automatic code generation (latter-day interpreters between the model and the source and unit test code) and high-performance, low-overhead middleware meet the needs of networked enterprise and embedded systems where application functionality is distributed among network nodes.

As a result, MDD is highly compatible with publish/subscriber middleware, such as Data Distribution Service (DDS) and distributed object middleware such as CORBA.

MDD hurdles

Software and system modeling has been around for many years. Typically the modeling occurs at the proof-of-concept stage using third generation languages such as C/C++ or Java. Universal Modeling Language (UML) tools have been refined over time. Use of UML has spanned anywhere from modeling to being used to develop designs. However, until this point, UML has historically lacked semantics to describe the system at the business or embedded application level. Work must be done to define the application within its domain, with a separate step required to translate that description to UML. Software frameworks, libraries, and software components available on the Web in open source form have also been used for modeling.

The biggest obstacle to achieving MDD with these traditional tools and components is *domain specificity*. Application stakeholders need to describe the system requirements and functionality in the domain of that system, including:

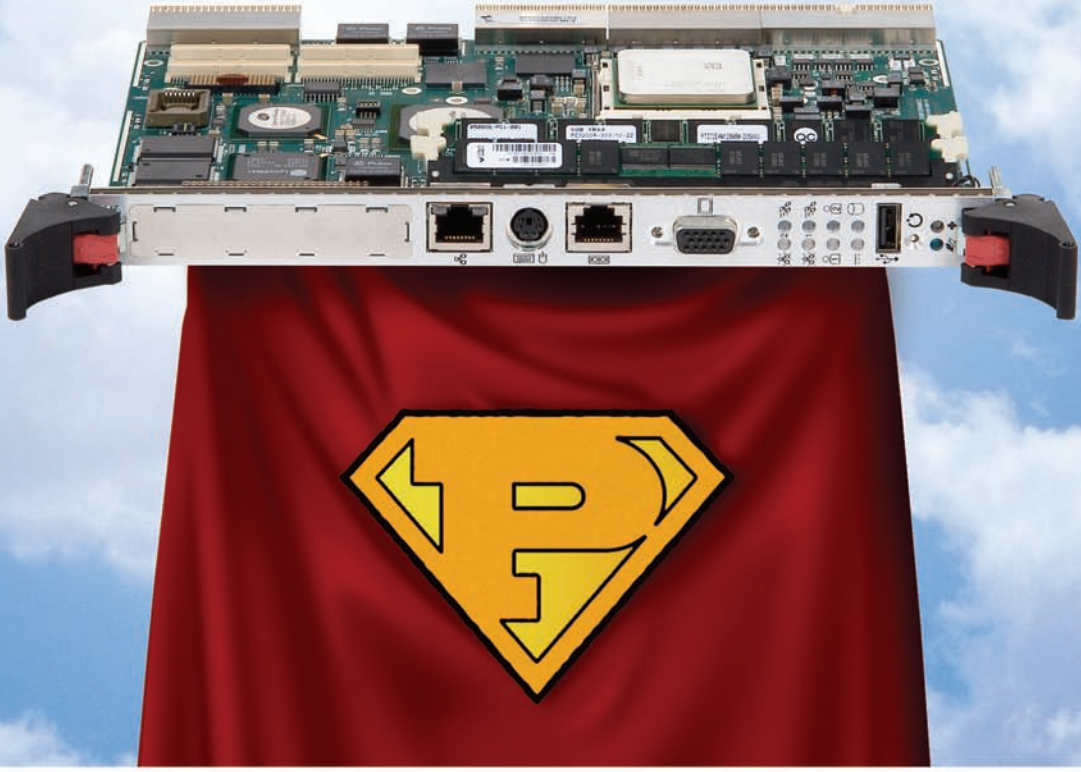
- Information that the system keeps
- Behavior of the components in the system
- Availability of the information to those components

The semantics of UML or third generation languages such as XML, C/C++, and Java, should not limit these descriptions. Nothing is worse than to have an experienced stakeholder in the domain unable to express to the engineering team important aspects of the system because the programming language puts up obstacles.

A chasm

So, there is a chasm that exists between the architecture created by the domain experts and third generation languages, tools, frameworks, and other components used to implement it. In this chasm, domain specific requirements decouple from the technical design and implementation of

A Compute Blade This Powerful Deserves A Cape.



The CPC5564 64-Bit AMD Opteron™ Single Board Computer

AMD 64 Opteron

The CPC5564 is the world's most powerful PICMG® 2.16 compute blade, and the first to be based on single- and dual-core AMD Opteron™ processors. The AMD Opteron™ processor provides a highly scalable x86 architecture that delivers next-generation performance as well as a flexible upgrade path from 32- to 64-bit computing. Its multi-core architecture offers advanced processing speed while reducing heat and power consumption.

With up to 8GB of ECC memory, multiple storage options and Linux, Solaris™ and Windows® operating system support, the CPC5564 is an ideal computer for high-end packet processing or multi-threaded software environments found in wireless, softswitch and defense applications.

Is it the superhero of the compute world? We like to think so.

PERFORMANCE TECHNOLOGIES

CELEBRATING 25 YEARS PERFORMANCE TECHNOLOGIES

Learn more at:
www.pt.com/sbc2

the system. This decoupling can lead to derailment of the project if a system does not function as intended.

MDD bridges this chasm using Domain Specific Modeling Language (DSML). Those familiar with the Eclipse Modeling environment will recognize that DSML brings high-level engineering/modeling work and low-level implementation programming together as two well-integrated parts of the same job.

The benefits of the MDD approach are numerous. There is a significant increase in cross discipline collaboration. The existence of the DSML means nontechnical and technical participants all speak the same language without getting into technical programming details that may cause miscommunication or errors in interpretation of the system requirements. Learning curves associated with this approach involve understanding of the domain specific terminology, not details behind programming languages and tools.

Model driven development and domain specific languages

So, how is model driven development done? First, a DSML must be defined for the application, forming a foundation for communication among all stakeholders. Next, a domain specific editor captures requirements and high-level operation of the system. Finally, transformation engines that take the output of the domain specific editor and generate source and/or link to functional components that can be built into the system executable complete the model driven development environment.

Using model driven development, modeling and programming activities blend into the same development process. The models become direct input into the development process, not just an aid to design activity. Domain specific models are developed to be machine processed for integration with implementation generators. Further, implementation of the model is done from the design perspective, not according to third generation language semantics.

PrismTech is using tools and middleware that implement DDS concepts and processes in its OpenSplice product family (Figure 1). OpenSplice is targeted to aid in the development of domain specific languages. It also allows for generators that transform the domain specific model into executable software for a specific enterprise or embedded platform or product family. Table 1 describes the steps involved in model driven development.

Each of the steps for model driven development is accounted for in the OpenSplice product line. Using OpenSplice, the model produces a collection of development artifacts that are used to generate the implementation.

A Software-Defined Radio using MDD

PrismTech has developed a Software-Defined Radio (SDR) product using MDD and the DDS tools. To drive home the impact of MDD, we will overview some of the key points of the PrismTech SDR product so you can have a look at MDD in action.

Like many other areas, radio technology is moving from custom hardware systems to general purpose platforms with software that implements the functionality of the radio. This enables radio systems to become easier to maintain, lengthens the deployment life cycle, and reuses or enhances existing software algorithms.

Development of SDR starts with the Software Communications Architecture (SCA). SCA is an SDR model created in 1999 by a consortium of leading military radio developers. SCA isolates abstractions and describes how they work together within the domain of an SDR.

The next step is to create a formalized grammar, or Domain Specific Language (DSL). Most SCA implementations use third generation languages applied directly from the SCA specification. The PrismTech approach raises the level of abstraction to define formalized meta-model components that are expressed in terms of a language workbench, specifically, the Eclipse Modeling Framework.

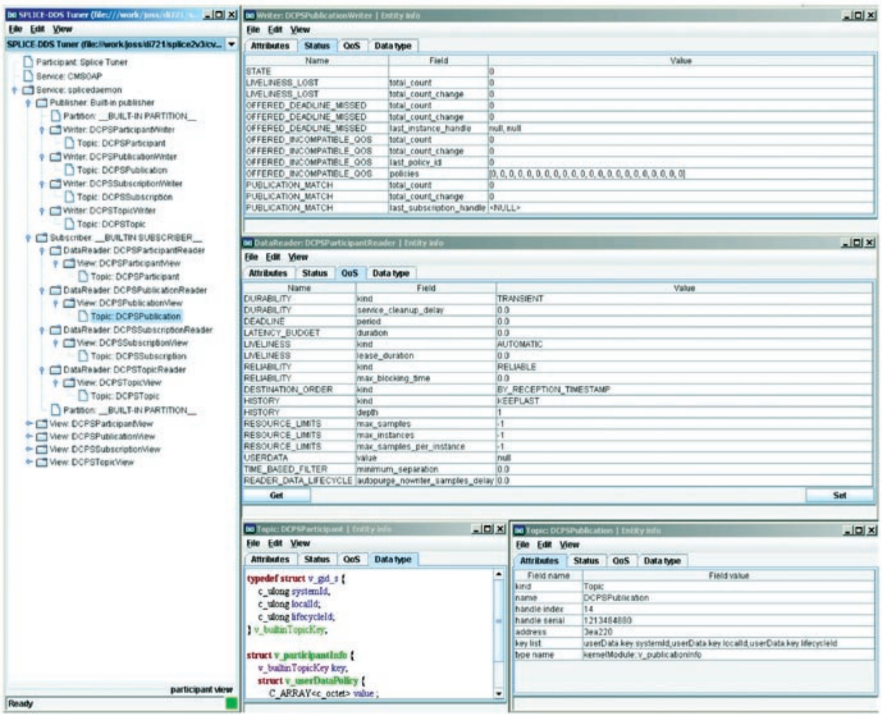


Figure 1

General MDD Methodology	PrismTech OpenSplice Process
Isolate the abstractions and how they work together	The Data Distribution Service Specification
Create a formalized grammar for these – DSL	Create a formalized DSS *meta-model*
Create a graphical representation of the grammar – DSGL	Create a DDS-specific graphical tool
Provide domain specific constraints – DSGL, DSCL	Program the constraints into the tool
Attach generators for necessary transformations	C/C++ and Java generators

Table 1

Once the DSL is completed, a meta-model for SCA is specified. The meta-model is the key ingredient that allows end users with knowledge in the domain to specify what they want to have, not how it is done. The meta-model also allows the end user to directly affect model implementation.

Next, a graphical description of the grammar is created, called Domain Specific Graphical Language (DSGL) and Domain Specific Views (DSV). The PrismTech Spectra SDR PowerTool modeling environment allows the end user to define functional components and connect them together to specify processing characteristics. All of this is done using the DSL.

The language workbench's programming facilities implement, within the domain specific graphical language, the Domain Specific Constraint Language (DSCL). So, the programming within the language workbench includes a structural framework for the rules of the domain. When end users develop their components and systems, the constraint language ensures that they are conforming to the domain requirements. The constraint language is an important part of maintaining the correctness of the model and requires domain experience.

Ultimately, the DSL is transformed into an executable format. This occurs through Domain Specific Generators (DSG). For embedded systems, PrismTech notes these generators may have multiple targets on the platform, including FPGAs, general purpose processors, or digital signal processors. As a result, the DSGL tool needs to be able to iterate over the model, interacting with multiple domain specific code generators to produce multiple types of executable code.

PrismTech's OpenSplice DGSL tool can declare a component in the SDR domain. This tool can also create software artifacts from the DSGs, keep code coverage information, and keep test case generation information for the components within the model. I was impressed by his tool chains' ability to bridge the gap between a graphical model component and its VHDL description to C source code with test case and code coverage information.

PrismTech notes a number of advantages of the OpenSplice MDD paradigm in the modeling and development of SDR versus using third generation languages. Domain experts can be far more productive in the MDD environment due to the abstraction. The domain specific generators provide a high level of correctness with pre-validated logic and the software artifacts derived directly from the model. The SCA architecture is captured in the PrismTech meta-model, lowering the cost of entry significantly for companies wishing to move to SDR. With the MDD paradigm, it's possible to determine defects in the system at modeling time rather than during system integration. This approach helps achieve architectural consistency across the model and implementation.

Conclusion

This SDR example covers specifics in the SDR domain. However, the MDD process has more far-reaching implications than one example in one domain. The OpenSplice MDD/DSS environment is capable of extending model driven development into a number of areas. Systems and software continue to become increasingly complex. Now more than ever, it's important to leverage domain expertise into the heart of the development process. Model driven development and products make this transition possible in an efficient and effective way.

For more information, contact Curt at cschwaderer@opensystems-publishing.com.

By Rob Davidson

PICMG specification update

It has been another busy year for those in the PICMG who, for reasons best known to themselves, love to delve into the ultimate in fine print of PICMG specifications. These spec heads have been creating entirely new documents that the industry has been eagerly awaiting, as well as updating existing popular specifications to incorporate the latest developments.

Achievements

PICMG's biggest achievement of the year so far is the July release of the much-anticipated MicroTCA specification (PICMG MTCA.0 R0). MicroTCA completes the trio of specifications that includes AdvancedTCA and AdvancedMC. This trio covers the wide range of equipment in the telecom network from the core to the edge. Even though products complying with these specifications are used in many markets, the Telecom Computing Architecture (the TCA in AdvancedTCA) framed the design goals.

MicroTCA takes the overall framework of AdvancedTCA, uses the module form factor from AdvancedMC, and defines small form factor system architecture. MicroTCA systems scale from small, inexpensive simplex implementations to fully redundant 6-nines high availability systems. As the AdvancedMC cards are the plug-in components of the system and most are already available, MicroTCA should be off to a strong start. Even though the form factor is small, the specification is not – at 2.4 lbs and 538 pages it represents substantial detailed work by the subcommittee that has labored diligently over the last year and a half.

After the release

Once a PICMG specification is released the work does not go away. Issues are identified as companies develop products and test them at the PICMG Interoperability Workshops, and new technologies can impact the specifications as new ways of solving problems are identified. PICMG has two methods of updating specifications, which include the revision and the Engineering Change Notification (ECN). PICMG specifications are referred to by their number and revision. The current version of the AdvancedTCA base specification is PICMG 3.0 R2.0, denoting the second revision. ECNs are effectively addenda to the specification. They are used to address relatively minor changes that do not require a reprinting of the entire specification. Revisions are more extensive and incorporate previous ECNs into a new document. PICMG is always very careful to ensure that both ECNs and revisions have the smallest impact on backward compatibility possible.

This year has seen ECN 002 for PICMG 3.0 R2.0 (AdvancedTCA) adopted. This ECN incorporates two years of learning from the industry and includes clearer language that removes ambiguities, as well as many technological updates. PICMG AMC.0 R1.0 (AdvancedMC) also had ECN 001 issued in June. In addition to including improvements similar to those of AdvancedTCA, this ECN added new carrier connector types.

Work in progress

Meanwhile, work continues on several other projects within PICMG. This includes AdvancedTCA300, a variant of AdvancedTCA designed to fit in 300 mm deep equipment cabinets that are used by some carriers.

The PICMG Requirements Engineering Subcommittee (RES) has major work underway, but will not deliver a specification. Rather, this committee is working on new practices that will make PICMG specifications easier to use and improve the interoperability of products developed to them. For example, the first task the RES has set itself is to *enumerate* the AdvancedTCA specification and fully catalog the optional language. This will make it easy to clearly reference the section of the specification when identifying which features and options have been implemented in a product. The practice they develop in this exercise will then be applied to future specifications as part of the development process. Once this exercise is complete the RES will develop a standardized means of mapping profiles for vertical applications into the specification. The first profile to be mapped will the one developed by the SCOPE Alliance for telecom platforms. RES has set ambitious goals but has a strong membership working hard, and they will have an important, long-term impact.

New fabric definitions

A new fabric definition for AdvancedTCA is well into member review. PICMG 3.6 defines a fabric called Packet Routing Switch (PRS) for rapid transport of packets over an AdvancedTCA backplane.

AdvancedMC will soon be getting two completed fabric definitions. PICMG AMC.2 defines an Ethernet fabric, while PICMG AMC.4 will define Serial RapidIO mapping.

Other updates underway include a revision to AdvancedTCA, PICMG 3.0 R3.0, which will incorporate the recent ECNs and other updates. A second ECN for AdvancedMC is also underway.

The future

This column has reported on the progress of subcommittees that have been formally approved by the PICMG Executive Board. Other efforts go on in the background of PICMG that will probably turn into formal work at some time. These background efforts will be the focus of much attention in the coming year. As they are not formalized yet, I cannot report on them here. You will need to join PICMG to participate. Hint: 10 Gigabit Ethernet.

Visit www.picmg.org/specifications.stm for all PICMG specification updates.

Rob Davidson *has been vice president of marketing for PICMG since 1995. He has held senior marketing positions at Intel and Ziatech and is now an independent consultant based in San Luis Obispo, California.*

For more information, contact Rob at:

PICMG
1334 Oceanaire Drive
San Luis Obispo, CA 93405
Tel: 805-542-0999
E-mail: davidson@picmg.org
Website: www.picmg.org

By Hermann Strass

Powered by CompactPCI

Providing power at all times

In order to make it easy for power companies to control the flow of electrical power across national boundaries (there are many boundaries in Europe), the International Electrotechnical Commission (IEC) has generated the IEC 61850 standard. Power companies and energy traders use equipment that adheres to this standard to communicate and interoperate with others who also use such standardized equipment.

The international standard IEC 61850, Communication Networks and Systems in Substations, was ratified in 2002 with the first products appearing in 2004. It is supported by major utility companies such as AEP, EdF, and EON as well as major power control or automation companies such as ABB, Alstom, GE, and Siemens. Efforts in standardization started in 1987 in the United States and in 1988 in Germany. In the United States, the Electric Power Research Institute (EPRI) developed a Universal Communications Architecture (UCA), which was also published by IEEE as a Technical Report (TR 1550) in 1999. The IEEE and IEC agreed in the mid 1990s to use this TR, also known as UCA 2.0, as one of the major inputs to what became IEC 61850, a global standard composed of 10 parts. IEC 61850 uses logic models for components and protocol-agnostic real-time communication services. It uses TCP/IP and XML for communication and ISO 9506, the Manufacturing Messaging Specification, as an application.

The IEC 61850 standardization committees aimed to foster additional standards and side standards under the umbrella of IEC 61850. Several of these, including hydroelectric power, wind power, and distributed energy resources have been implemented. The gas and water works industry in the United States, including the American Water Works Association (AWWA) and others, has accepted and is promoting the use of IEC 61850. Given that IEC 61850 is neither application nor product specific it can also be used for other process control and automation applications outside the electrical utility area. The IEC 61850 motto is "One World, One Technology, One Standard."

In order to control electrical power on its way from generator to consumers in factories or homes and across national boundaries, ABB Power Technologies (Sweden) uses Intelligent Electronic Devices (IEDs). The ABB IED670 family of products satisfies the stringent requirements of the IEC 61850 standard in providing extensive communication capabilities and interfaces for maximum compatibility. The extensive I/O capability on analog and binary I/O allows implementation of the most advanced applications. Utilization of common hardware and software components simplifies setting, commissioning, and maintenance. IED670 features extensive logic capabilities that can be used, for instance, to perform load transfer, automatic disconnector opening, and other functions. The ready-to-use IED670 packages are designed to achieve optimum operation of the power system. The packages are delivered preconfigured and with default settings for line distance, line differential, transformer protection, and bay control applications.

The IED670 products from ABB are based on CompactPCI boards from Kontron (Germany). Kontron's CP620 board was modified into the CP6200 board to comply with ABB's EMC requirements and I/O capabilities in accordance with the IEC 61850 standard (Figure 1). The CP6200 is based on a PowerPC processor running under the VxWorks real-time operating system, a processor/software combination, which is most frequently used in such demanding applications. The CP6200 is equipped with one PMC and two PC•MIP mezzanine sockets for I/O flexibility through rear I/O connections. IEC 61850 uses Ethernet and TCP/IP, making it no surprise that the CP6200 is equipped with two full-duplex fast Ethernet channels. For reliability reasons, memory is protected with Error Correction Code (ECC).

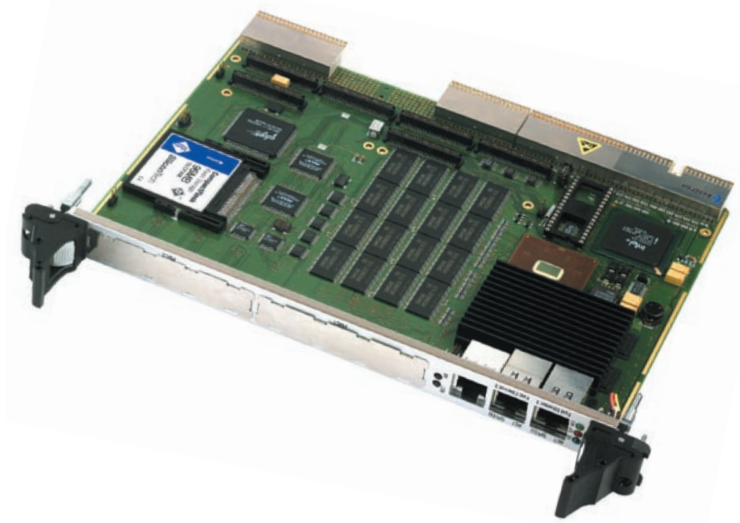


Figure 1

IEC 61850 was made for a very broad and varied application range. ABB claims that they were the first in the market to have products that meet all the requirements of IEC 61850. The IED670 family of products based on Kontron's CP6200 CompactPCI boards is a steppingstone into a large market.

For more information, contact Hermann at hstrass@opensystems-publishing.com.

By Peter Yan

Advanced traffic management aids converged IMS applications

IP Multimedia Subsystem (IMS) describes the network infrastructure that supports emerging Internet Protocol (IP) multimedia and telephony applications. IMS is defined by the 3rd Generation Partnership Project (3GPP) standards for wireless networks and is also being applied to wireline networks.

As applications based on IMS are becoming widely available to consumers, the equipment deployed in the traditional best-effort Internet will need to be upgraded to support the increased bandwidth and stringent Quality of Service (QoS) requirements.

To support IMS, new wireless cell phones and multimedia platforms will integrate combinations of technologies, including:

- Bluetooth
- Wireless USB
- Ultra Wideband
- 2.4 GHz and 5 GHz wireless LANs
- GPS location
- High-Speed Downlink Packet Access (HSDPA)
- True mobile video broadcasting technologies

For wireline terminals, high-definition video, DSL, and Passive Optical Network (PON) enable and drive high-bandwidth IMS applications.

Nonblocking architecture essential

With real-time video becoming more widely deployed, real-time traffic can account for significant network bandwidth, which can lead to starvation of data traffic. As such, a combination of strict priority and minimum bandwidth guarantees will become crucial and the system must be nonblocking to support deterministic QoS.

To realize the required QoS of a mixture of traffic with various Class of Service (CoS), advanced traffic management architectures are often used. The challenge is that QoS guarantees must be preserved in the presence of network congestion, component or board failure, various CoS requirements, and multicast traffic.

In order to meet these goals, advanced traffic management often makes use of the following techniques:

- Prioritization and isolation of traffic based on CoS using queuing architectures
- Congestion management using flow control mechanisms that act on queues
- Allocation and management of resources (bandwidth, buffers) to optimize system performance

Network element systems that implement advanced traffic management often support multiple ports, which are used for aggregation or interconnection of various networks together in the Internet. A popular standard interface used inside such systems is RapidIO. Defined by the RapidIO Trade Association, RapidIO is an industry standard fabric interconnect supplying the advanced traffic management that converged IMS applications need.

RapidIO is designed to be compatible with popular integrated Network Processing Units (NPUs), communications processors, host processors, and networking DSPs. RapidIO enables nonblocking switching and guaranteed QoS. Table 1 shows the system requirements for achieving guaranteed QoS, and how RapidIO addresses these requirements.

RapidIO features that enable low latency include:

- Low overhead protocol resulting in high fabric utilization
- Hardware-based data encapsulation with a small Maximum Transmission Unit (MTU) size for reduced latency variability
- Hierarchy of flow control features for congestion avoidance and congestion management

Requirements	How RapidIO addresses requirements
Low system-level latency	Lightweight protocol stack implemented in hardware
High link bandwidth to support broadband applications	1 and 4 lane SerDes-based serial links support 2.5 and 10 Gbps data rates.
Next generation physical layer	Next generation physical layer SerDes with support of up to 80 Gbps data rate per port
Minimum bandwidth guarantee	Virtual Channel (VC) architecture consists of scheduling and flow control mechanisms, which result in isolation of traffic from diverse classes of service.
Nonblocking system	System-level Virtual-output-Queuing (VoQ) and flow control enable real-time QoS support
Fine granularity traffic management	Streams with a few Kbps bandwidth granularity are managed individually.
End-to-end flow control and resource management	End-to-end logical layer flow control between processors
Multicast	Transport layer supports up to 64K connections that can be used as unicast connections or to designate multicast groups. Switches are capable of multicast.
Interworking with other packet interfaces with QoS support	Data streaming encapsulation and physical layer (segmentation and reassembly)
High availability, redundancy, hot swap, and failover	Fault detection and dual star configuration
In-order packet delivery	Supported by physical layer
Lossless transmission at the link and end-to-end levels	Supported by physical and logical layers

Table 1

RapidIO offers hierarchical flow control architecture at the link and logical layers. The link layer's transmitter based flow control makes pipelining effective. Credit based Virtual Channel (VC) and Virtual-output-Queuing (VoQ) flow control are also supported. The logical layer (processor to processor) supports Xon/Xoff of specific flows, bidirectional arbitration for flows, and end-to-end flow management of classes, streams, and ports.

The associated flow control mechanisms of the VC and VoQ architecture operate at the link layer. What's more, they can provide dramatic performance benefits at the system level, while adding minimal overhead. VC architecture allows for minimum bandwidth reservation for each class of service. VoQ architecture allows for system-level head-of-line blocking avoidance to guarantee deterministic latencies for real-time traffic.

VoQ and VC architectures

Consider a one-lane road with cars arriving at an intersection. If the first car in line should turn left, and is blocked from doing so (due to heavy traffic in the left road), then all of the cars behind the first car must wait, even though the other roads (straight and right) are clear of traffic.

Translating this example to a communication system, the cars represent packets, the intersection represents a hub switch, and the backed-up line represents a First-in-First-out (FIFO) queue. Real-time packets that are blocked in the FIFO would suffer latencies, which are nondeterministic. The packets would likely fail to achieve their required levels of QoS. Examples of standard protocols, which suffer from system-level blocking, are Ethernet and PCI Express.

On the other hand, consider a road with multiple lanes. Cars arriving at the intersection go to the lane corresponding to the turn they plan to make. If the car turning left is unable to do so because of congestion, the cars in the other lanes are still able to go because they have another path to their destination using the other lanes. Implementing the RapidIO VoQ architecture enables a nonblocking system.

To understand the advantages of the Virtual Channel architecture consider a road with a continuous stream of cars passing through an intersection that have the right-of-way because they are on the main road. If the car on the side street arrives at the intersection and does not have the right-of-way (for instance, if the vehicle encounters a stop sign), it must wait for a gap in the main street traffic in order to turn left. This wait could indefinite, which can lead to starvation.

In a communication system, real-time packets, are usually given the highest priority in order to guarantee the lowest latency. With the resulting strict-priority scheduling, a data packet, must wait until there are no other higher priority packets (such as real-time packets) destined for the same output before it can be transmitted. Thus, data packets can experience starvation, receiving zero bandwidth for a potentially long time. The Ethernet protocol does not specify the scheduling for its priority queues. PCI Express provides the option of minimum bandwidth for its VC queues. Implementations of only strict priority for these standard interfaces will suffer system-level blocking.

Combination approach

On the other hand, consider that data packets will be scheduled to be transmitted at particular intervals. Thus, data traffic will not be starved and can be guaranteed a minimum amount of bandwidth specified by the QoS requirements of the particular CoS to which the data packets belong. The RapidIO VC architecture allows for the system to guarantee minimum bandwidths, while also preserving the low latencies required for real-time packets. To do this, often a combination of strict and minimum bandwidth scheduling will be employed VC and VoQ architectures can be implemented in a communication system to improve system performance.

A communication system, typically consists of several line cards. The line cards communicate to each other as peers through a shared hub switch. Each line card may have a single processor or multiple processors used as a farm. The processors are usually connected to a bridge or a local switch on the line card, which is in turn connected to the hub switch over a RapidIO backplane. The interface between the processor and the bridge and between the processors and the local switch can be RapidIO as well in order to reduce system cost and improve performance.

In order to support VoQ, the local switch allocates a separate queue per hub switch output port. In this simple example, if the hub switch's output port 1 is congested, the hub switch conveys VoQ flow control information to the local switch, which should halt the traffic in the queues corresponding to hub output port 1. The local switch's multiple queues, one per hub switch output port, correspond to the multiple lanes at an intersection for cars going left, straight, and right. The link between the local switch and the hub switch represents the intersection. If any one of the hub switch's output ports is congested, the packets in the other queues of the local switch are not affected and can still proceed as usual.

Similarly, to support the virtual channel architecture in RapidIO, a separate set of queues is allocated for each VC. While RapidIO provides support for up to nine VCs. In this simple example, there are two VCs. In the local switch, each VC hierarchically supports a group of VoQs for the hub switch's output ports.

The hub switch, which can maintain the same queuing architecture as the local switch, should schedule packets for each VC according to its minimum required bandwidth. VCs that correspond to data applications are usually the most in need of minimum bandwidth guarantees. Real-time traffic scheduled according to strict priority could grab much of the system bandwidth and potentially starve data packets indefinitely. However, the scheduler must also make sure that interactive and streaming packets are transmitted with the required levels of low latency. Erlang has implemented schedulers that support the requirements noted earlier as a combination of strict priority and minimum bandwidth scheduling.

If the hub switch experiences excessive congestion for a particular VC, flow controlling that VC lets traffic belonging to the other VCs traverse the system without violating their QoS requirements. Control takes place by having the hub switch convey VC flow control information to the local switch for a particular VC. The local switch's scheduler will then react to the flow control by limiting the number of packets transmitted for that VC. This can only be done if the local switch has queued packets for each VC separately. If the hub switch experiences congestion for VC1, it sends flow control information to the local switch, which temporarily stops transmission of all packets belonging to VC1 queues.

To model IMS systems with a mixture of voice, video, and data traffic, it is important to simulate bursty traffic. Data transfers and variable bit-rate video traffic tend to be bursty in nature. The simulation assumes an average burst length of 20 packets being transferred between line cards. If each RapidIO packet size is 256 bytes for the payload, this would correspond to 20 × 256 = 5,120 bytes being transferred, which could be the size of four video packets (each of 1,280 bytes), transmitted in a burst.

For the base case, consider a system architecture that does not support any flow control. The system implementation could be simpler and may be able to achieve the lowest latency at very low loads. For instance, at 1 percent load, it was assumed that this switch architecture has a fall through latency of 200 ns. However, with increased levels of congestion and the inability to control the congestion, the latency is about 100 microseconds at 55 percent load and quickly goes to infinity thereafter.

A switch architecture that supports VC flow allows for improved performance, with about 100 microseconds latency at 65 percent load. This is an incremental performance improvement, however, the VC architecture allows for minimum bandwidth guarantees for traffic that is not real-time (data), while preserving the QoS for real-time traffic (voice and video). This can be achieved with a combination of strict, plus Deficit Round Robin (DDR) or Weighted Round Robin (WRR) scheduling, which Erlang has implemented in switch fabrics and traffic managers.

Finally, the switch architecture, which supports VC and VoQ flow control, starts at 800 ns latency at 1 percent load because the scheduling algorithm requires more start-up time in the pipeline. However, the latency will be lower than the base case at loads greater than 25 percent and can reach 80 percent or higher loads. With additional scheduling and bandwidth management optimizations, Erlang has been able to achieve 95 percent and greater loads with less than 100 microseconds latency in high-performance switch fabrics.

Peter Yan *is an active member of the RapidIO Trade Association and chief technology officer at Erlang Technology.*

To learn more, contact Peter at:

Erlang Technology
345 Marshall Avenue, Suite 300
Saint Louis, MO, 63119
Tel: 314-276-5583
Fax: 314-336-5902
E-mail: petery@erlangtech.com
Website: www.erlangtech.com

How DSO, COTS, and open architectures can help solve the looming telecom software crunch

By Michael Christofferson

Complex distributed telecom and networking applications require a new method of development. Michael makes the case that by using industry standard interfaces and open architectures, NEPs and TEMs can greatly accelerate the development of applications and systems.

Worldwide, most network equipment makers have already abandoned the practice of creating their own proprietary DSPs, network processors, operating systems, protocol stacks, and management tools. Many, however, are still creating significant pieces of their application-specific hardware and software infrastructure from the ground up, constantly inventing and reinventing the wheel from one project to the next. For these equipment makers, many of whom are trimming engineering staffs in order to contain costs, this homegrown approach is becoming increasingly untenable.

According to industry analyst Venture Development Corporation (VDC), the amount of code deployed in today's network equipment is growing exponentially – currently accounting for more than half of total project costs. Meanwhile, the number of available developers is growing at a relatively flat pace, thereby creating a serious mismatch that makes it increasingly difficult to meet time-to-market windows. Already, VDC estimates that 50 percent of device projects fall behind schedule by an average of four months.

The world's approximately 600,000 developers cannot keep up with the rocketing demand for device software required by today's smart cell phones, automobiles, appliances, and entertainment systems. In addition, manufacturers are facing the twin challenge of ever-shortening production cycles to meet competitive marketing pressures while at the same time having to handle exploding device complexity as end users demand new features and sophisticated capabilities.

To ease this software development challenge, and to make do with leaner engineering staffs, many equipment makers are embracing a new development process. An approach known as Device Software Optimization or DSO, represents a fundamental rethinking of the design process, leveraging products and practices that embrace reusable code, open standards, and preintegrated Commercial Off-the-Shelf (COTS) technology, standardized across the enterprise (not just across a single development group).

Equipment makers using a combined DSO and COTS paradigm can trim their platform teams by up to 80 percent. Manpower cost is reduced, and NEPs can allocate their engineering resources to value-added application and service development.

Advantages of an open architecture platform for telecom

By using a preintegrated DSO telecom platform, telecom developers can shorten the lengthy platform design/integration process into an evaluation and purchasing process that can take as little as two months. All told, this COTS approach can shorten the application development cycle by up to 50 percent.

An open architecture platform's layer of abstraction clearly separates telecom applications and the underlying hardware and system software. This layer of abstraction, coupled with the use of standard interfaces, enables designers to use best-of-breed COTS hardware and software from multiple vendors. It also enhances portability, allowing NEPs to upgrade hardware and software at later dates with minimal disruption to their proprietary applications.

Open architecture telecom platforms provide the basic components needed to develop and host telecom applications and services. Figure 1 shows the components typically represented by the Enea Networking Application Services Platform (NASP) platform:

- Operating systems
- Interprocess Communications (IPC), such as Enea LINX and Open Source IPC technology
- High Availability (HA) middleware framework that is Service Availability Forum (SAF) compliant
- Database management system

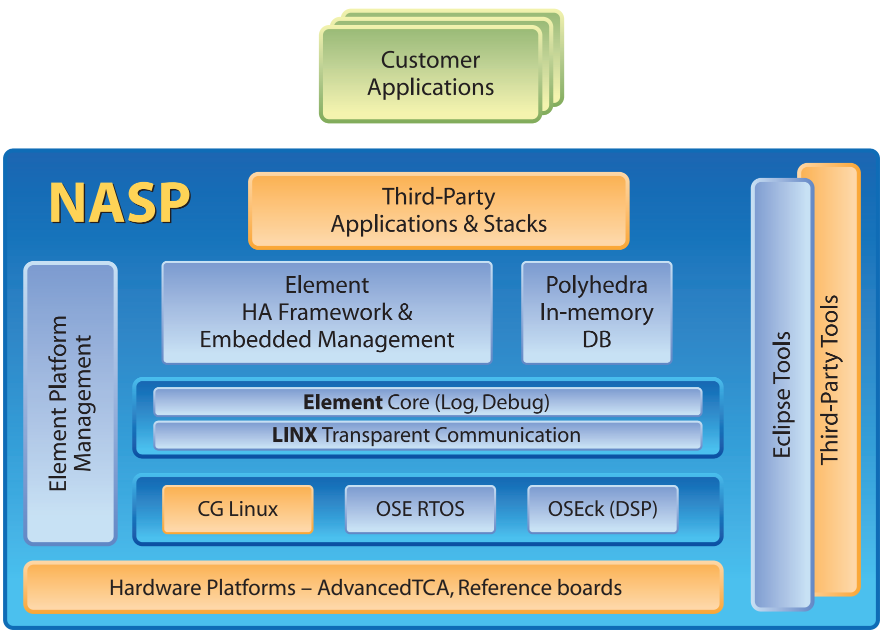


Figure 1

Operating systems

Ideally, a telecom software platform should support multiple operating systems in both homogeneous configurations, such as those with Linux or an RTOS deployed throughout the system, and heterogeneous configurations, which combine Linux and one or more RTOSs deployed on multiple CPUs, shelves, and blades.

This flexibility enables developers to select the OS or processor combination best suited to their application. For example, some NEPs may prefer to run Linux on one set of blades to host IT-oriented supervisory and enterprise management functions, while using an RTOS on another set of blades to host DSP-based media processing applications with tight size and performance constraints.

Interprocess communications

In a distributed network, an interprocess communications framework like Enea's open source LINX can provide the glue needed to integrate platform components and applications across multiple processors, operating systems, blades, and shelves (Figure 2). Ideally, this framework should provide dependable, high-speed transport for both the control and data plane over reliable as well as unreliable interconnects and protocols. It should also support the encapsulation of other bearer protocols – such as TCP, UDP, and SCTP – for data transport. Because it is open source, Enea's LINX also makes it possible to use the IPC framework for a wide variety of applications and systems.

By using direct message passing, an interprocess communications framework's can increase performance by enabling application processes to communicate directly with each other on a peer-to-peer basis, without having to synchronize through intermediate mechanisms such as mailboxes, semaphores/mutexes, event flags, UNIX-style signals, or even sockets. This direct approach also simplifies communications and facilitates logical process separation, thereby enhancing reliability and simplifying fault recovery, particularly in distributed systems utilizing multicore devices and complex network topologies.

In order to maximize scalability and portability, the interprocess communications services should provide transparency, independent of the underlying processor, operating system, or interconnect. This transparency enables distributed platform components and applications to communicate in a seamless fashion, as if they were residing on a single processor under a single operating system. When combined with the ability to dynamically discover communication endpoints, this transparency also enables developers to locate applications on any node in the system, and change the configuration at run time. The result is that developers and service providers can dynamically change and scale the system configuration, redistribute applications across multiple blades, and upgrade the hardware with minimal application code changes.

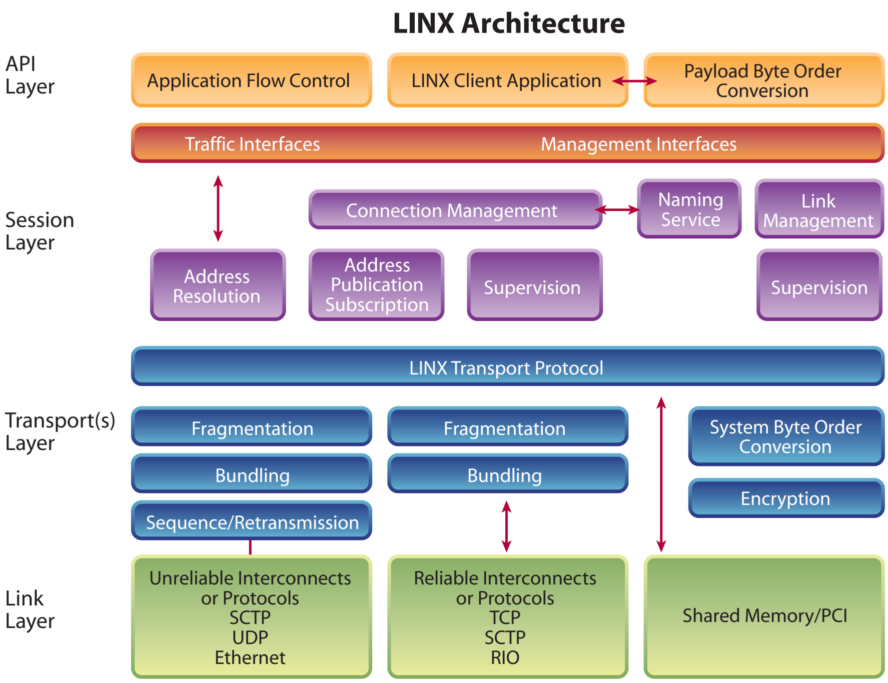


Figure 2


CompactPCI Express
Development Systems
Available Now!
8U CPCI/CPCIe Hybrid System
MAX EXPRESS
Cable from a Host PC to One Stop Systems' Hybrid CPCI/CPCIe System at 10Gb per second
Ideal Platform for CPCI and CPCIe Board and Software Development at Highest Performance Available.
Interface Board to Host PC
Interface Board to Host PC
5U CPCI/CPCIe Hybrid System
MAX EXPRESS
Now available at
ONE STOP SYSTEMS
Call today.
(877) GET-CPCI
www.onestopsystems.com

Middleware framework

The flexibility provided by the network platform's IPC layer lays the foundation for more advanced distributed communications, instrumentation, monitoring, and high availability services, collectively referred to as middleware. The middleware extends the IPC's process-to-process communications services, providing one-to-many communications that facilitate system wide communications, instrumentation, and event notification. These extended communications services, in turn, lay the groundwork for high availability monitoring, detection, recovery, and reporting services that are essential for building a true nonstop computing platform.

To simplify configuration and management at the slot, blade, and chassis level, COTS middleware solutions provide shelf management services, typically utilizing standard interfaces, including SAF's Hardware Platform Interface (HPI). Complementing the middleware's shelf management services are heuristic fault management services, which provide monitoring, detection, recovery (for example, restarting a failed application or failing over to a redundant blade), and reporting for every resource in the system.

Database management

The network platform may simplify information (data) management and sharing across multiple nodes with a Relational Database Management System (RDBMS). Unlike traditional desktop databases, these embedded databases must often work in a diskless environment and deliver higher levels of performance and availability. Enea's small-footprint Polyhedra RDBMS, for example, uses a memory-resident design that boosts performance by 10x relative to conventional disk- and flash-based RDBMSs.

A new way of getting the job done

In the past, NEPs have been content to create their own OS, middleware, and database solutions. However, with the new challenges of reduced production cycles and ever-increasing software complexity, a growing number have recognized that they can no longer remain competitive by creating, maintaining, and porting platform software in-house. Field-proven, pre-integrated COTS network platforms allow NEPs to outsource their platform design, focus engineering resources on value-added applications and service development, and get their completed designs to market on time and on budget.

Michael Christofferson *is director of product management, Enea Embedded Technology.*

To learn more, contact Michael at:

Enea Embedded Technology
2635 North First Street, Suite 118
San Jose, CA 95134
Tel: 408-383-9480
Fax: 408-383-9485
E-mail: mikec@enea.com
Website: www.enea.com

I-TDM: Supporting TDM voice in the age of MicroTCA and AdvancedTCA

By Robbie Dhillon, Ian MacMillan, and Amir Zmora

The ecosystem that is growing around the I-TDM standard now includes both hardware- and software-based implementations. As with any new standard, initial implementation work involves identifying areas where the standard needs enhancement. The authors outline the role PICMG SFP.1 – also known as Internal Time Division Multiplexed circuit switching – plays in converting voice and media packets for transport and storage.

Demand for voice and video over IP along with the adoption of IMS architecture for next-generation networks are driving the trend towards network components based on standard form factors. Many telecom equipment manufacturers who have traditionally designed proprietary platforms internally are now seeking off-the-shelf components based on standard telecom grade, high capacity form factors. As a result, the market is adopting MicroTCA and AdvancedTCA platforms, with large deployment numbers predicted for 2007 onward.

A number of key IMS architecture elements handle voice and media traffic. In order to interconnect with voice and media traffic from TDM networks, the IMS architecture provides platforms that interface with these TDM networks and support voice, media, and signaling.

MicroTCA and AdvancedTCA are packet-based, causing IMS systems to transmit TDM via I-TDM running over packet transport, such as GbE. There is now a growing ecosystem around the I-TDM standard with the availability of both hardware and software-based implementations.

IMS voice and media platforms

There are a number of IMS platforms that interface with TDM voice and media.

Media gateways

IMS and other NGN networks require a media gateway, which typically translates voice and video traffic from TDM to IP networks, to connect between the following networks:

- Broadband wireline IP network, mainly using SIP but also using legacy H.323 equipment
- Broadband wireless IP network (Wi-Fi and WiMAX), typically using SIP
- 3G real-time conversational voice and video, using 3G-324M currently and SIP in the future
- Voice PSTN network
  - Access media gateways that have TDM telephone lines or TDM trunk interfaces
  - Border media gateways that interconnect TDM networks to IMS networks. For example, connecting a TDM wireline network to an IMS-based wireless network
  - Mobile video media gateways that translate voice and video bidirectional and streaming traffic between IP (typically SIP) networks and mobile 3G-324M networks. The 3G-324M network has a fixed limited bandwidth of 64 Kb and screen size is typically limited to QCIF resolution, so the gateway must perform two key tasks:
    - **a.** Transcoding: Voice to NB-AMC and video to H.263 or MPEG-4
    - **b.** Modification: Changing the frame rate, typically to 10 FPS and the resolution to QCIF
- Video over PSTN using H.324 is deployed in countries where broadband penetration is limited

In the case of video over PSTN, deployed in Italy and the UK, the H.324 streams are sent using modem connectivity over PSTN lines. As in 3G-324M control, voice and video are multiplexed and sent over the network. Connecting this communication with other networks such as broadband SIP requires gateway functionality similar to that used by the mobile video media gateway.

Media resource functions

Media resource functions perform IMS network media services, such as voice mail and recorded announcements. Many MRFs are designed to support both IP and TDM interfaces, although implementing an MRF with IP support only is possible.

Wireless radio network controllers/ base stations

Wireless radio network controllers manage and connect with wireless base stations. While the base stations will migrate to IP transport over time, many existing base stations use TDM transport to connect with the RNC. Base stations performing IP transport can use I-TDM to transport voice internally to the base station.

Conferencing servers

Similar to MRFs, many conferencing servers are designed to support both IP and TDM interfaces.

I-TDM allows these IMS platforms to be implemented using MicroTCA or AdvancedTCA by taking the TDM voice and media and converting them into packets for transport and storage within the platform.

I-TDM building blocks

The IMS platforms we have described incorporate two types of building blocks that must support I-TDM:

- I/O interfaces, which provide the physical interface to TDM networks
- Digital signal processors, which transform the TDM media for storage and transport in IMS networks

I/O interfaces

In MicroTCA and AdvancedTCA platforms, I/O interfaces are typically implemented as Advanced Mezzanine Cards (AdvancedMCs). The AdvancedMCs take the TDM interfaces and convert the TDM voice to I-TDM for transport over the backplane of the MicroTCA and AdvancedTCA platforms.

Bundling signal channels with the voice bearer channels enables AdvancedMC interface cards to add significant value to the MicroTCA/AdvancedTCA platform by providing intelligent protocol offload and acceleration. The AdvancedMC processor and protocol software must be sophisticated enough to handle the TDM network's large number of different protocols.

The typical standard TDM interfaces include T1/E1/J1 and OC-3/STM-1 or OC-12/STM-4.

The Interphase iSPAN 3639 AdvancedMC Multiprotocol T1/E1/J1 Intelligent Communications Controller, available in quad or octal configurations, (Figure 1) is an example of an intelligent protocol offload/acceleration AdvancedMC. This card handles both:

- Signaling protocols such as SS7 and ISDN with an onboard processor
- I-TDM for up to 256 DS-0 flows with an onboard FPGA

Figure 1

Wireless networks introduce an additional complication by using subrate DS-0 TDM voice. AdvancedMCs that can provide subrate TDM voice interfaces address this issue and have enhanced the I-TDM protocol to transport the subrate voice. For example the Interphase iSPAN 3632 Quad-Port Channelized OC-3/STM-1 Interface Processor (Figure 2) provides up to 8,032 I-TDM flows.

Figure 2

Digital signal processors

A digital signal processor farm is an essential component in media processing-intensive applications such as media gateways and media servers. The DSP farm handles all media processing functionalities that enable convergence of IP (wireline and wireless), PSTN, and mobile networks. This board must perform not only simple transcoding of voice and video, but also:

- Voice event detection and generation, DTMF detection, CNG, VAD, and ECAN
- Video frame rate and resolution change, text overlay, alpha blending, cropping, picture-in-picture
- Media server tasks such as streaming, recording, and conferencing of voice and video
- Fax and modem processing

In MicroTCA/AdvancedTCA platforms, the media processing capabilities are usually implemented on AdvancedMC cards populated with DSPs. The SurfRider AdvancedMC from Surf Communication Solutions (Figure 3) for example can support the convergence of PSTN, IP, and wireless networks, and must interface to the IP and TDM worlds by supporting I-TDM. I-TDM enables the passing of the TDM traffic over the AdvancedMC card's packet-based interfaces. Dedicated mechanisms on the AdvancedMC cards convert the incoming I-TDM packets to TDM traffic, and vice versa.

An AdvancedMC DSP board for media processing functions must support:

- A flexible number of channels, I-TDM flows, and different mixes of 1 ms and 125 µs flows
- A variety of external interfaces: Some customers may require the TDM to be moved over Ethernet packets; others may require different packetization support (such as SRIO, InfiniBand)
- The ability to dynamically and simultaneously run all media types to allow moving from 100 percent voice to 100 percent video, and any mix in between
- Separation between media and control functions and utilizes DSPs with a direct IP network interface to avoid aggregation on the host processor, which typically creates bottlenecks in the system and increases media delay, reducing quality
- External memory per DSP on board, enabling easy addition of features without concerns about code and data size
- A DSP software framework that enables:
  - Adding user-defined and proprietary algorithms to the DSP
  - Support for predictive scheduling, allowing tasks such as DMA of relevant data to be sequenced automatically while a previous task is being processed
  - Support for real-time processing with guaranteed quality of service and latency

Figure 3

I-TDM standard brief

The legacy solution for carrying TDM on the backplane has been the H.110 bus, with 32 TDM data highways at 8 MHz. Carrying TDM over a serial packet bus reduces pin count, increases reliability, and allows the prospect of a single fabric for carrying all chassis traffic. The advent of MicroTCA and AdvancedTCA has increased the urgency of the problem, because unlike CompactPCI, there is no defined TDM highway backplane in AdvancedTCA/AdvancedMC.

PICMG chose a layered, fabric-agnostic approach to standardize a TDM-over-packet protocol. The lower layer specification, SFP.0, defines essential fabric services, such as detection of misrouted or dropped packets, multiplexing, and end-to-end fabric integrity check. PICMG deliberately chose a lightweight protocol to run directly on top of the Layer 2 packet. For example (Figure 4), SFP.0 runs directly over MPLS over Ethernet, without requiring a bulky IP or TCP/UDP layer.

The next protocol layer, SFP.1, also known as I-TDM, provides TDM-centric header services. I-TDM multiplexes several TDM channels together into one packet,

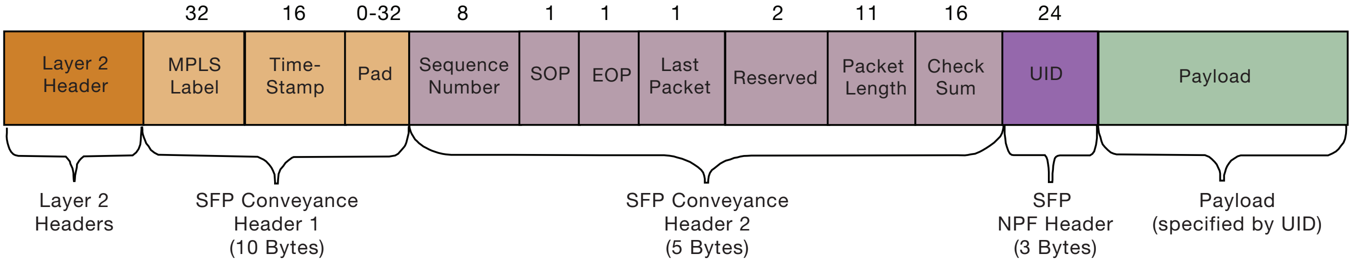


Figure 4

as opposed to waiting several frame times to accumulate enough data for a given TDM channel. This step maintains fabric efficiency, because most fabrics (and network hardware such as switches and endpoints) become increasingly inefficient with small packet sizes. Figure 5 shows an I-TDM 125 µs mode payload format. I-TDM payload format choices are:

- A packet emission interval of 125 µs provides the lowest possible latency, and is recommended for hardware implementation
- Packet emission interval of 1 ms, which creates higher latency, but is easier to handle in host media processing and other software-centric approaches

Unlike WAN-centric TDM over packet standards such as PWE3/TDMoIP, I-TDM is intended as an in-chassis protocol. Therefore, there is no support for timing recovery, which greatly simplifies the implementation.

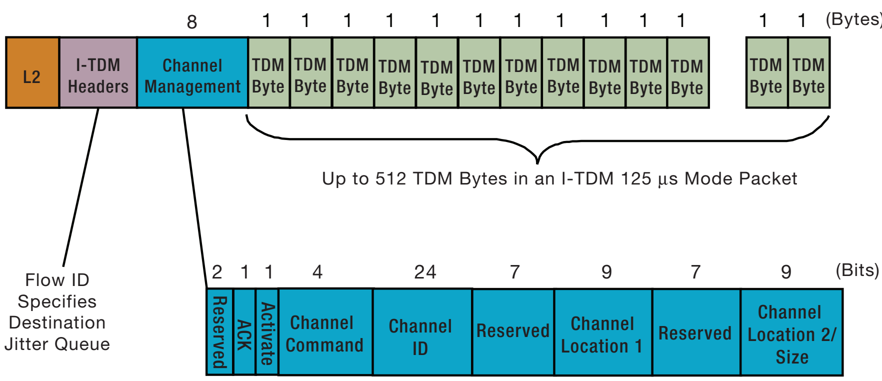
The I-TDM standard primarily benefits designers as a chassis-optimized, fabric-neutral technology supported by multiple vendors. It is possible to transport TDM over packet in multiple nonstandard ways, and point solutions have been implemented in the industry. Widespread adoption of I-TDM as the TDM transport backplane technology will allow system vendors to use interoperable vendor parts and concentrate on end functionality over plumbing.

I-TDM enabling technologies

Early implementation of the I-TDM standards has included software-only implementations using dedicated network processors and reprogrammable FPGAs (Altera and Xilinx). Both approaches have the flexibility to accommodate the changes and extensions inherent in a newly introduced standard.

The NP-based approach is ideal for supporting a mix of 1 ms and low density 125 µs modes of operation. The FPGA-based method scales better to higher density 125 µs implementations.

A software implementation of 125 µs I-TDM in Wintegra's WinPath NP family (Figure 6) supports densities of up to



Command Set
0 = Reserved
1 = New Channel_ID at Byte Offset Channel _Location_1 with Size = 1
2 = Close Channel_ID at Byte Offset Channel_Location_1 with Size = 1
3 = Relocate Channel_ID from Byte Offset Channel_Location_2 to Channel_Location_1
4 = Cyclic Reaffirmation: Channel_ID is at Byte Offset Channel_Location_1 with Size = 1
5 = Packet Rate Integrity Check
6-15 = Reserved

Figure 5

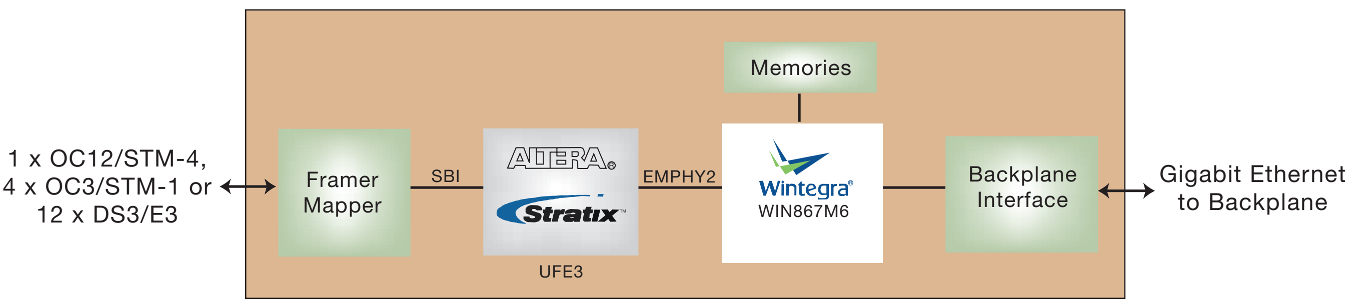


Figure 6

28 T1/21 E1s (672 DS0s) with DS0 granularity per I-TDM channel and up to 84 T1/63 E1 with 8xDS0 granularity per I-TDM channel. Wintegra also supports higher densities of up to OC-12 (8K channels) by using an I-TDM load in its UFE FPGA.

Figure 7 shows Accolade Technology's FPGA-based ASTDM solution. The ASTDM features dual GbE interfaces to the fabric switch side, a TDM bus (signaling termination, DSP resources, or SONET framers), and a CPU interface. This architecture uses dedicated state machines to manage both 1 ms and 125 µs modes of operation while directing command and control packets to the CPU interface. It can support densities of four T1/E1s to OC-12.

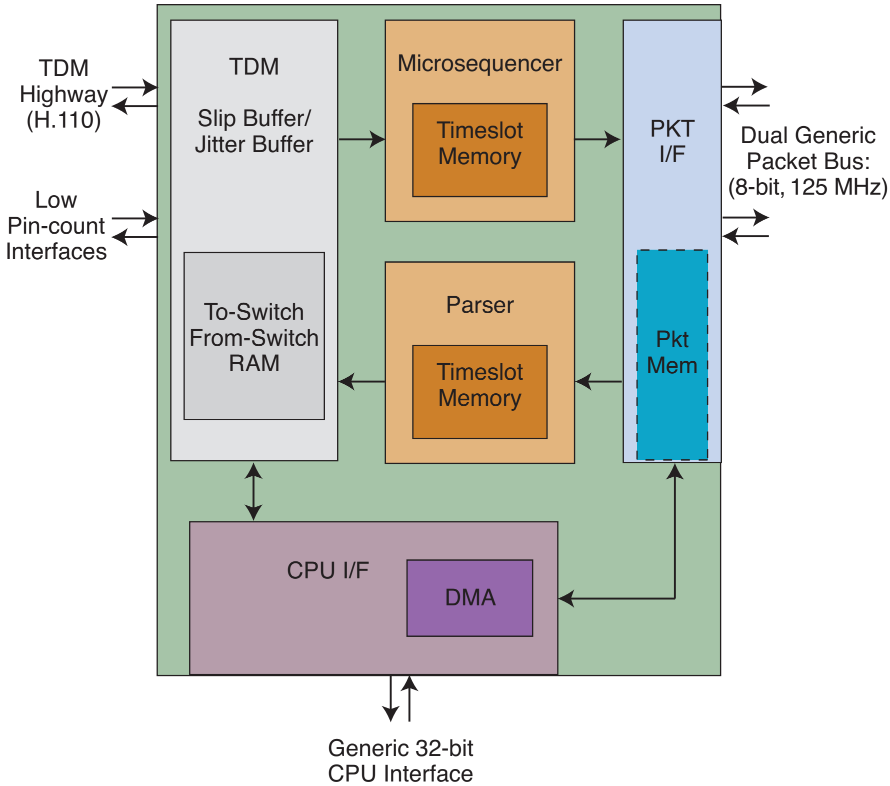


Figure 7

State of the I-TDM ecosystem

The current I-TDM ecosystem includes manufacturers of enabling technologies and board level products. Suppliers of IP cores for FPGAs and software implementation on network processors that have announced I-TDM solutions include Accolade Technology and Wintegra Inc.

Suppliers of TDM, signaling interfaces, and media server/DSP blades that have announced AdvancedTCA/AdvancedMC board level solutions with I-TDM functionality include Interphase Corporation and Surf Communications, among others.

TDM interface vendors and DSP vendors are testing I-TDM interoperability. Accolade Technology is introducing an I-TDM reference test platform based on its ASTDM implementation of the I-TDM standard on a Xilinx-based development platform. This menu-driven I-TDM reference test platform supports call setup and I-TDM traffic generation and termination.

Future enhancements to standard

The current I-TDM standard is sufficiently mature for product implementation. However, for optimal functionality and interoperability, additional issues should be considered.

Explicit support for subrate channels

The most common channel format is a complete DS0, equivalent to a 64 Kbps data rate. However wireless networks widely use subrate channels (fractional DS0, such as 32 Kbps, 16 Kbps, 8 Kbps). Currently, the I-TDM standard cannot specify channel ID or carry out 125 µs mode channel management commands like New, Change, Relocate, or Cyclic Reaffirmation on a sub-DS0 granularity. While it is still possible to transport sub-DS0 channels by some private understanding between the two peers, a standardized scheme promotes interoperability and possibly reduces wasted bandwidth.

Redundancy and protection switching support

While specific redundancy schemes at the chassis level are not precluded by the I-TDM standard, they are not explicitly supported.

Modifications or extensions to the 125 µs channel management command scheme

I-TDM's 125 µs channel management in-band nature is a strong architectural benefit. However, improvements in some modes of operation may be desirable.

Summary

Platforms designed around MicroTCA and AdvancedTCA are rapidly coming to the market. I-TDM provides a key technology to enable IMS next-generation network platforms based on MicroTCA and AdvancedTCA to successfully leverage the significant investment in legacy TDM voice and media networks, while at the same time being able to provide the advanced services and flexibility inherent in the MicroTCA/AdvancedTCA architectures.

A growing number of critical IMS I/O and DSP building blocks are incorporating I-TDM solutions.

Since the standards and the building blocks for these solutions are currently in the initial stages of market penetration, innovative and flexible implementations will pave the way for additional capabilities in the near future. As with any new technology, the I-TDM standards will likely continue to evolve based on implementation experience in voice and media transport within MicroTCA and AdvancedTCA platforms. I-TDM clearly

I-TDM ECOSYSTEM GLOSSARY

BSC	Base Station Controller
CNG	Comfort Noise Generation
DMA	Dynamic Memory Allocation
DSP	Digital Signal Processor
DTMF	Dual Tone Multi-Frequency
ECAN	Echo Cancellation
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GGSN	Gateway GPRS Serving/Support Node
IMS	IP Multimedia Subsystems
IP	Internet Protocol
I-TDM	Internal Time Division Multiplexed
MRF	Media Resource Function
NP	Network Processor
PSTN	Public Switched Telephone Network
PWE3/TDMoIP	Pseudo Wire Emulation Edge to Edge/Time Division Multiplexed traffic over IP
QCIF	Quarter Common Intermediate Format
RNC	Radio Network Controller
SIP	Session Initiation Protocol
SONET	Synchronous Optical Networking
SRIO	Serial RapidIO
TCP/UDP	Transmission Control Protocol/User Datagram Protocol
TDM	Time Division Multiplexed
TEM	Telecom Equipment Manufacturer
VAD	Voice Activity Detection
VoIP	Voice over Internet Protocol

offers the benefits of a cost-effective, standards-based solution for offering new services while protecting investments in today's infrastructure.

Robbie Dhillon *is VP of business development at Accolade Technology, with more than 20 years of telecommunications and networking experience. Prior to cofounding Accolade, he was president of Network Modules Inc. and VP of business development at SBS Technologies. Robbie has a BSEE and MS in Physics from Portsmouth University, UK.*

Ian MacMillan *is the senior product marketing manager at Interphase Corporation responsible for the AdvancedTCA/AdvancedMC and Signaling Solutions product lines. Ian's broad telecommunications background spans more than 15 years and includes work for large TEMs and carriers, including Nortel Networks and Verizon. Ian has worked with emerging technologies covering all sectors of telecommunications including voice, data, and wireless.*

Amir Zmora *is Surf Communication Solutions VP business development, responsible for all business development, including establishing partnerships with telecom infrastructure hardware manufacturers. Amir is a well-known speaker at VoIP events, and has published articles in numerous industry magazines. Amir holds an MBA from Tel Aviv University, a BA in Economics from Hebrew University, and a BA in Software Engineering from the Sela Institute.*

To learn more, contact the authors at:

Robbie Dhillon
Accolade Technology
8 Woodfield Road
Acton, MA 01720
Tel: 508-479-9663
E-mail: rdhillon@accoladetechnology.com
Website: www.accoladetechnology.com

Ian MacMillan
Interphase Corporation
2901 North Dallas Pkwy, Suite 200
Plano, TX 75093
Tel: 214-654-5000
E-mail: imac@iphase.com
Website: www.iphase.com

Amir Zmora
Surf Communication Solutions.
496 Old Connecticut Path, Suite 320
Framingham, MA 01701
Tel: 866-644-3379
E-mail: amir@surf-com.com
Website: www.surf-com.com

Selecting a modular media gateway to enable VoIP and other content-rich media services

By Venkataraman "VP" Prasannan

Here Venkataraman argues the case for a modular media gateway architecture that can help developers drive down costs for VoIP and support other content-rich communications services.

With continued globalization, many corporations have workgroups dispersed around the world. To support workgroup productivity and communications, companies are considering simpler, less expensive network solutions that combine content-rich voice, wireless, data, and video.

These businesses expect the services they select and implement to have the high quality of the telephone and other services they now use, and they expect them to boost productivity and help reduce overall communication costs.

To access the desired network services requires connections from wireless, wireline networks, and the Internet to the Public Switched Telephone Network (PSTN) with flexible, robust, scalable, and cost-effective media gateways. These gateways must reduce communication cost, increase the effectiveness of the dispersed workgroups, and form the foundation for future media services.

Juniper Research estimates that the business VoIP market will grow from $4.5 billion in 2004 to $20 billion by 2009. What's driving this growth? The cost of VoIP service is dropping, and its quality of service is continuously improving. What's more, VoIP costs less to run, install, and scale. Attracted by their near wireline quality and lower cost, businesses are already considering or employing offerings from vendors such as Vonage, DeltaTree, Net2Phone, and 8x8.

Initial VoIP considerations

Today, all communication can take place through a computer. Widely accessible broadband technology and Internet Protocol (IP) networks enable voice, data, wireless, and increasingly, video.

When considering VoIP for reducing communications costs, companies need to consider these questions:

- Is the media gateway under consideration a comprehensive and cost-effective solution with a low price but no price penalty for a fully loaded box?
- What is the existing voice and data traffic on our networks?
- What are the current voice and data usage patterns?
- Will the quality of the VoIP audio be acceptable?
- Are the reliability and uptime high enough to meet our requirements?

Media gateways bridge multiple technologies

A media gateway provides the conversion and switching of voice media between a network and its access points. For those using computers, Digital Subscriber Line (DSL), or cable modems, a media gateway converts, compresses, and packetizes voice data for transfer back and forth across the Internet backbone for wireline or wireless phones. Media gateways fit between the PSTN and wireless or IP-based networks (Figure 1). Because of the need to reduce costs, engineers are today building media gateways on cost-effective open systems standards such as AdvancedTCA.

At the core of media gateways is an enormous amount of signal processing. This is performed by Digital Signal Processors (DSPs) to provide the traffic interface between the Internet and the wireless network of the PSTN, and to convert Time-Domain Media (TDM) voice to VoIP and back. This process is time-dependent and the system must re-assemble packets in their time-stamped sequence (Figure 2). When packets are missing or late, the media gateway discards and interpolates them. The media compresses voice packets, corrects for jitter, cancels echoes, and generates or recognizes tones.

Packetizing such time-dependent media as voice, wireless, and video data is more complex and requires special processes, such as time stamping. In short, the order in which the time-dependent media IP packets arrive determines their meaning. Without proper sequencing, these packets become unintelligible gibberish, not unlike a sentence made up of randomly generated phonemes that ignore linguistic rules. All ingress and egress data type and formats – including TDM from the RAM, Internal Time-Division Multiplexing across the backplane, TDM, or (AAL2) and Real-time Transport Protocol (RTP) – have time-stamp information associated with each packet and/or cell.

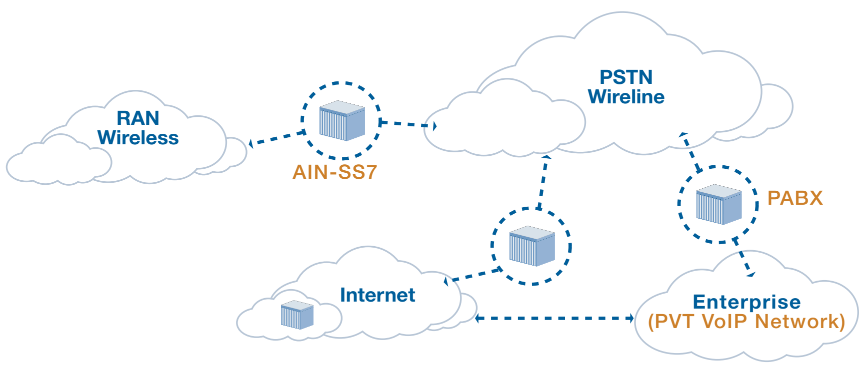


Figure 1

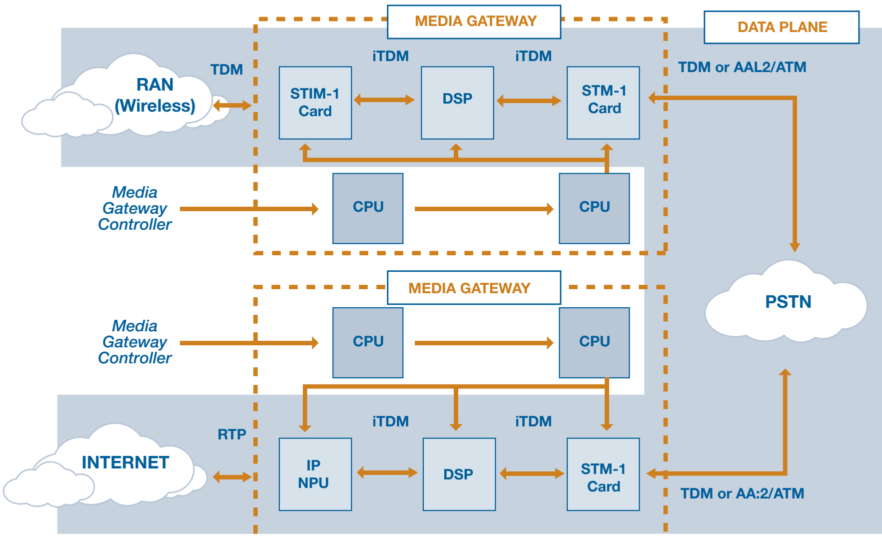


Figure 2

Why modular media gateways for VoIP?

Several market demands are pushing companies to converge all of their media services using media gateways, beginning with VoIP. Companies are expecting this architecture to:

- Lower initial costs. Capital investment is less because hardware can be used for multiple functions.
- Lower development costs. Open system hardware and software standards with well-defined application mean lower costs, and Application Programmable Interfaces (APIs) accelerate development.
- Handle multiple media types. Companies want VoIP solutions today, but need to select solutions that will also handle video in the near future.
- Lower the costs of deployment and maintenance. Standardized, modular systems reduce training costs and maintenance while also improving uptime.
- Enable faster time-to-market. Early market entry hits the window of opportunity and maximizes revenue.

VoIP business issues

The process of selecting a VoIP media gateway platform begins with developers answering several business questions, including:

- What are the business drivers for implementing and providing VoIP?
- Have we determined the immediate and future data capabilities we will need?
- What are the security concerns and challenges for our business?
- What is the expected return on investment from VoIP?
- Have we identified the total cost of ownership including soft cost savings from easier system expansion and updates and reduced cost of space?

Investing in the future

In the past, network applications dedicated separate, often proprietary and costly networks for each application. Modular media gateways' horizontal organization offers the advantage of a common architecture for all applications. Today, media gateways can ensure the inter-working of transactions between different technologies by enabling services for media-based applications involving voice, video, fax, and data.

As a bridge between the PSTN and wireless networks, the media gateway connects to the Radio Network Center (RNC), the Mobile Switching Center (MSC), and the PSTN. Connecting the PSTN and Radio Access Network (RAN) to the Internet requires vendors to design and market less costly, modular, and configurable media gateways that handle more voice and video.

To meet the current and future *dollar-per-port* value needs, media gateway designs should include multicore DSPs and powerful Network Processor Units (NPUs) to distribute data, handle multiple data-transport protocols, increase the number of data ports, and handle more bandwidth. To protect a buyer's investment, this also requires developing media gateways that are flexible enough to scale up from today's 100 megabit networks to 1 gigabit, and even multiple gigabit networks.

Considerations for modular VoIP media gateways

Companies need to answer several questions when considering a media gateway solution.

What solutions are available for the application?

A carrier-grade shelf-and-server platform meeting 5-nines (99.999 percent) performance, and offers expansion capacity to add more processors and edge cards. AdvancedTCA and MicroTCA architectures offer this. A combination of AdvancedMCs in an AdvancedTCA or MicroTCA chassis is also a possible solution.

What is most cost-effective for the application?

This depends on the application's call volume and the need to scale it up or down. AdvancedTCA handles volumes of more than 10,000 calls. MicroTCA will easily handle call volumes of up to 1,000 calls. The advantage of AdvancedTCA is the high density it enables – 8,000 calls or more per slot. However, the same advantage could become a drawback if the requirement is to scale in smaller steps, and potential reliability problems could be associated with such high call volume on a single slot.

To meet the smaller densities, leveraging the modularity of AdvancedMC/MicroTCA could be the better choice. In addition, the media gateway needs to be scaled in 8,000 call blocks, which may be cost-prohibitive in many applications. A mix of AdvancedTCA and AdvancedMC or MicroTCA and AdvancedMC assets offers a more cost-effective solution. The combination approaches use AdvancedTCA or MicroTCA chassis with AdvancedMC cards that handle call volumes of 500 and 10,000 subscribers at one tie. With lower calls per card, it may not be necessary to support one-to-one (2N) redundancy. N+1 or N+N may suffice to deliver the required service quality, thus reducing the overall cost of the system and addressing a higher level of granularity.

Which solution allows better scaling up and down?

Application call volume will determine the approach to take here. Deciding on which of these environments suits your application's market size and your time-to-market deadline must be the first decision made. The market size and call volume may influence your architecture choice, your ability to scale up or down by adding new combinations of cards and chassis, as well as the system cost.

An implementation of a modular media gateway

One example of an application-ready modular media gateway that processes 1,000 channels or more per blade is the RadiSys ATCA-1200 AMC Carrier blade. Based on today's STM-1 card (155.52 mbps capacity) and DSP technology, this design scales up or down easily. In addition to VoIP, these gateways support data, fax, and video moving through the network, including managing TDB sequencing.

RadiSys' typical modular media gateway architecture includes components to address flexibility, scalability, and processing needs.

Figure 3 depicts a media gateway implemented with four AdvancedTCA AdvancedMC carrier blades and the appropriate AdvancedMC cards populating them. The AdvancedMC carrier blade (a) is populated with:

- (a) CPU AdvancedMC running a MEGACO or SIP client
- (b) Carrier blade with DSP AdvancedMC
- (c) Carrier blade with optional E1/T1 to the SS7 network
- (d) Carrier card with STM-1/OC-3 line cards, connecting to the PSTN

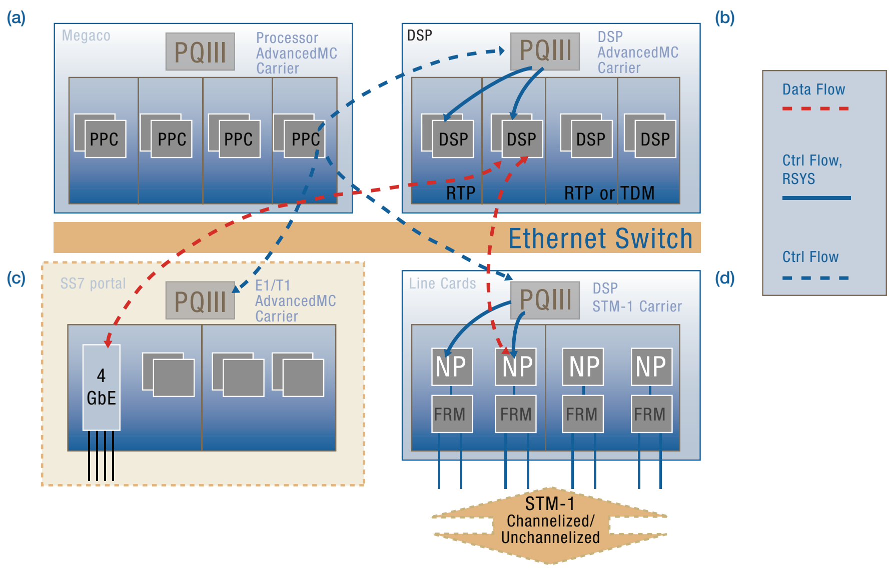


Figure 3

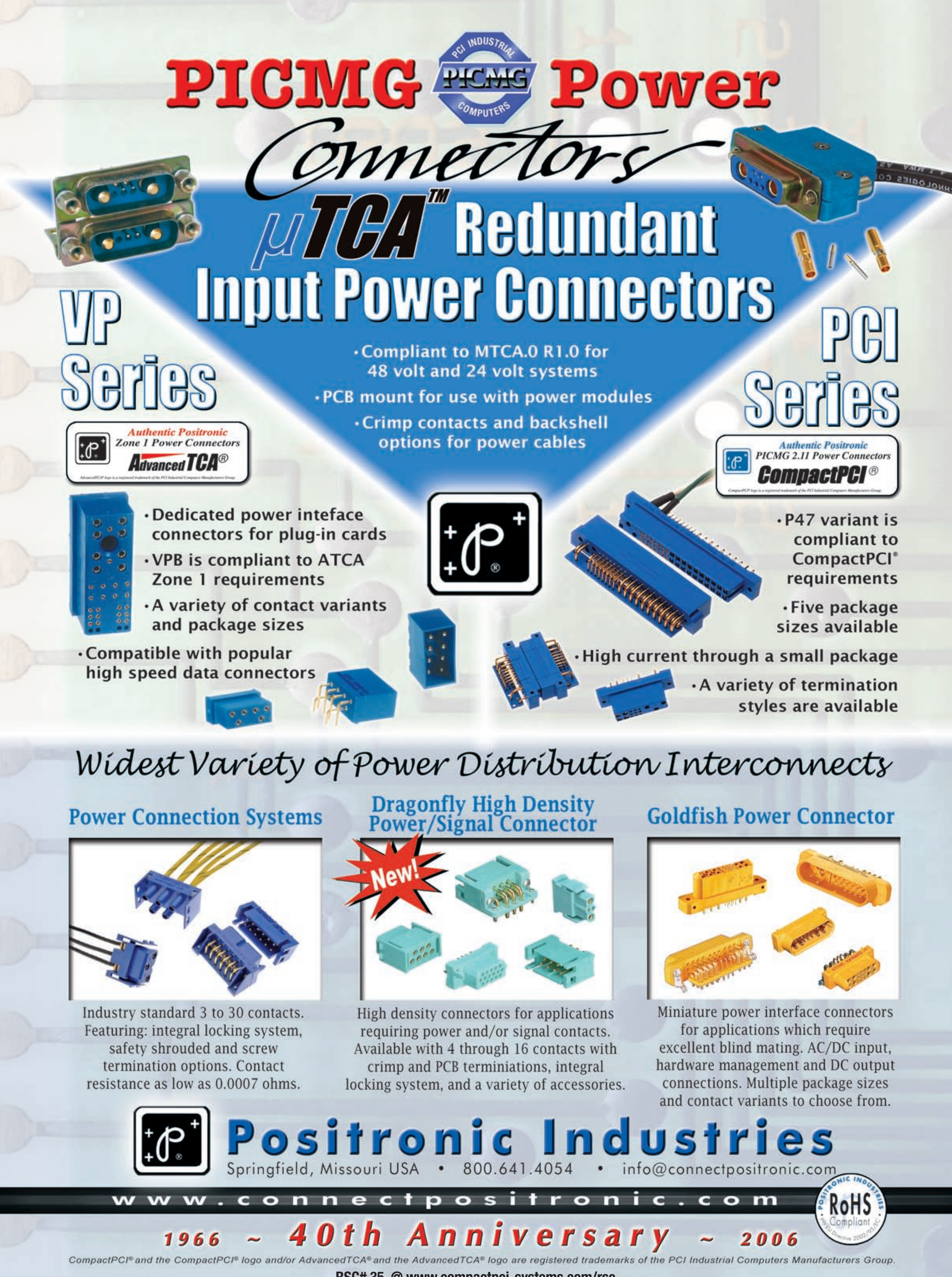
Summary

Today, companies of every size are under pressure to manage costs while increasing workgroup and team interaction to improve productivity. The fundamental factors driving the shift to VoIP and other media services are lower capital costs, reduced operational costs, and improved business processes, especially a company's internal and external communications and collaboration. Integration of media services into the realm of IT is now possible through the use of media gateways.

A standards-based media gateway provides companies with a platform on which to build the converged, content-rich media applications they need – including VoIP – while gaining cost savings, quality, and scalability.

Venkataraman "VP" Prasannan *is the senior director of Product Line Management at RadiSys Corporation.*

RadiSys Corporation
5445 N.E. Dawson Creek Drive
Hillsboro, OR 97124
Tel: 503-615-1100
E-mail: vp@radisys.com
Website: www.radisys.com


PICMG Power
PCI INDUSTRIAL PICMG COMPUTERS
Connectors
μTCA™ Redundant
Input Power Connectors
·Compliant to MTCA.0 R1.0 for 48 volt and 24 volt systems
·PCB mount for use with power modules
·Crimp contacts and backshell options for power cables
VP Series
Authentic Positronic
Zone 1 Power Connectors
AdvancedTCA®
·Dedicated power inteface connectors for plug-in cards
·VPB is compliant to ATCA Zone 1 requirements
·A variety of contact variants and package sizes
·Compatible with popular high speed data connectors
PCI Series
Authentic Positronic
PICMG 2.11 Power Connectors
CompactPCI®
·P47 variant is compliant to CompactPCI® requirements
·Five package sizes available
·High current through a small package
·A variety of termination styles are available
Widest Variety of Power Distribution Interconnects
Power Connection Systems
Industry standard 3 to 30 contacts. Featuring: integral locking system, safety shrouded and screw termination options. Contact resistance as low as 0.0007 ohms.
Dragonfly High Density Power/Signal Connector
New!
High density connectors for applications requiring power and/or signal contacts. Available with 4 through 16 contacts with crimp and PCB terminiations, integral locking system, and a variety of accessories.
Goldfish Power Connector
Miniature power interface connectors for applications which require excellent blind mating. AC/DC input, hardware management and DC output connections. Multiple package sizes and contact variants to choose from.
Positronic Industries
Springfield, Missouri USA • 800.641.4054 • info@connectpositronic.com
www.connectpositronic.com
POSITRONIC INDUSTRIES RoHS Compliant
1966 ~ 40th Anniversary ~ 2006
CompactPCI® and the CompactPCI® logo and/or AdvancedTCA® and the AdvancedTCA® logo are registered trademarks of the PCI Industrial Computers Manufacturers Group.

Liquid-cooled embedded computing initiative

By Tahir Cader, Eric Grabowski, Joe Pavlat, and John Peters

In last month's CompactPCI and AdvancedTCA Systems, *Tahir, Eric, Joe, and John introduced the objectives of the Liquid-Cooled Embedded Computing (LCEC) initiative, a privately funded group tasked with creating an open standard for liquid-cooled embedded computing architectures. Here they detail development of an architecture that deploys liquid cooling for the entire board, also known as full board cooling. This article continues in full at www.compactpci-systems.com.*

The full board cooling solution being developed consists of a number of enclosed boards. Each board is envisioned to be a Line Replaceable Unit (LRU) housed in a common chassis. This system, to be discussed in greater detail, is being targeted to achieve a greater power density than any competitive air-cooled system, and will possess a number of inherent advantages.

In the early system development stages, the LCEC committee recognized a number of key technology risks associated with implementing liquid cooling. As a result, it adopted a two-pronged development approach. The first involves the development of what is called the Static Display Model (SDM). The second approach leverages a prototype system, developed under a Defense Microelectronics Activity (DMEA) program by member company ISR. The second development activity has resulted in a live system that will simply be referred to as the prototype system. The live *prototype system* was developed to address key technology risks, to prove feasibility, and to provide a reference design. Even though the SDM and the prototype systems have some differences, the core engineering development tasks apply to all LRUs that are completely cooled by a dielectric coolant, such as Fluorinert. These core tasks include heat acquisition and rejection and hermetic sealing. In addition, these LRUs must have manufacturability, reliability, and serviceability/maintainability

Static display model

Figure 1 shows the 9U static display model subrack with disassembled enclosure and printed circuit board. It is a nonfunctional mechanical model built as an example of a potential architecture that could be realized from the standard. Building the SDM has provided critical insight into what it will take to create a practical standard, and is playing an important role as the committee works towards a standard.

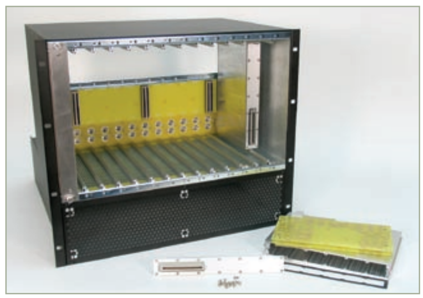


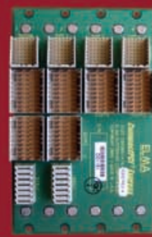
Figure 1

The model is intended to roughly represent key subsystems and their placement with respect to each other, and will serve as a baseline as LCEC members gather marketplace requirements. The SDM aims to achieve a physical representation of the ideal packaging for a liquid-cooled LRU subrack.

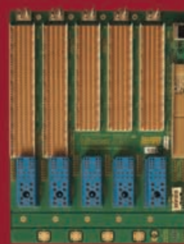
This article continues in full at www.compactpci-systems.com.

"If you would hit the mark,
you must aim a little above it."
-Henry Wadsworth Longfellow

cPCI/2.16



cPCI Express



ATCA

MicroTCA

PICMG compliance is just our starting point

Many in the industry can develop a basic PICMG-compliant backplane. But, with newer technologies like AdvancedTCA, CompactPCI Express, and MicroTCA, you want to go with the leader. We've led the PICMG backplane evolution and with our focus on signal integrity, quality, and innovative design, we'll continue to lead the way. With Elma Bustronic, you get good old-fashioned hard work, perseverance, and a drive for perfection. We don't just meet PICMG specifications, we aim higher.

ELMA BUSTRONIC

Tel: 510.490.7388 www.elmabustronic.com info@elmabustronic.com

RoHS
compliant versions available

ELMA
Your Solution Partner

Clocking in: Real-world MicroTCA needs close clocking/fabric interaction

By Will Chu

In this article, Will briefly surveys MicroTCA architecture and then focuses on four different example systems, with a particular emphasis on the integration of clocks and fabrics in MicroTCA. The example systems are:

- *General purpose computing and software development platform*
- *WiMAX basestation*
- *3G/4G basestation*
- *Quadruple/triple play IP Multimedia System (IMS) platform*

MicroTCA architecture overview

The MicroTCA specification provides system designers with a very flexible architecture. In developing a number of working MicroTCA systems at CorEdge, we found certain applications frequently demanded tight coupling of the MicroTCA clocks and network fabrics, yet the need for this close interaction is often misunderstood.

MicroTCA systems typically consist of the following elements: AdvancedMCs, MicroTCA Carrier Hubs (MCH), MicroTCA Power Modules (PM), and a MicroTCA chassis that comprises a backplane, connectors, and cooling units. The AdvancedMCs deliver specific applications while the remaining elements serve as general purpose infrastructure. The MCH serves as the logical and physical hub for delivering IPMI management (the *Carrier* in MCH) plus networking of common option and fat pipe fabrics and clocking (the *Hub* in MCH). The PM accepts various AC or DC inputs and provides power conversion, distribution, management control, and safety functions. The MicroTCA chassis houses and cools the AdvancedMCs, MCH, and PM. Figure 1 shows the PICMG MicroTCA RC1.0RC2 block diagram.

By intelligently pairing specific types of AdvancedMCs with MCHs that support specific networking protocols and clock types, developers can leverage this generic MicroTCA platform to deploy a wide array of applications. Table 1 summarizes a number of possible AdvancedMC/MCH pairings used for different applications.

For general purpose computing/software development platform MicroTCA systems, there are a number of implementation

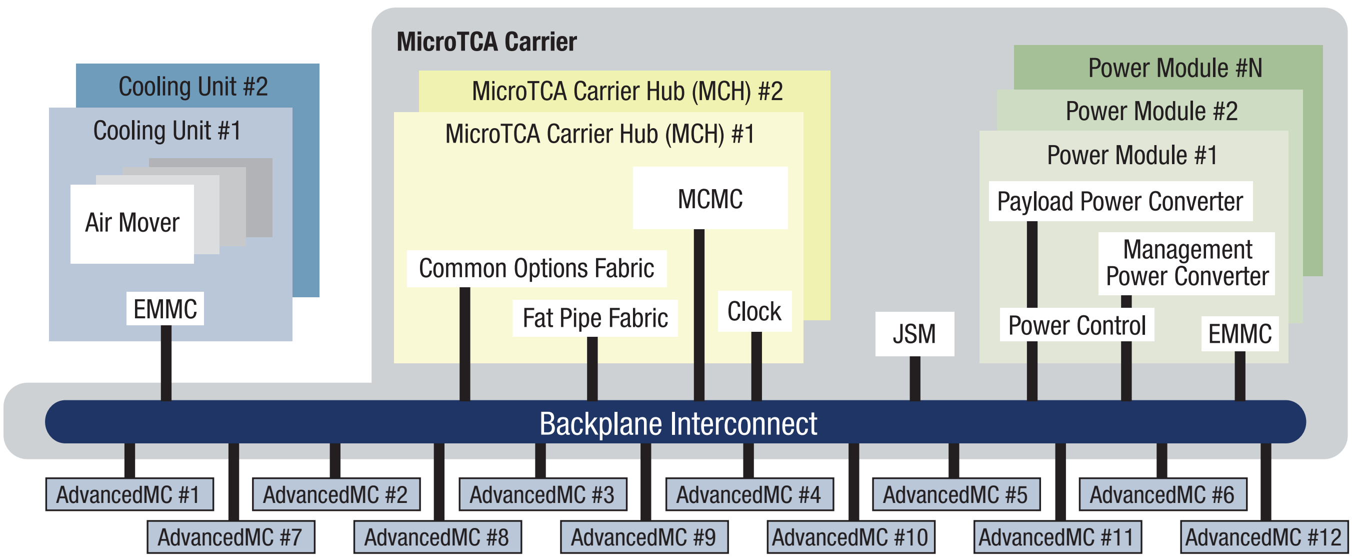


Figure 1

Application	AdvancedMCs	MCH Fabrics	MCH Clocks
General Purpose Computing/Software Development	Processor • Storage • I/O • VGA	1 GbE • SATA/SAS • PCI Express	100 MHz
WiMAX	WiMAX • Processor • Storage	1 GbE	1 PPS/30.72 MHz
3G/4G	DSP • Processor • I/O	1 GbE • Serial RapidIO	8 kHz/19.44 MHz
Triple/Quadruple Play (Voice, Video, Data, Wireless)	10 Gigabit Ethernet Processor • 10 Gigabit Ethernet I/O	1 GbE • 10 Gigabit Ethernet	8 kHz/19.44 MHz

Table 1

options (Table 2). For our first implementation, we used processor, storage, I/O, and VGA AdvancedMCs. A MicroTCA general purpose computing/software development platform using a CorEdge Networks PicoTCA 2UE test and development platform is shown in Figure 2. In this case, the MCH is supplying a 1 GbE fabric between the processor AdvancedMC, I/O AdvancedMC, and the outside world. The MCH supplies a 100 MHz PCI Express oscillator to serve as the master clock domain between the processor and VGA AdvancedMCs. A direct connection on the backplane achieves the PCI Express link between the processor and VGA AdvanceMCs. The MCH supplies a SATA/SAS switch fabric between the processor and storage AdvancedMCs. It is important to note that AdvancedMCs using PCI Express requires a single 100 MHz clock source to enable any PCI Express links. This is a very tight coupling indeed, and highlights the importance of having good clocking support in the MCH.

Figure 2

In future implementations (Table 3), an MCH PCI Express fabric could tie the processor, I/O, and VGA AdvancedMCs into a single PCI Express domain with the MCH 100 MHz PCI Express oscillator.

For a MicroTCA WiMAX basestation (Table 4), the key requirement is support for a 1 PPS clock typically sourced from an external GPS antenna. The MCH generates a 30.72 MHz clock locally that is synchronized to the 1 PPS external clock source and distributes those clocks to the WiMAX AdvancedMCs. Typically the base 1 GbE fabric provided by the MCH has enough bandwidth for the entire system. Some implementations of MicroTCA WiMAX basestations under consideration use a Serial RapidIO fabric in place of the 1 GbE fabric. In this case, an MCH SRIO fabric is required.

For a MicroTCA 3G/4G basestation (Table 5), the key requirement is support for a low latency Serial RapidIO (SRIO) fabric for data transport, 1 GbE fabric for management traffic, and

Modules	MicroTCA Carrier Hub/AdvancedMC Backplane Interfaces				
	CLK1	CLK3	Port 0	Port 2	Ports 4-7
Processor AdvancedMC		MCH CLK1	1 GbE link to MCH	MCH SATA/SAS Fabric	Direct connect to VGA
Storage AdvancedMC		MCH CLK1		MCH SATA/SAS Fabric	
VGA AdvancedMC		MCH CLK1			Direct connect to Processor
I/O AdvancedMC			1 GbE link to MCH		
MCH	Local PCI Express 100 MHz clock source to AdvancedMC CLK3		AdvancedMC 1 GbE Base Channel A	AdvancedMC SATA/SAS Fabric Base Channel B	

Table 2

Modules	MicroTCA Carrier Hub/AdvancedMC Backplane Interfaces				
	CLK1	CLK3	Port 0	Port 2	Ports 4-7
Processor AdvancedMC		MCH CLK1	1 GbE link to MCH	MCH SATA/SAS Fabric	MCH PCI Express Fabric
Storage AdvancedMC		MCH CLK1		MCH SATA/SAS Fabric	
VGA AdvancedMC		MCH CLK1			MCH PCI Express Fabric
I/O AdvancedMC		MCH CLK1	1 GbE link to MCH		MCH PCI Express Fabric
MCH	Local PCI Express 100 MHz clock source to AdvancedMC CLK3		AdvancedMC 1 GbE Base Channel A	AdvancedMC SATA/SAS Fabric Base Channel B	AdvancedMC PCI Express Fabric Base Channel D, E, F, G

Table 3

Modules	MicroTCA Carrier Hub/AdvancedMC Backplane Interfaces				
	CLK1	CLK2	CLK3	Port 0	Port 2
WiMAX AdvancedMC		MCH CLK2	MCH CLK1	1 GbE link to MCH	
Processor AdvancedMC				1 GbE link to MCH	Direct connect to processor
Storage AdvancedMC					Direct connect to processor
MCH	Local 30.72 MHz clock to AdvancedMC CLK3	External 1 PPS GPS clock from face plate to AdvancedMC CLK2		1 GbE Base Channel A with 1 GbE uplinks	

Table 4

potentially 8 kHz/19.44 MHz telco synchronization clocks sourced from an external master system clock. The MCH provides the 1 GbE and SRIO fabric and acts as a clock hub that distributes the incoming telco clocks to the AdvancedMCs.

For a MicroTCA quadruple/triple play IMS platform (Table 6), the key requirement is support for 10 Gigabit Ethernet with advanced flow control and congestion management support throughout the system. IMS networks must handle a massive amount of traffic with precisely controlled quality of service levels. With advanced flow control and congestion management support, both the data and management traffic can be carried across the 10 GbE fabric. This approach obviates the need for additional fabrics, which reduces overall system costs. In an all-Ethernet system, the requirement for synchronization clocks may also be relaxed because advanced flow control and congestion management capabilities coupled with a well-designed packet buffering scheme can provide a user experience and network performance similar to a fully synchronized network.

Implications for MCH design

In looking at these MicroTCA systems examples, it is clear that once you have selected your target applications, you select the appropriate AdvancedMCs and then select an MCH that supports both the application and AdvancedMCs. In a perfect world, a single MCH would support the entire spectrum of potential applications that could be addressed by the MicroTCA architecture. However, in the real world that is impossible. Different applications require different protocols, different bandwidths, and different clocking schemes. One size MCH cannot fit the complete range of requirements. For example, fabric options include:

- 1 GbE as a general purpose fabric for data and management traffic
- PCI Express fabric for processor AdvancedMCs to other peripheral AdvancedMCs (I/O, VGA, others)
- SATA/SAS fabric for processor to storage AdvancedMC communications
- Serial RapidIO fabric for Processor and DSP AdvancedMCs
- 10 GbE fabric for next-generation processor and I/O AdvancedMCs that will use a 10 GbE backplane interface
- Future fabrics

Designers also face a number of clocking choices:

- 100 MHz clock for PCI Express applications
- 1 PPS and 30.72 MHz clock for WiMAX applications
- 8 kHz/19.44 MHz clock for telco applications
- Custom clocking requirements

To handle this broad range of requirements, CorEdge has taken advantage of the multitongue connector architecture in the MicroTCA spec to create a series of modular replaceable clock cards for MCH tongue 2 and different fabric MCH cards for different protocols. This has allowed us to support a wide range of customer application needs, which in turn will be critical for jumpstarting the launching of the MicroTCA market. Figure 3 shows a base MCH with PCI Express/SATA switch module and multitongue plug.

Figure 3

Conclusion

The key take-away for companies wanting to develop complete solutions using MicroTCA is to give careful consideration upfront to the interplay between clocks and fabrics in MicroTCA systems. With proper upfront thinking, MicroTCA applications can be developed relatively efficiently and, in many cases, using many off-the-shelf components including AdvancedMCs and MCHs.

__Will Chu__ is the president of CorEdge Networks, a developer of AdvancedTCA, MicroTCA, AdvancedMC, and IPMI products.

To learn more, contact Will at:

CorEdge Networks, Inc.
50 Commonwealth Avenue, Suite 504
Boston, MA 02116
Tel: 617-267-5205
E-mail: info@coredgenetworks.com
Website: www.coredgenetworks.com

Modules	MicroTCA Carrier Hub/AdvancedMC Backplane Interfaces			
	CLK1	CLK2	Port 0	Ports 4-7
DSP AdvancedMC	MCH CLK1	MCH CLK2	1 GbE link to MCH	MCH SRIO Fabric
Processor AdvancedMC	MCH CLK1	MCH CLK2	1 GbE link to MCH	MCH SRIO Fabric
I/O AdvancedMC	MCH CLK1	MCH CLK2	1 GbE link to MCH	MCH SRIO Fabric
MCH	External 8 kHz clock to AdvancedMC CLK1	External 19.44 MHz clock CLK2	1 GbE Base Channel A with 1 GbE uplinks	AdvancedMC SRIO Fabric Base Channel D, E, F, G w/ SRIO uplinks

Table 5

Modules	MicroTCA Carrier Hub/AdvancedMC Backplane Interfaces	
	CLK	Ports 4-7
10 GbE Processor AdvancedMC with advanced flow control and congestion management support	N/A	MCH 10 GbE Fabric
10 GbE I/O AdvancedMC with advanced flow control and congestion management support	N/A	MCH 10 GbE Fabric
MCH	N/A	AdvancedMC 10 GbE Fabric Base Channel D, E, F, G with 10 GbE uplinks

Table 6

MicroTCA – a new standard for the battlefield

By Rob Persons

Although you may not see specific references to battlefield applications as you peruse this issue's MicroTCA Product Guide*, Rob makes the case here for MicroTCA as a viable architecture for many new military systems such as the Warfighter Information Network – Tactical (WIN-T).*

The rapid and aggressive transformation mandated by the Department of Defense for integrated battlefield management, or the network approach to warfare, has far-reaching influence over military technology development and insertion. The transformation of the battlefield to interconnect war fighters to their command structure and to other war fighters is driving the need for new communications strategies and system architectures that can maximize the amount of Commercial Off-the-Shelf (COTS) content and reuse. Developing high performance military systems that can leverage large economies of scale has been an elusive reality because most current architectures are tightly coupled to the industry that defined the standard. At the same time, maximizing reuse of common nondifferentiating technologies, such as CPU cards and disk modules, has been complex and difficult.

Rapid modernization is only possible when new systems are developed around advanced or superior open standard hardware and software. Not using COTS solutions has become too expensive and slow to combat the heightening global and homeland security requirements. In addition, resources for modernization are limited, so military and federal agencies are looking for new open standard approaches for rapid, cost-effective development and deployment.

The MicroTCA standard based on the Advanced Mezzanine Card (AdvancedMC) was ratified by PICMG in July 2006. Basing MicroTCA on AdvancedMC modules enables the standard's rapid development and adoption. Companies have a framework to develop new network-centric platforms for small network devices that address both telecommunications and battlefield systems.

Network-centric warfare

One effort to modernize the battlefield is a program called Future Combat Systems (FCS), which will improve communications and data connectivity between battalion headquarters and all command structures below, down to the individual soldier. Radio modernization has been underway for several years through the Joint Tactical Radio System (JTRS) program, where a single radio will perform a variety of functions by dynamically changing the waveforms. Rear echelon and maneuvering battalions of the Future Force (FF) will share voice, data, and video on the battlefield through a network developed as part of WIN-T to improve situational awareness for all command structure elements. The network is being designed to be extremely mobile, resilient, and adaptable for many battlefield situations.

Developers are adopting Internet Protocol (IP) based strategies for WIN-T to maximize throughput and flexibility for new devices that are being developed for FCS. Compatibility with the Global Information Grid (GIG) will allow military and civilian leadership direct access to the battlefield from around the world. An emerging standard, World Interoperability for Microwave Access (WiMAX), which is a certification mark for products that conform to the IEEE 802.16-2004 family of standards, along with IEEE 802.11, are two wireless protocols that will be used along with other standard IP protocols to improve data throughput in the field. Sprint has recently announced it will deploy a WiMAX network to support 4G wireless phones for making broadband data performance to the phone possible.

Network-centric system architectures

MicroTCA leverages the emerging ecosystem for AdvancedMCs to create a new, flexible, small form factor platform, enabling a variety of system configurations to be created. The MicroTCA specification allows for modular or monolithic chassis configurations from 1 carrier and 1 module to 16 carriers and 192 modules, while ensuring that modules always see the same *virtual* environment. These MicroTCA communications servers, such as the Motorola Centellis 1000 communications server (Figure 1), typically support 2 to 3 independent fabric interconnects on a carrier, where each fabric *port* (differential transmit/receive pairs) is capable of at least 6.25 Gigabaud (5 Gbps) in each direction, and specific ports can be aggregated to form *fat pipes* with higher throughput.

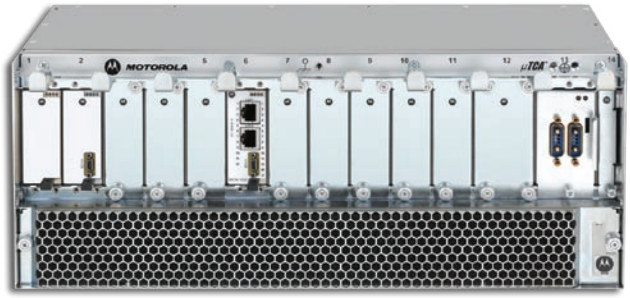


Figure 1

Systems like the Centellis 1000 will support three different fabric protocols simultaneously in a chassis: Gigabit Ethernet, PCI Express, and Serial ATA. The current aggregate carrier (switched backplane) bandwidth is around 40 Gbps, but next generation hubs should exceed this. The MicroTCA specification allows for up to 12.5 Gigabaud per port.

Migration of existing I/O PMCs to the AdvancedMC form factor is straightforward because PCI Express is an extension of standard PCI. PCI Express maintains backward software compatibility to PCI so that drivers and operating system software can be reused. PCI to PCI Express bridges can be incorporated on an

AdvancedMC, allowing reuse of existing PMC card designs. As new controllers are released with PCI Express, MicroTCA can add this new functionality while maintaining more traditional I/O or custom PCI based designs in the same chassis. Also, migrating to a switched serial architecture like PCI Express eliminates the *slowest link* limitations[1].

Applying MicroTCA to WIN-T

Referred to as WirelessMAN or Wireless Metro Area Network, IEEE 802.16-2004 was developed to promote wireless broadband services to the *last mile,* the connection from the street to the home. Operating frequencies in the original 802.16 specification were from 10 GHz to 62 GHz and expanded to include 2 GHz to 11 GHz frequencies with 802.16-2004, though the frequencies will be relegated to licensed frequencies of 2.5 GHz to 2.69 GHz and 3.4 GHz to 3.6 GHz and unlicensed spectrum 5.725 GHz to 5.850 GHz. In late 2005, 802.16e was added and included Orthogonal Frequency-Division Multiplexing (OFDM), where a single transmitter transmits on many (typically dozens to thousands) different orthogonal frequencies, that is, frequencies that are independent with respect to the relative phase relationship between the frequencies[2]. OFDM improves the performance of this wireless protocol, reduces interference between devices, and allows for Non Line Of Sight (NLOS) operation. The IEEE 802.16 standard also utilizes scheduling algorithms that gives all subscribers a controlled access to the network and allows for quality of service control of network traffic.

Army programs are interested in WiMAX because it has been designed to deliver broadband data performance both for fixed and mobile devices. Dynamic creation and maintenance of these mobile networks along with Quality of Service (QoS) that will allow true battlefield situational information between the rear echelon and the advancing troops. WiMAX AdvancedMC modules will be available in the future, and MicroTCA will be the platform architecture best suited for deploying it into the field.

Rugged MicroTCA

Working closely with Motorola, Hybricon has developed a ruggedized MicroTCA ATR chassis that leverages Motorola's commercial MicroTCA platform, while also accommodating double-width modules (Figure 2). The ruggedized ATR platform remains compliant with the MicroTCA specification, and addresses many of the limitations of commercial MicroTCA for military applications:

- The ruggedized ATR chassis uses shock isolation of the MicroTCA card cage inside the ruggedized ATR chassis; this attenuates the level of shock and vibration that is seen by the MicroTCA cards, allowing the chassis to meet stringent MIL-STD-810 shock and vibration requirements
- Military circular connectors for copper and fiber I/O are used to meet military ruggedization requirements for external connectors
- A secondary EMI barrier is used, in addition to aggressive power line filtering, to meet stringent MIL-STD-461 EMI/EMC requirements
- The ruggedized ATR chassis uses the MicroTCA specification's optional locking provisions, to firmly retain the MicroTCA cards into the card cage, providing significant additional resistance to shock and vibration
- Military power supply front ends can be used to meet specific military power supply requirements such as MIL-STD-704 aircraft power or MIL-STD-1275 vehicle power

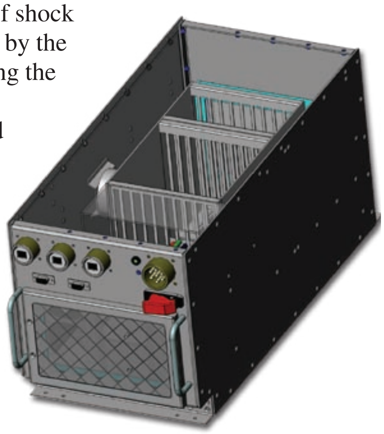


Figure 2

The specifications of the AdvancedMC and MicroTCA cards that are used in a particular application are the limiting factor in determining the system's operating temperature range. Commercial AdvancedMC and MicroTCA cards can satisfy less stringent military temperature ranges. Ruggedized and/or extended temperature range AdvancedMC and MicroTCA cards may be required in some applications. This is similar to the existing VME and CompactPCI form factors.

Rugged MicroTCA enclosures with adapted AdvancedMC modules will allow for a more flexible deployment of new network centric technologies to the battlefield. Adoption of PCI Express and Gigabit Ethernet as the base fabrics of MicroTCA will reduce the complexity of migrating critical military I/O to AdvancedMC form factors and help quickly ramp up the availability of necessary I/O. New AdvancedMCs that can deliver the new wireless technologies to the battlefield are the same technologies that will be used in the next generation mobile phones with high-speed broadband capabilities. But it is the efforts of companies investigating the ruggedization of commercial AdvancedMCs that will help the military utilize truly COTS hardware in the battlefield that is also being deployed in civilian applications.

Summary

MicroTCA has the same potential as VME did 25 years ago to become the standard for multiple industries. Many of the telecommunication industry's COTS advancements will finally unite with the network initiatives found in medical, military, and aerospace to drive true COTS rapid insertion of cost-effective, ubiquitous, high performance, flexible, and scalable platforms.

References

[1] Bringing up to PCI Express from PCI, Intel Corporation White Paper, http://download.intel.com/design/bridge/papers/25375501.pdf

[2] Orthogonal frequency-division multiplexing, Wikipedia, http://en.wikipedia.org/wiki/Orthogonal_frequency-division_multiplexing

***Rob Persons** is a field applications engineer at Motorola Embedded Communications Computing.*

To learn more, contact Rob at:

Motorola Embedded Communications Computing
2900 S. Diablo Way DW205
Tempe, AZ 85282
Tel: 407-699-7129
E-mail: rob.persons@motorola.com
Website: www.motorola.com/computing

MicroTCA offers a direct solution for tight cost and size restraint applications

By Stuart Jamieson

Stuart describes the benefits telecom OEMs can realize by taking advantage of the MicroTCA form factor, which enables AdvancedMC modules to be plugged directly into a backplane, without the need for an AdvancedTCA carrier.

Telecom Equipment Manufacturers (TEMs) and Network Equipment Providers (NEPs) are very excited about the new capabilities provided by AdvancedTCA, AdvancedMC, and MicroTCA, also often referred to collectively as xTCA. TEMs and NEPs must upgrade their basic architecture to respond to the exploding demand for new telecom, networking, and entertainment services and features, as well as a tidal wave of new subscribers and users. Within a few years, billions of new users from emerging countries like India and China will also be demanding these solutions.

Because of this demand, almost every major telecom equipment manufacturer and network equipment provider is looking at some flavor of xTCA for the next generation of telecom infrastructure.

Telecom analyst VDC (Framingham, Massachusetts) forecasts a $1.15 billion total market for merchant AdvancedTCA blades by the end of 2009, and a $763 million dollar market for AdvancedMCs. This bodes well for MicroTCA, which is largely an extension of these two platforms. VDC is already projecting that the market for integrated MicroTCA systems encompassing chassis, power, fans, and MicroTCA Carrier Hubs (MCHs) will grow to about $217 million in 2009. Emerson's own preliminary market estimates indicate that the total available market for MicroTCA platforms will reach $900 million in 2008, growing to $3.3 billion in 2010.

High-performance roots

In late 2001, under the auspices of PICMG, component suppliers, TEMs, and service providers from throughout the world came together to define a new open architecture platform for packet-based telecom infrastructure applications. The platform adopted in 2003, AdvancedTCA, combined a large form factor and high power capability with a hot swappable, multiprotocol switched fabric that made it ideal for packet based telecom systems of high performance, density, and availability.

In 2005, PICMG released a complementary new mezzanine standard for AdvancedTCA. Known as AdvancedMC (PICMG AMC.0), the new mezzanine interface enhanced AdvancedTCA's flexibility by extending its high-bandwidth, multiprotocol interface to individual hot swappable modules. Together, AdvancedTCA blades equipped with AdvancedMC modules gave telecom OEMs a versatile platform for quickly building modular telecom systems that could be designed, outsourced, manufactured, scaled, upgraded, and serviced with a finer degree of granularity at a much lower cost.

A direct connection

MicroTCA reduces cost and size by enabling telecom OEMs to plug AdvancedMC modules directly into a backplane. No AdvancedTCA carrier is necessary. This backplane environment, which supports a variety of flexible packaging options, enables telecom OEMs to utilize standard off-the-shelf Advanced modules. What's more, OEMs can leverage existing AdvancedTCA/AdvancedMC switching, protocol, and Intelligent Platform Management Interface (IPMI) infrastructure, thereby helping them to preserve their investment in existing shelf management and application software. This combination of flexibility and synergy makes MicroTCA an excellent complement to AdvancedTCA/AdvancedMC for small form factor central office and outside-plant applications, including wireless basestations, digital loop carriers, optical ADMs, and Fiber to the Curb optical network units.

MicroTCA architecture

MicroTCA is in some respects a repackaging of the modular AdvancedTCA/AdvancedMC fabric. In effect, the MicroTCA enclosure acts as a virtual AdvancedTCA carrier, emulating the AdvancedTCA carrier environment specified in AMC.0. MicroTCA backplanes support star, dual star, and full mesh topologies. MicroTCA backplane communications are also protocol agnostic, supporting a variety of packet-based protocols, including Ethernet, PCI Express/AS, and Serial RapidIO.

The foundation for the MicroTCA chassis is the MCH, which provides the switched fabric, clock distribution, and shelf management functions needed to support up to 12 AdvancedMC modules. See Figure 1. The MCH module acts as a star hub, providing a central switch and high-speed lanes to each module. Adding a second MCH to the MicroTCA enclosure creates the dual star topology required for reliability. Utilizing the same serial transport mechanism as AdvancedMC, the MCH provides a scalable bandwidth of up to 12.5 Gbps per channel, and an aggregate bandwidth of up to 612 Gbps per MCH.

MicroTCA backplanes provide redundant I2C-based IPMI, which enable shelf management to monitor and control each module installed in the backplane. The IPMI Module Management Controller (MMC) on each AdvancedMC module gathers information for temperature, voltage, and other parameters that are deemed vital to the module's normal operation and conveys them to shelf management.

MicroTCA shelves will be able to accept any standard AdvancedMC module in a variety of form factors, including:

- Half-height/single-wide
- Half-height/double-wide
- Mid-size/single-wide
- Mid-size/double wide
- Full-height/single-wide
- Full-height/double-wide

A typical high-availability shelf could combine redundant MCHs and power modules with up to 12 AdvancedMC modules. MicroTCA shelves will take power from an AC main or traditional -48 VDC telecom source, and convert it to 12 V for delivery to individual AdvancedMC modules.

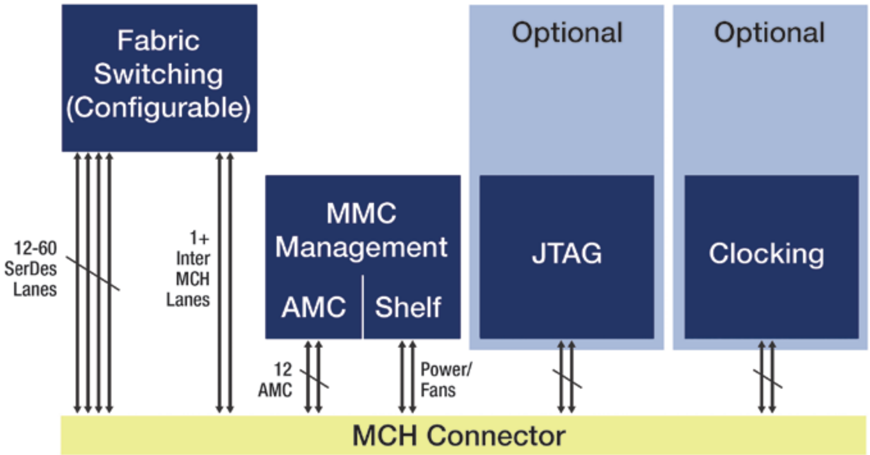


Figure 1

Versatile packaging

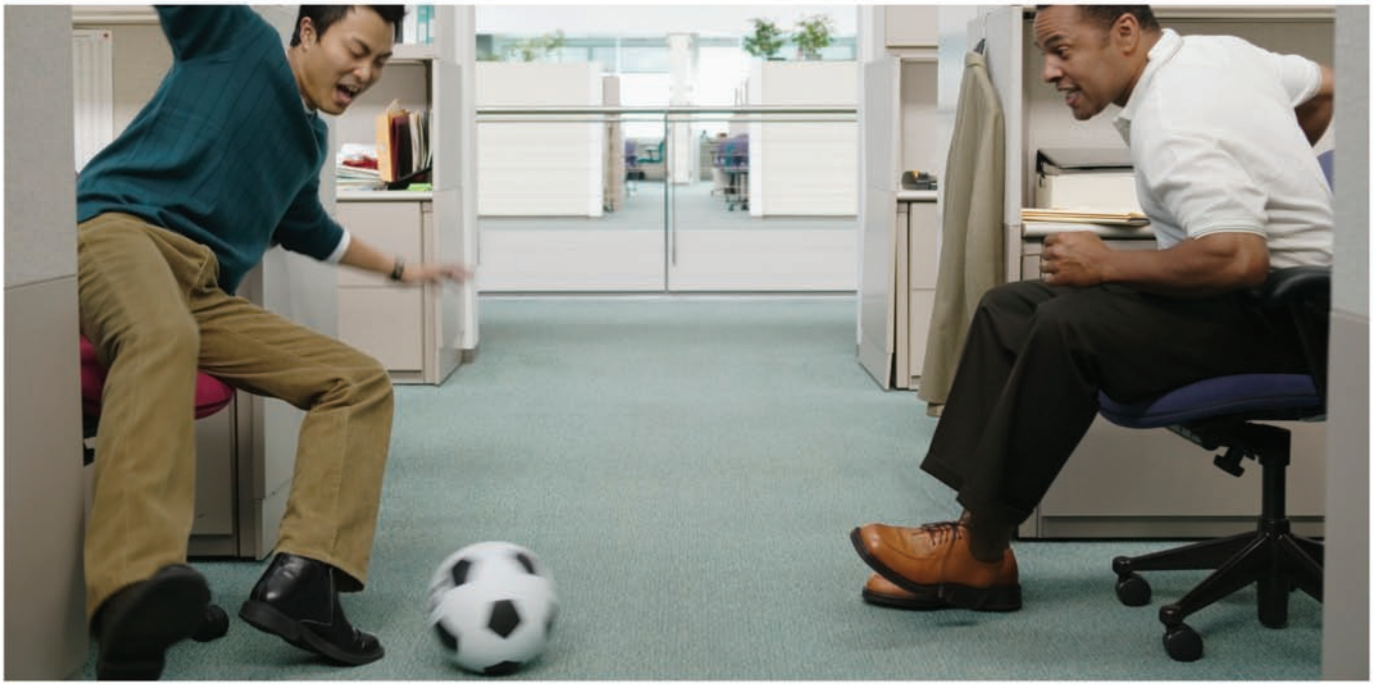
The MicroTCA specification suggests a number of packaging options, but does not define one as part of the spec. The suggested 19-inch rack-mount MicroTCA chassis, for example, would range from 2U to 6U and measure just 300 mm deep (including cabling), a key requirement for many optical applications. To accommodate more irregular outside plant, pole-mounted environments, work is underway to make the MicroTCA chassis available in a cube configuration, which measures 8 inches wide by 8 inches high by 200 mm (roughly 8 inches) deep. Cubes can be used in a standalone mode. They can also be assembled into two-dimensional arrays and installed in a standard rack.

MicroTCA enclosures are not limited to standard shelves or cubes. AdvancedMC's compact size enables MicroTCA enclosures to be used in a variety of space-constrained applications where only a few modules (pico assemblies) are needed to complete a system. Alternatively, MicroTCA enclosures can also be used to build large-capacity systems with hundreds of AdvancedMC modules.

Summary

MicroTCA is the first open shelf architecture to meet the cost, performance, and availability requirements of emerging low- to mid-range wireline and wireless telecom applications. Equally important, it does so in a way that leverages existing AdvancedTCA and AdvancedMC infrastructure, enabling TEMS to preserve

GE Fanuc
Embedded Systems



We can save you time. How you spend it is up to you.

With 50+ single board computers to choose from, we probably have what you're looking for.

Finding exactly the right single board computer can be a time-consuming task, but it can be lot simpler when you start your search at GE Fanuc Embedded Systems. We have such a vast selection that you're likely to find what you're looking for, no matter what the form factor, processor, ruggedization level, I/O or configuration.

This PICMG® 2.16 compliant computer, for example, offers 3 Gigabit Ethernet ports, 16 programmable GPIO ports, a 167 MHz MPX system bus, and gives you the choice between a 1 GHz or a 1.4 GHz Freescale™ PowerPC® G4 processor. It can be ordered with convection or conduction cooling, and it's just one of a dozen of our off-the-shelf cPCI single board computers, most of which are available in multiple configurations.

We not only offer you cPCI in 3U and 6U, Intel® or PowerPC with convection or conduction cooling, we also have a range of VME, PMC and AdvancedTCA® and AdvancedMC™ processor boards. Take a look at our selection. We've spent a lot of time pulling it all together so you don't have to.

www.gefanucembedded.com

C2K
High Performance
PICMG 2.16
6U CompactPCI®
PowerPC Embedded
Computer

GE FANUC

CONDOR ENGINEERING

SBS Technologies.

Now a part of GE Fanuc Embedded Systems

MicroTCA demonstration

PICMG has completed putting the finishing touches on a new small form factor open architecture telecom platform that addresses central office, outside plant, and last-mile access applications with tight size and cost constraints. Released in July 2006 MicroTCA enables AdvancedMC modules to be used directly in a variety of compact, low-cost enclosures without the need for an AdvancedTCA carrier. At SUPERCOMM 2005, PICMG performed the first physical MicroTCA demonstration using a 2U rack based system equipped with five Emerson Pentium M-based AdvancedMC modules.

At the 2006 3GSM show, Emerson took MicroTCA to the next level, demonstrating a turnkey 12-slot MicroTCA system for evaluating and developing wireless base station (WiMAX and 3G), IP Multimedia Subsystems (IMS), MSPP, and IPPBX applications. The system was equipped with KosaiPM payload modules, an MCH module, power supply, fat pipe switch module, application/protocol processing, and platform management software, all developed by Emerson.

At the recent GLOBALCOMM event, Emerson demonstrated a variety of multimedia and telecom applications using its new 12-slot MicroTCA development system, which is equipped with a MicroTCA Carrier Hub (MCH) module, power supply, Fat Pipe switch module, application/protocol processing, and platform management software (Figure 2). In one of the demos, Emerson KosaiPM AdvancedMC modules, plugged directly into the MicroTCA chassis, performed application hosting with Surf Communication Solutions AdvancedMC modules handing the IMS video streaming and videoconferencing. In a second demo, a KosaiPM module (Figure 3) running Linux from a hard drive performed videoconferencing.

Figure 2

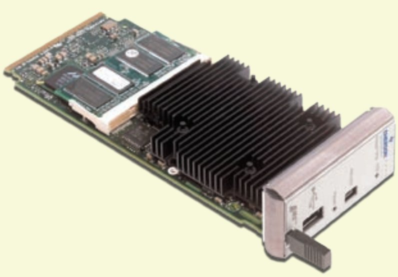


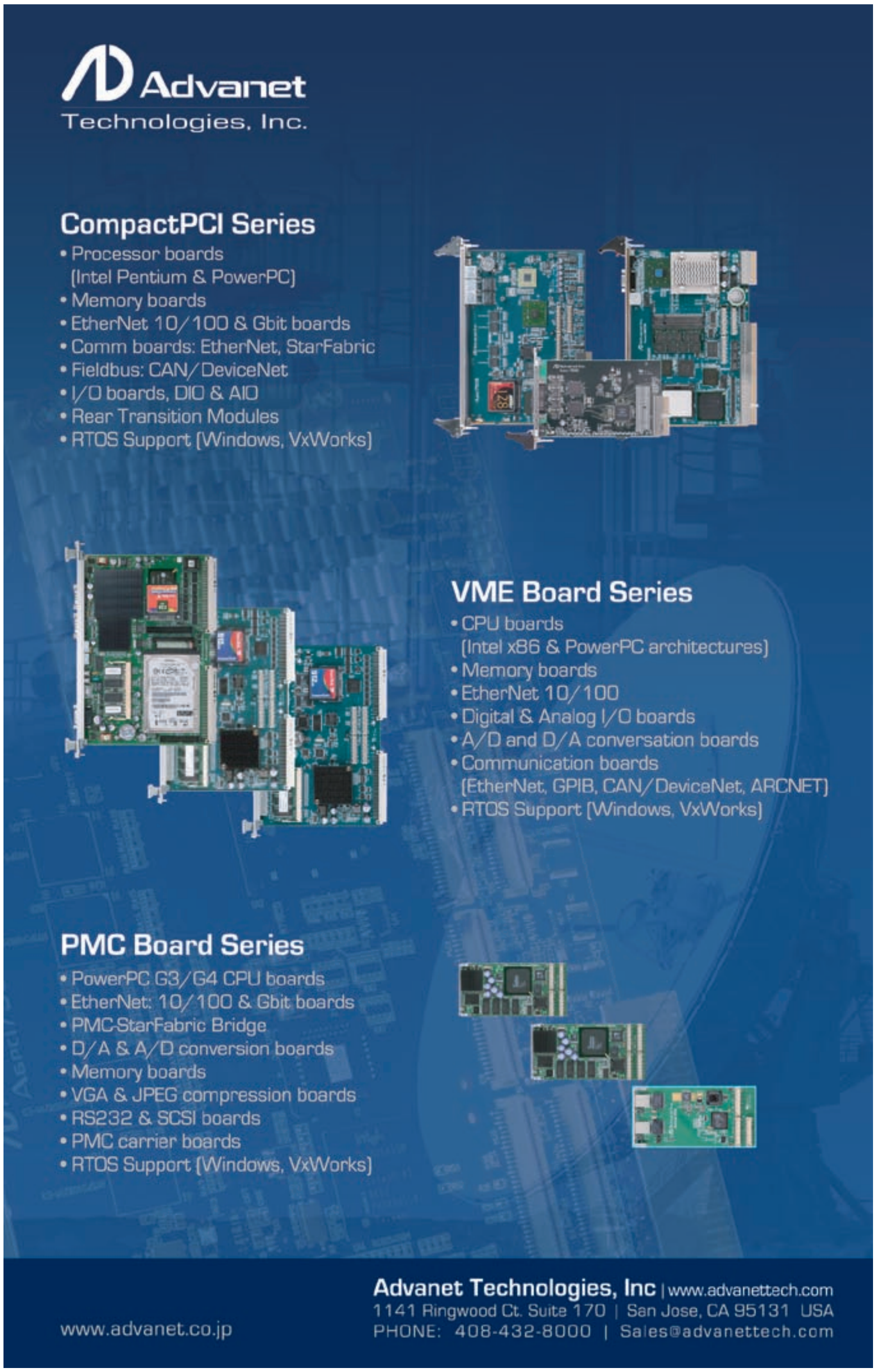
Figure 3

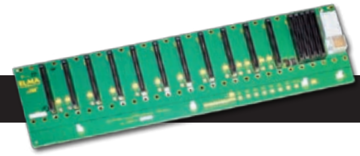
their investment in existing software while giving them easy access to off-the-shelf AdvancedMC modules.

__Stuart Jamieson__ is director of advanced technology with Emerson Network Power.

To learn more, contact Stuart at:

Emerson Network Power
Suite 4, 2 Anderson Place
Edinburgh EH6 5NP UK
Tel: 44-131-475-7012
Fax: 344-131-475-7001
E-mail:stuart@artesyncp.com
Website: www.artesyncp.com

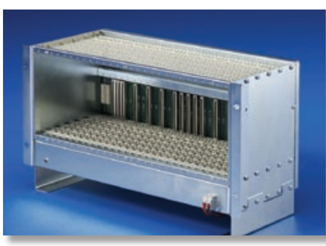




COMPANY NAME	DESCRIPTION
Carlo Gavazzi CS	**www.gavazzi-computing.com**
6862 Series 1U MicroTCA Starter Kit	A complete AdvancedMC and MicroTCA development system • 1.75-inch (1U) (H) x 10.3-inch (W) x 7.7-inch (D) • MicroTCA backplane supports AMC.0, AMC.1, AMC.2, AMC.3, AMC.4 • IPMI system manager creates a MicroTCA-like environment
CorEdge Networks, Inc.	**www.coredgenetworks.com**
AMC Mechanicals	Complete suite of mechanicals for AdvancedTCA AdvancedMCs, AdvancedTCA carrier cards, and MicroTCA Carrier Hubs • Have passed rigorous NEBS Level 4 shock, vibration, and seismic tests (industry first) • Available as a suite or a la carte
CEN-MCH	MicroTCA Virtual Carrier Manager Controller that has been proven to support multivendor MicroTCA systems at numerous open interoperability workshops • High performance IPMI management and multiprotocol networking support
CEN-MCHv2.7	MicroTCA Carrier Hub (MCH) designed to the PICMG MicroTCA v1.0 specification • Serves as the logical and physical hub for delivering management, clock, and fabric connectivity of AdvancedMC-centric MicroTCA systems
CEN-MPWR	Power Entry Module designed to the MicroTCA v0.95 specification • Supports an IPMI interface to the CorEdge Networks MicroTCA Carrier Hub
CEN-MTCv1.0	Small, self-contained chassis-based test system that supports testing of multiple AdvancedMCs • Supports 2 AdvancedMCs with integrated shelf management • Supports 1 MicroTCA Carrier Hub and 1 AdvancedMC to simulate a MicroTCA system
CEN-PICO-1UR	PicoTCA/MicroTCA/AdvancedMC development system with RTM customizable to support various I/O interfaces and provide I/O access to all 21 AdvancedMC ports • MicroTCA midplane supports AMC.0, AMC.1, AMC.2, AMC.3, AMC.4 specifications for one AdvancedMC (single or double wide)
CEN-PICO-iUS	PicoTCA/MicroTCA/AdvancedMC 1U standalone test and development system • Cross-connected MicroTCA backplane supports one double wide or two single wide AdvancedMCs and AMC.0, AMC.1, AMC.2, AMC.3, AMC.4 specifications
MicroTCA MCH Hub	MicroTCA Carrier Hub (MCH) card that controls multiple AdvancedMC cards in a MicroTCA chassis • Flexible front panel I/O options including telco alarms, Ethernet, and various serial interfaces
MicroTCA MCH Hub v3	MicroTCA Carrier Hub (MCH) card that controls multiple AdvancedMC cards in a MicroTCA chassis • High performance IPMI management and multiprotocol networking support
ELMA Bustronic	**www.elmabustronic.com**
14-Slot MicroTCA	14-slot backplane that complies to MicroTCA.0 Rev 1.0 • High speed connector up to 6.25 Gbps and slot-to-slot aggregate bandwidth of 5,000 MBps
ELMA Electronic	**www.elma.com**
MicroTCA 4U System	19" rack-mount, compliant to MicroTCA 1.0 • Single star backplane accepts 12 AdvancedMC modules
MicroTCA 7U Cube Development System	19" rack-mount, compliant to MicroTCA 1.0 Draft 0.9 • Dual star backplane • 2 MicroTCA Carrier Hubs (MCH) • 2 redundant power modules • 6 AdvancedMCs, Single width/full height
MicroTCA 7U System	19" rack-mount, compliant to MicroTCA.0 Rev. 1.0 • Single star backplane accepts 12 AdvancedMC modules

COMPANY NAME	DESCRIPTION
MicroTCA Dual Star Backplane	Single-width, full-height dual star backplane with two MicroTCA Carrier Hubs (MCHs) and two redundant power modules • 6 AdvancedMCs
Emerson Network Power	**www.artesyncp.com**
KosaiPM AMC card	Half-height AdvancedMC for adding control and packet processing performance to small form factor MicroTCA systems and low-profile custom carrier blades equipped with AdvancedMC sites • Hot-swappable, Pentium-based card suitable for control plane processor for optical and wireless infrastructure
MicroTCA Development Platform	Open frame 19" rack-mount chassis with tabletop cabinet • 12 single-wide content slots with a combination of 6 full height and 6 half height AdvancedMC modules or 9 full height AdvancedMC • A MicroTCA Carrier Hub (MCH) module with dual front panel 10/100/100 Ethernet ports
Harting	**www.harting.com**
AMC pressfit connector for MicroTCA	AdvancedMC connector for MicroTCA backplanes, selected by PICMG for inclusion in the new standard • Suitable for routing without the need to use blind or buried vias
Interphase	**www.interphase.com**
iSPAN 3632 AMC	MicroTCA ready AdvancedMC for next-generation media gateways, basestation controllers, and radio network controllers • Quad-Port channelized single-width, single-height module OC-3/STM-1 interface processor used to support integration with TDM telecom interfaces in the network
iSPAN 36NP AMC	MicroTCA ready network processor card is a single-width, single-height AdvancedMC packet processing engine designed for use with deep packet inspection, packet forwarding, and packet switching applications • Intel IXP2350 packet processor
Kaparel	**www.kaparel.com**
AdvancedTCA Enclosure Family	Systems up to Level 5 for AdvancedTCA and MicroTCA • Everything is fully assembled, ready to run and individually configured • Case solutions in 5U, 12U, 13U, or cube design
Linear Technology	**www.linear.com**
LT4351	MicroTCA MOSFET diode OR controller • Low-cost replacement for ORing diode in multiple power supply applications
LTC4221	MicroTCA dual hot-swap controller with a dual-level circuit breaker • Allows safe board insertion and removal from a live backplane
Motorola	**www.motorola.com/computing**
Centellis 1000	MicroTCA open application-enabling platform • Integrated and verified hardware and software components • Physically smaller, with finer-grained scalability than communications servers based on the AdvancedTCA industry standard
Performance Technologies	**www.pt.com**
AMC111	Single width, full-height single board compute module for AdvancedTCA and MicroTCA systems • 64-bit single core AMD Turion 2.0 GHz processor
AMC131	Single width, full-height 32-bit AdvancedMC compute module designed for AdvancedTCA and MicroTCA systems • Freescale Dual Core 1 GHz vMPC8641D PowerPC Processor

COMPANY NAME	DESCRIPTION
PMC-Sierra	**www.pmc-sierra.com**
PM6352 RSE 160	Carrier-class 16-port Serial RapidIO switch capable of scaling up to 10 Gbps per port that is suitable for AdvancedTCA- and MicroTCA-based wireless infrastructure platforms • Protection and diagnostic features for carrier grade applications
Positronic Industries	**www.connectpositronic.com**
MicroTCA Input Power Connectors	The "QB" Series meets requirements of the MicroTCA Specification for 48 V and 24 V systems • Board mount connectors for power modules and cable connectors for bringing power to modules.
Rittal	**www.rittal.com**
MicroTCA system	MicroTCA system that accommodates AdvancedMC cards • 2U, 3U, and 5U (high) configurations • Built-in fan aids shelf cooling to keep AdvancedMCs cool in 3U and 5U versions
SANBlaze Technology	**www.sanblaze.com**
SB-AMC-HD	A drive carrier module for AdvancedTCA or MicroTCA systems • Configured with either one 2.5 inch SATA or one SFF SAS drive
Schroff	**www.schroff.us**
6U MicroTCA Development System	6U, 316 mm deep ratiopac PRO case with front handles • Card cage for single width, full-height AdvancedMC modules • 14-slot MicroTCA backplane (two power module slots, two MCH slots, 10 AdvancedMC slots) or 16-slot (two power module slots, two MCH slots, 12 AdvancedMC slots)
8U MicroTCA Development System	8U, 316 mm deep ratiopac PRO case with front handles • Card cage for double width, full-height AdvancedMC modules • 14-slot MicroTCA backplane (two power module slots, two MCH slots, 10 AdvancedMC slots) or 16-slot (two power module slots, two MCH slots, 12 AdvancedMC slots)
Tyco Electronics Power Systems	**www.tycoelectronics.com**
MicroTCA Backplane Connector	Press-fit through-hole and surface mount configurations • Designed for high-speed differential pair applications (12.5+ Gbps)
MicroTCA Power Connector	24 individual 15 Amp power contacts • 72 individual high density signal contacts • All contacts stamped and formed
Yamaichi Electronics	**www.yeu.com**
AdvancedMC BackPlane Connector	Compression technology reduces number of layers • Highest signal speed capability beyond 12.5 Gbps with GR-1217-CORE compliant reliability
CN080 Series Connector	Compliant to MicroTCA with highest speed perfomance beyond 12 Gbps • GR-1217-CORE and RoHS compliant
VCM Plug Connector	MicroTCA and GR-1217-CORE compliant • Available in 1, 2, 3, or 4 (all) tongues • Solves tolerance stack up problem between aggregate backplane connectors



CompactPCI® and AdvancedTCA® Systems

ADVERTISER INFORMATION

Page/RSC#	Advertiser/Product description
9	ADLINK Technology – AdvancedTCA Products
47	Advanet – CompactPCI, VME, PMC Series
52	Arrow Electronics – MicroTCA Communication Servers
16	Az-Com – Quality Extenders
49	Concurrent – Intel Based SBCs
2	Conec – AdvancedTCA Zone 1 Power Connectors
7	Diversified Technology – ATCA Blades
37	Elma Bustronic – PICMG Compliant Backplane
15	Elma Electronics – Handles and Panels
39	Embedded Planet – System Creation
3	Emerson Network Power – Communication Products
13	Excalibur Systems – Avionics Communications
46	GE Fanuc Embedded Systems – SBCs
5	GE Fanuc Embedded Systems – Embedded Products
33	Hartmann Elektronik – CompactPCI Backplanes
21	Kontron – Open Modular Solutions
20	N.A.T. – µTCA, MCH, AMC products
23	National Instruments – High-Speed Digital I/O
24	One Stop Systems – CompactPCI Express
11	Performance Technologies – CPC5564 64-Bit AMD Opteron SBC
50	Performance Technologies – Advanced Managed Platforms
35	Positronic Industries – MicroTCA Input Power Connectors
25	Radian Heatsinks – Low profile heat sinks
51	RadiSys Corporation – AdvancedTCA Solutions
36	Red Rock Technologies – Mass Storage Modules
27	Schroff – Hybrid Serial Parallel Cooling
45	Simon Industries – Conduction-Cooled Heat Frames
6	TEWS Technologies – Embedded I/O Solutions
17	Winchester Electronics – Signal and Power Connectors

OpenSystems Publishing

Advertising/Business Office

30233 Jefferson Avenue
St. Clair Shores, MI 48082
Tel: 586-415-6500 ■ Fax: 586-415-4882

Vice President Marketing & Sales
Patrick Hopper
phopper@opensystems-publishing.com

Business Manager
Karen Layman

Sales Group

Dennis Doyle
Senior Account Manager
ddoyle@opensystems-publishing.com

Tom Varcie
Account Manager
tvarcie@opensystems-publishing.com

Doug Cordier
Account Manager
dcordier@opensystems-publishing.com

Barbara Quinlan
Account Manager
bquinlan@opensystems-publishing.com

Andrea Stabile
Advertising/Marketing Coordinator
astabile@opensystems-publishing.com

Christine Long
E-marketing Manager
clong@opensystems-publishing.com

Regional Sales

Jane Hayward
Regional Manager – California
jhayward@opensystems-publishing.com

Phil Arndt
Regional Manager – East Coast
parndt@opensystems-publishing.com

Richard Ayer
Regional Manager – West Coast
rayer@opensystems-publishing.com

International Sales

Stefan Baginski
European Bureau Chief
sbaginski@opensystems-publishing.com

Dan Aronovic
Account Manager – Israel
daronovic@opensystems-publishing.com

Reprints and PDFs

Call the sales office: 586-415-6500