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VOLUME 11 • NUMBER 1
FEBRUARY 2007

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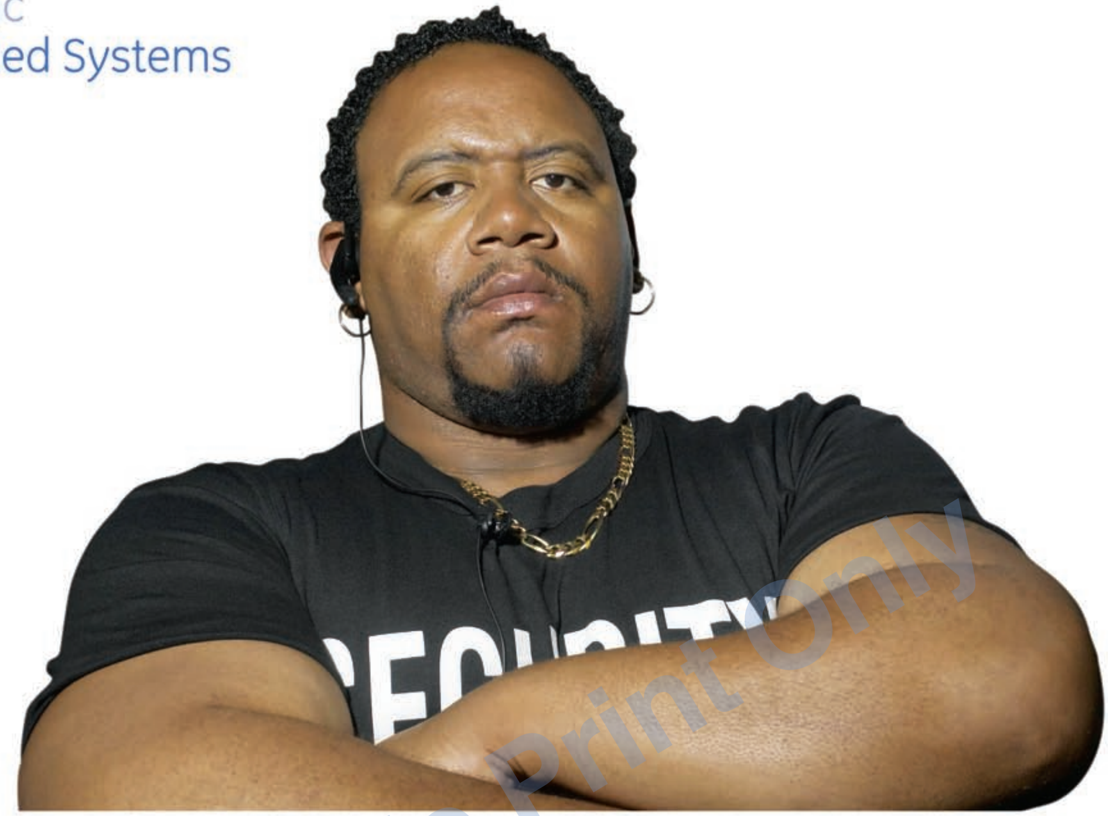

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CompactPCI® and AdvancedTCA® Systems

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Communications Group

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CompactPCI and AdvancedTCA Systems (USPS 019-288) is published nine times a year (Feb, March, April, May, June, July/Aug, Sept, Oct, Nov/Dec) by OpenSystems Publishing LLC, 30233 Jefferson Avenue, St. Clair Shores, MI 48082. Print ISSN 1098-7622, Online ISSN 1550-0381. *CompactPCI and AdvancedTCA Systems* is free to qualified engineers or management dealing with or considering open system technologies. For others, paid subscription rates inside the US and Canada are $63/year. For first class delivery outside the US and Canada, subscriptions are $90/year (advance payment in US funds required).

Periodicals postage paid at St. Clair Shores, MI, and at additional mailing offices. Canada: Publication agreement #40048627. Return undeliverable Canadian addresses to: WDS, Station A, PO Box 54, Windsor, ON N9A 615.

POSTMASTER: Send address changes to *CompactPCI and AdvancedTCA Systems* 16872 E. Ave of the Fountains, Ste 203, Fountain Hills, AZ 85268


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By Joe Pavlat

Ready for the future

"There has been more material progress in the United States in the 20th century than there was in the entire world in all the previous centuries combined." – Stephen Moore and Julian Simon, Cato Institute, December 1999

We have come to expect rapid advances in the technology we use in our lives, and these advances come at a rate unimaginable just a few generations ago. Many of these are in the field of communications, which has greatly altered our personal and professional lives and permeates virtually every aspect of life including world affairs, politics, government, education, health care, and relationships. PICMG began in 1994 as a consortium focused on using the then-new PCI technology for industrial computer applications. Over the years PICMG has shifted its focus to add communications and telecom oriented platforms and technologies. The biggest of these appears to be AdvancedTCA, although MicroTCA, made possible by the AdvancedMC specification, is attracting intense interest from an increasing number of non-telco market segments for which packet-based communications are a key ingredient.

Last year, PICMG completed and ratified the MicroTCA specification and released Revision 2 of the AdvancedMC card specification, adding more features and a new card size optimized for storage applications. The work on the Ethernet version of AdvancedMC, AMC.2, was completed as well.

2007 promises to be a busy year for PICMG. Now underway is a large effort to produce Revision 3 of the AdvancedTCA specification. It should be completed this year. Work continues in the Requirements Engineering Subcommittee, which is tackling the large task of numerically cataloging all of the AdvancedTCA specification's necessary and optional requirements. This effort will make the creation of specific configurations, or profiles, possible in a straightforward manner. The first likely customer for this work on profiles will be the recently formed Communications Platforms Trade Association (CP-TA), as they work on defining specific AdvancedTCA platforms. CPTA will also be developing test software and plans to conduct compliance testing. PICMG and CP-TA have been working together for about a year, and a formal liaison agreement between the two organizations was ratified late last year. This agreement allows the two organizations to share information while protecting each body's intellectual property rights and confidentiality.

Customers, at least in the telecom industry, are clearly and rapidly moving away from building everything in house and are starting to buy standards-based platforms such as AdvancedTCA on the open market. This allows manufacturers to concentrate on providing their customers, the carriers, new and innovative products and services in the extremely competitive consumer markets for broadband, wireless communications, and video services. Increasingly, vendors are finding that Telecom Equipment Manufacturers (TEMs) do not want to buy bits, pieces, and boards from an assortment of vendors and assemble it themselves. They are demanding that the market provide assembled and tested systems that have the operating system and other important software such as high availability middleware already installed. The TEMs focus on adding value by adding their applications. This is creating the need for a new kind of super systems integrator, one who has the diverse skill set needed to put together and test these sophisticated platforms.

This drive to deliver application-ready systems is creating a new dynamic in the standards world. The task of creating all of the open standards needed to build these systems is beyond the charter and scope of any one of the existing consortia or Standards Development Organizations. Organizations including SCOPE, which is a group of telecom equipment suppliers that are jointly developing AdvancedTCA profiles, the Service Availability Forum, Open Source Development Labs (OSDL), focusing on Carrier Grade Linux, PICMG, and CP-TA are all working on parts of this puzzle.

"There has been more material progress in the United States in the 20th century than there was in the entire world in all the previous centuries combined."

All of these organizations need to cooperate and work together to develop their piece of the puzzle and share that piece with the others. Gaps must be identified and fixed and overlaps eliminated. The Mountain View Alliance has been formed to bring these various groups together. Also, intellectual property rules and obligations are different for every organization, and formal liaison agreements must be put in place to protect all. This is a big task in itself. The liaison agreement between PICMG and CP-TA took 10 months of effort before both parties and their members were happy with it. I suspect informal agreements are unfortunately becoming a thing of the past, but I guess that the legal profession can always use more work.

The intense interest in MicroTCA will likely result in that specification being opened up this year to add more features and define additional packaging for some of the newly defined applications that were outside the initial core telecom focus. As I mentioned recently in this column, the military and aerospace communities are looking for a ruggedized version of MicroTCA, and that will take a significant amount of work. Another identified application is unprotected outside environments such as towers and down inside manholes where much communications cabling exists. It will be a challenge to meet the requirements for applications such as these, but the diverse skill set and the talents of the PICMG membership continues to amaze me, and I am confident they will meet the challenge. It's going to be another interesting year.

Joe Pavlat
Editorial Director

3U CompactPCI boards key for *always on* passenger infotainment

Flat screens are used everywhere to display information. Because they are flat and light, they are now also used in mobile public transport vehicles such as subways, trams, commuter trains, and buses for public transportation. A common configuration combines two screens side by side. The left hand screen shows route information, such as upcoming stops. It also displays information about transfer possibilities to other transportation systems. The right hand screen displays a news ticker, local advertising, and similar information, such as a scene from a local movie theater. Some installations use single screen versions.

Visual information about the next stop is superior to audible announcements, which may be hard to hear at high noise levels. Audible announcements are also a problem for foreign visitors, especially in Europe with its many small countries with different languages. Passengers may not understand the local language.

Inova Computers (Germany) has supplied these systems for a long time to many worldwide public transportation vendors and authorities. Some examples include the Airport Express trains in Hong Kong, Kuala Lumpur, London Heathrow, and Vienna. Inova estimates that about three million travelers a day benefit from their installations in mainland Europe. Engineers at Inova Multimedia (Germany) pioneered the use of *always on* Digital Multimedia Broadcasting (DMB), which is based on Digital Audio Broadcasting (DAB). Inova Computers has integrated GSM, GPS, GPRS, and UMTS/3G into a 3U CompactPCI board for 24 x 7 operation (Figure 1). The small 3U CompactPCI boards are ruggedized to withstand vibration, shock conditions, and temperature extremes.

Commuter trains in places such as Athens, Berlin, and Hannover are also equipped with Multimedia Information Systems (MIS) supplied by Inova Computers. Inside the trains is the GigaSTaR serial digital transmission system. Inova Semiconductors (Germany) developed the GigaSTaR technology and chipsets. Recently NBC Universal gave Inova an order for a passenger infotainment system for Port Authority Trans-Hudson (PATH), the train service operating the railway link between New York City and New Jersey. Within the next three years, Inova Computers will supply equipment for 340 new trains, including 1,360 double video screens, stationary video terminals in 12 railway stations, wireless LAN equipment in 5 railway stations, and a studio interface. A service contract between NBC Universal and Inova Computers covers a period of 10 years after first installations.

Figure 1

Underwater

MEN Micro Elektronik GmbH (Germany) has supplied a control system in a highly compact 3U subrack, which is only 220 mm deep. The enclosure is 32 HP wide (representing eight CompactPCI slots). Six slots are available for CompactPCI cards. The remaining two slots are equipped with a pluggable power supply providing more than 100 W. A Pentium III processor running at 880 MHz under Windows NT Embedded powers the CPU card. An onboard hard disk is integrated into the system, which is used in a safety-critical environment onboard a submarine. Flexible I/O is provided by M-Module (ANSI/VITA 12) mezzanine cards on CompactPCI carrier boards. The M-Module M45 provides eight intelligent full-duplex RS-232 interfaces, which work in asynchronous mode. The M66 M-Module features an extremely high output current of 1.9 A per channel out of 16 A switching power. The 32 optically isolated binary process signals can be configured individually for input or output.

European trade fair in Asia

The Deutsche Messe AG, organizer of CeBIT and the Industrial Fair in Hannover (Germany), has organized a combination of four trade fairs at the Shanghai New International Expo Centre. The fair sections were Factory Automation Asia, Interkama Asia, Energy Asia, and Metal Working Asia. Exhibitors included Rittal, KUKA Robots, and Phoenix Contact. There were 704 exhibiting companies showing their products over five days to approximately 40,000 visitors from 26 countries. Many countries grouped exhibitors into country pavilions. These included Germany, Spain, Switzerland, United States, Japan, and Taiwan.

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By Dieter Carl and Louise Moser

The SCOPE of telecommunication standards

Introduction

The days in which a single Network Equipment Provider (NEP) designed, manufactured, and supplied all of the software and hardware in a telecommunication system are long gone. Now, the NEP obtains both software and hardware platform components from different component vendors and then integrates those components together with its own components and applications into a complete telecommunication system that it delivers to the service providers (carriers). Examples of such components are:

- Hardware, such as server cards, shelves, and cabinets
- Operating systems, such as Carrier Grade Linux
- Middleware, such as high availability middleware
- Tools, such as development and profiling tools
- Operations and maintenance services, such as network management
- Applications, such as multimedia services

It is important to the NEP that several alternative suppliers exist for each of the components, so that a competitive market ensures high quality, responsive service, and reasonable prices. Interoperability is also important. The components provided by the platform component vendors should work together (interoperate), and a single standard should exist, rather than competing standards that would fragment the market.

Standards organizations

Several organizations have been established to define standards for various aspects of the platform components, including:

- PICMG for physical hardware
- Service Availability Forum (SA Forum) for high availability middleware
- Open Software Development Laboratory (OSDL) for Carrier Grade Linux

These standards provide an excellent basis for the development of telecommunication software and hardware, but the standards organizations are not focused exclusively on telecommunication systems. A great deal of understanding and hard work goes into the creation of a standard and, thus, these organizations seek to promote their standards for a wide range of applications. For example, the SA Forum wants to establish standards for service availability that apply not only to telecommunication applications, but also to enterprise applications. To satisfy a wider range of applications, the standards might require additional features or requirements beyond those that telecommunication systems need. Consequently, the NEPs have started to worry about *specification creep*. On the other hand, there are gaps in the standards, because of the specialized nature of some requirements. For example, the current MicroTCA specification does not cover all of the requirements for outdoor equipment.

The SCOPE Alliance is a consortium of NEPs that reviews industry standards to determine their relevance to telecommunication systems. It is organized as a program of the IEEE Industry Standards and Technology Organization. The sponsor members of SCOPE are major NEPs: Alcatel-Lucent, Ericsson, Huawei, Nokia, Motorola, NEC, and Siemens Networks.

In addition, the SCOPE Alliance also has contributor members, which are typically the component suppliers. Currently, there are 12 contributor members.

The member companies of the SCOPE Alliance contribute experts that review the standards and generate a NEP-focused profile for each platform standard. The profile defines which aspects of the standard are required for quality and interoperability in telecommunication systems, and which aspects are not necessarily needed. It also identifies gaps in the standards. The SCOPE Alliance does not itself define standards, and it does not provide specifications to fill the gaps that it has found in existing standards.

The SCOPE reference architecture

Figure 1 shows the SCOPE Reference Architecture. The initial focus of the

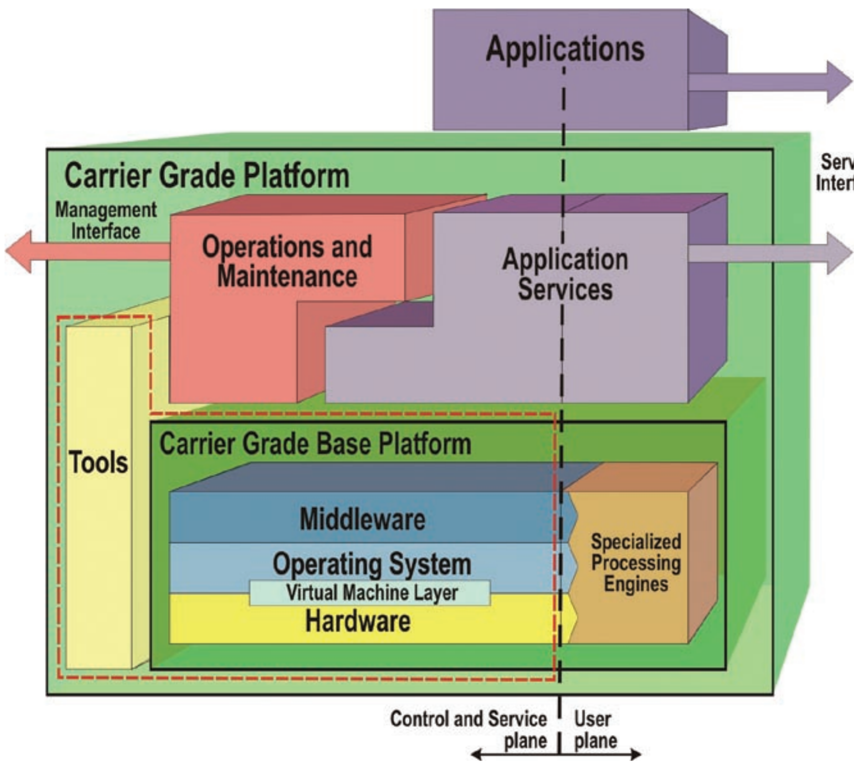

Figure 1

SCOPE Alliance centers on the components within the red dashed lines, that is, the carrier grade base platform and the tools. The carrier grade base platform includes:

- Hardware, such as blades and shelves
- Operating systems, particularly Carrier Grade Linux
- Middleware, including high availability middleware

These technologies are quite mature, and many base platform components are becoming commodities with little proprietary differentiation. Good standards for many aspects of the base platform already exist, and the SCOPE Alliance seeks to strengthen those standards and to focus them on telecommunication systems.

In contrast, few industry standards for tools currently exist; however, SCOPE has determined that standards for development and test tools can reduce the difficulties of combining together software components. SCOPE is encouraging the development of standards for such tools. Among the methodologies of interest to SCOPE are the UML-based Model Driven Architecture developed by the Object Management Group, XML, and other formats of the World Wide Web Consortium for specifying configuration files and other application input, the Eclipse guidelines for interactions between tools and their users, and various UNIX system development tools.

The SCOPE Alliance has initially focused on the control and service plane, to the left of the black dashed line in Figure 1, which is vital for interoperability between components, rather than on the user plane, where proprietary differentiation still exists.

SCOPE has already issued profiles for the Advanced Telecommunication Computing Architecture (AdvancedTCA) standard from PICMG and for the Carrier Grade Linux (CGL) standard from OSDL. SCOPE is currently developing a profile for the Application Interface Specification (AIS) high availability middleware standard from the SA Forum. Gap analysis of existing platform standards is underway.

The role of SCOPE in the platform industry

Today, there are many activities around standardization in the platform industry. Sometimes it is hard to understand who will deal with what. Figure 2 gives a simplified picture of how these various initiatives interact.

The primary role of SCOPE here is to produce input to the Special Interest Groups (SIGs) of the standardization bodies, based on the existing specifications and reflecting the requirements of the service providers. On the other side, the Communications Platforms Trade Association (CP-TA) takes the SIGs' output (specifications) and drives the delivery of products that comply with SCOPE profiles.

Future activities

During its first year, the activities of SCOPE focused on profiling existing specifications and on the control and service planes shown in Figure 1, where SCOPE will continue to focus its activities.

In 2007 SCOPE intends to create a *tools content profile* for development and test tools. The term *tools content profile* means the description of requirements related to functions and properties of tools for the development of carrier grade systems. SCOPE is looking at such tools standards as the UML-based Model Driven Architecture, XML, and other formats for specifying configuration files and other application input, the Eclipse guidelines for interactions between tools and their users, and various UNIX system development tools. Tools content profiles for such tools can reduce the difficulties of combining software components in telecommunication systems.

Gap analysis will be a second important area of work for SCOPE. Gaps exist in the standards due to the specialized nature of some requirements. For example, the AdvancedTCA specification does not currently address certain blade and shelf thermal requirements, which are necessary for interoperability. The intention of SCOPE is to influence the development of upcoming standards before they are finalized. Thus, the work on gap analysis will be performed in close cooperation and dialogue with the SIGs.

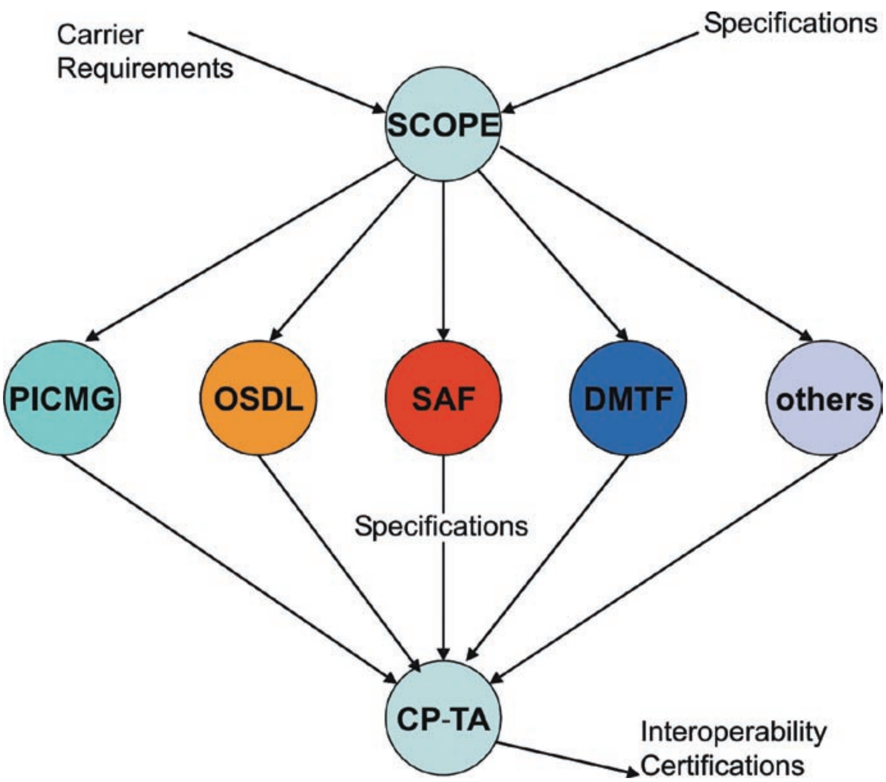

Figure 2

A third important area of work for SCOPE is definitions. The platform industry today has different roots, experience, and history. Thus, there is a lack of common interpretation of such terms as carrier grade, service availability, long lifetime support, and central office environment. As an example, consider the 5-nines availability requirement. Many companies interpret this requirement to mean the availability during the operational phase of a system, but in the telecommunication industry this requirement is understood to be an overall requirement including maintenance. Thus, zero downtime means no service interruption at all over many years. There is clearly a need to create a common understanding of terminology across the entire industry.

Conclusion

The SCOPE Alliance has successfully started to review and influence standardization work in the platform area. The main goal of SCOPE is to help to develop a powerful platform ecosystem, which allows the Network Equipment Providers to fulfill the requirements of their customers.

The SCOPE Alliance continues to encourage contributions to, and comments on, their profiles and gap analyses. SCOPE welcomes companies that seek to build, or supply components for, telecommunication and network equipment. Widespread active participation in SCOPE will result in realistic standards and a vigorous market that increases the quality and reduces the cost and time to market, to the benefit of all.

Dr. Dieter Carl *is vice president, platform strategy at Siemens Communications.*

Dr. Louise E. Moser *is a professor in the Department of Electrical and Computer Engineering at the University of California, Santa Barbara.*

For more information, please see the websites of the following organizations:

- SCOPE Alliance
  www.scope-alliance.org
- PICMG
  www.picmg.org
- Open Source Development Lab
  www.osdl.org
- Service Availability Forum
  www.saforum.org
- Distributed Management Task Force
  www.dmtf.org
- Communications Platforms Trade Association
  www.cp-ta.org

WWW

Core functions of the highly available application-ready platform: Don't promise availability without them

By Dr. Asif Naseem

As standards-based hardware platforms such as AdvancedTCA, MicroTCA, and BladeCenter gain increased application in the telecommunications market, Telecom Equipment Manufacturers (TEMs) are looking for preintegrated, pretested application-ready platforms. These platforms need to include standards-based, sophisticated high availability management capabilities. The value of such capabilities lies in ensured service continuity in the face of various hardware and software failures. Current approaches demonstrate that using a standard set of services to implement highly available network elements can save TEMs a significant amount of effort, cost, and time to revenue. Asif describes a few of the key concepts and services required in such an endeavor and presents a real life example.

Modeling the system

One of the key features of a highly available system is its ability to represent the configured system resources – managed objects – in a dynamic system model that can be used in implementing sophisticated availability management policies. The system represents each resource that is to be managed as a managed object in the system model. It also captures resource dependencies, including intricate relationships that form a given service. The system model ensures that project teams can easily maintain and/or change a system configuration over time. The key features of the system model include the following:

- Management representation of resources based on relevant industry standards, such as ITU Recommendation X.731
- Scaling to 10,000+ managed objects
- Defined attributes for health, operational state, administrative state, role, availability status, and dependencies
- Methods for access/control, monitoring, and configuration
- Logical representation of redundant resources and any arbitrary collection thereof
- Implementation of important redundancy policies such as 2N, N+1, N+M, and Active/Active

Highly available systems must provide redundancy of the system model to ensure uninterrupted availability management. Systems configured with more than one node can automatically replicate the system model from the active node to a standby node. This ensures the system can quickly fail over and continue service in case the manager node experiences a failure or can no longer communicate with the other nodes in the system.

Creating and maintaining a dynamic system model for managing system availability requires a set of sophisticated platform resource management services. Let us look at a few that are essential.

Platform resource management

The Platform Resource Management Service (PRMS) offers a standard abstraction layer that provides the ability to integrate with the hardware resources of a particular platform when integrated with the Service Availability Forum (SA Forum) Hardware Platform Interface or HPI. (SA Forum documentation is available at: www.saforum.org/specification.) PRMS can provide expansive platform management capabilities in a way that is both standard and hardware agnostic. Let us look at each in some detail.

Discovery

A discovery capability allows user applications to automatically discover and enumerate the set of hardware resources present within the system, along with the respective management capabilities those resources possess. This service enables discovery and monitoring of real-time dynamic information on all the configured hardware resources including compute cards, networking boards, fans, and power supplies. Furthermore, this service collects and maintains inventory management information about various hardware entities, which typically includes information such as the manufacturer ID, product name, product version, and serial number. This information is used to populate the system model, manage the platform resources, and apply appropriate availability management policies.

Monitoring

This capability of the PRMS/HPI service includes detailed mechanisms to monitor the health and performance of various hardware resources. The notification and logging capabilities provide a mechanism to monitor, communicate, and log various events occurring in the system. Key examples include the following:

- *Sensor events* that identify the change in the state of a sensor, such as a temperature or a voltage gauge exceeding or dropping below one of its predefined thresholds
- *Hot swap events* that identify a change in the hot swap state of a Field Replaceable Unit (FRU)
- *Resource failure events* that identify whether a resource has failed, has been restored to a healthy state, or has been added to the system

Management

Manageable hardware resources – known as HPI entities – generally have one or more management instruments associated with them. Some key examples include sensors, controls, watchdog timers, and annunciators. Sensors provide information on an entity through the measurement of a critical hardware entity attribute, such as a voltage sensor or a temperature sensor. As the states of sensors change, this service will also send event notifications to all subscribing applications identifying the change in sensor state, such as a voltage or temperature sensor exceeding a critical threshold. Controls provide read/write access to control devices associated with hardware entities such as LEDs, dry contact closures, LCD displays, and audible alarm indicators. In addition controls allow a user application to customize the manner in which information (on alarms for example) is communicated to the system administrator. Watchdog timers monitor the health of a system by ensuring that critical aspects of the system, for example BIOS operations or the loading of the operating system, are progressing well. Annunciators provide abstracted controls that can have a set of alarm conditions associated with them. The annunciators ensure that the alarms are properly annunciated through the platform's and the entity's alarm indicators.

Hot swap management

Hot swap ability is a critical requirement of highly available systems. Such systems provide Hot Swap Management Service (HSMS) to manage insertion and extraction sequences for the FRUs in the system. Although HSMS typically builds upon the functionality of the PRMS, it goes beyond PRMS and HPI capabilities. For example, HPI provides a standardized interface for accessing and managing hardware resources but lacks more advanced management functionality, such as managing resource(s) that depend on a hardware resource or FRU that can be dynamically inserted or extracted from a system.

HSMS, on the other hand, in conjunction with PRMS, fully manages hot swap insertion and extraction sequences within the system. HSMS assists in each step of hot swap insertion and extraction sequences to allow the operator to manage and control the hardware resources being inserted into the system, as well as coordinating the controlled shutdown of software resources, such as applications, that depend on a hardware resource being extracted from the system. Sophisticated hot swap management services provide this management functionality with minimal programming. HSMS typically includes predefined hot swap management policies and actions for each of the key steps in the managed hot swap sequences. The operator can choose from among the predefined set to quickly and easily establish the hot swap management policies. For systems requiring more complex or custom policies, HSMS provides programmatic interfaces to extend the predefined HSMS policies and actions.

Alarm management

Alarm management is the process of monitoring a system for conditions that may jeopardize healthy operations and using this information to implement policies to take appropriate action in response to various alarm conditions. In a highly available system, the Alarm Management Service (ALMS) deals with alarm conditions found at the software as well as the hardware level. ALMS custom code enhances and further integrates the particular hardware platform. Working together, PRMS, HSMS, and ALMS offer a powerful set of functionality required to create a highly available application-ready platform. Although the ALMS is designed to work as a standalone service, it provides enhanced functionality when running in conjunction with PRMS. ALMS includes the following functionality:

- Maintains an active alarm list for the system that can be queried by the management applications to get the latest alarm status information
- Enables user creation/deletion of alarm conditions, including automatic alarm annunciation on the system platform(s); allows the management applications to identify additional alarms in nonhardware resources and still have these software-related alarms annunciated on the system platform(s) consistently with other alarm conditions

- Allows acknowledgement of alarm conditions including automatic updating of the system alarm annunciation
- Automatically identifies alarm conditions based on changes in system state, which enables the operator to define the associated alarm level for different events in the system and have ALMS automatically generate the alarm conditions based on the particular configuration settings
- Redundant service design to eliminate single points of failure and to ensure ALMS functionality is continually accessible on the system
- Detection, generation, and annunciation for resources undergoing a state transition to a state of failed or no resource, for resources that do not belong in the system model, and for resources whose sensor indicates a temperature or voltage threshold violation
- Configurable severity levels – critical, major, and minor – to adjust how the system reacts to an alarm condition, and configurable actions to be taken in the event that sensor temperature or voltage thresholds are crossed

Vendor specific integration

Often various hardware platforms provide a differentiated set of monitoring and management capabilities. Such items as sensors, control, special displays, and annunciators can be employed to tailor platform management for particular applications or simply enhance management capabilities. It is helpful to have platform management services with extensibility. This allows vendor-specific capabilities to be included to augment the standard set of management capabilities. HPI includes these provisions, and services such as PRMS, HSMS, and ALMS can be designed to take advantage of these extensions.

An example implementation – RadiSys and GoAhead

GoAhead Software, Inc. and RadiSys Corporation have worked together to build an application-ready platform for equipment manufacturers from a variety of markets, who all must ensure carrier grade (99.999 percent and above) service availability. Makers of next-generation networks and IP multimedia subsystems are among those looking toward preintegrated platforms as a way to ensure availability and accelerate time to market for new services. By leveraging a solution based on standards, these equipment manufacturers can repurpose their original investment many times across multiple applications, gaining significant cost efficiencies. Some examples of applications that leverage this carrier grade application-ready platform include Session Initiation Protocol (SIP)-enabled applications, media gateways, and softswitches.

Such a platform has been created by utilizing the suite of high availability and platform management services available in GoAhead SelfReliant and on the RadiSys Promentum AdvancedTCA hardware platform running the Linux operating system, as shown in Figure 1. The critical integration elements to create this platform are depicted in Figure 2.

PRMS along with HPI, HSMS, and ALMS form key components of this integration. PRMS has been integrated with the HPI libraries implemented in the hardware. Additionally HPI resource discovery capabilities enumerate all the resources to create an initial system model, and to dynamically update this model as the various resources' roles and states change while different system events take place. These resources – or managed objects – can

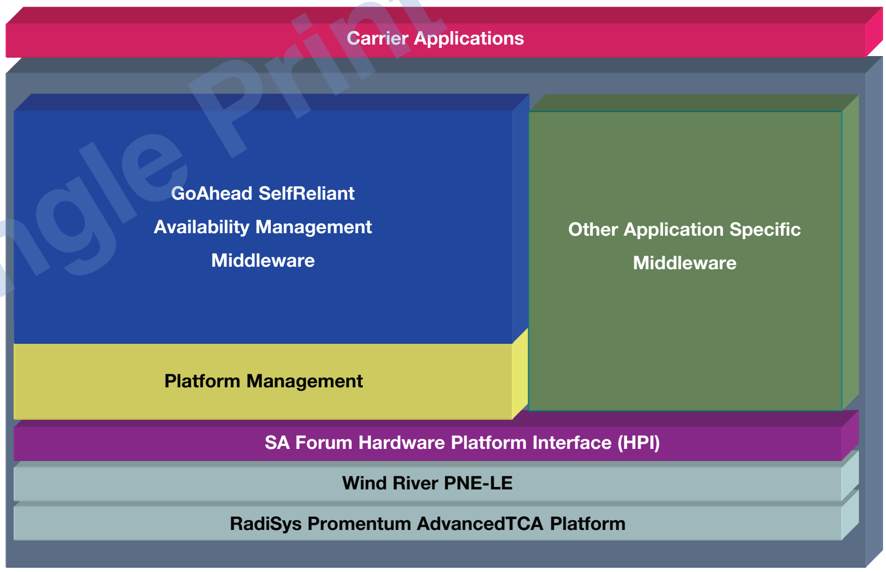

Figure 1

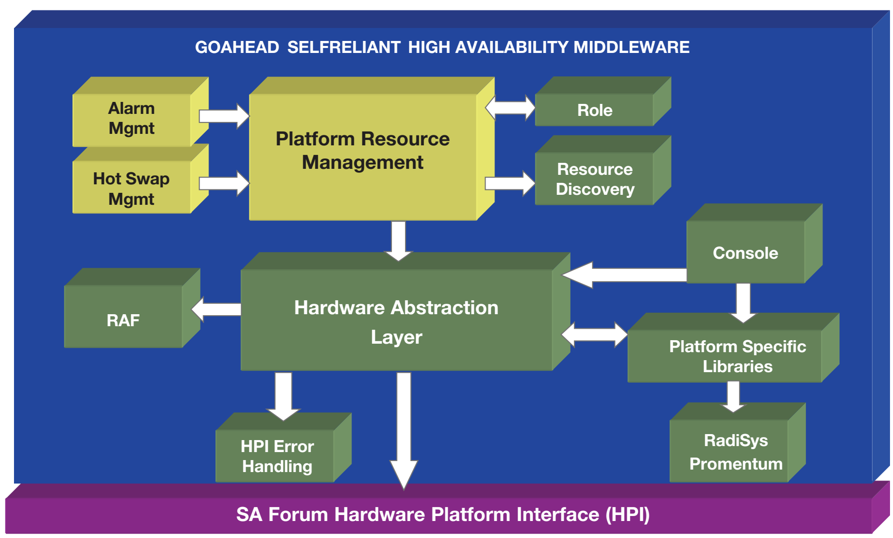

Figure 2

either be local to the cluster or remote, in which case they are represented by a remote adapter. A Remote Adapter Factory (RAF) is employed to maintain the current state of such managed objects. A state engine – depicted as a *role* – establishes if a PRMS instance is active, standby, or unassigned. A Hardware Abstraction Layer (HAL) translates standard HPI calls into actions that are specific to the underlying hardware. Conversely it translates hardware events such as hot swap events, into appropriate HPI notifications that are sent upstream to the management application. HAL also uses an error-handling component to identify and recover from errors that may occur during HPI calls. These error-handling policies are customizable through an XML file.

The integration of these capabilities is carried out to ensure portability across different hardware capabilities. As such a platform specific library provides abstraction from any differences in the underlying platform, that is, any differences in HPI implementation, such as OEM specific data types, platform specific configuration, and the like. Finally, a console component is used to implement a browser-based console to access and display various platform attributes in a readable format.

Conclusion

As we have discussed, there are fundamental elements that must be present in order to have a robust highly available system: a dynamic mechanism for enumerating system resources; platform resource management that enables discovery, monitoring, and management of hardware resources; comprehensive and graceful hot swap and alarm management; and integration with vendor-specific hardware sensors and controls. While selecting standards-based hardware and high availability management middleware offers unquestionable value, much work remains to be done to integrate the two to the level described here. A preintegrated solution based on standards takes this effort out of the equation and enables equipment manufacturers to focus on differentiation at the application layer by leveraging an application-ready platform that has all of this functionality already baked in. This offers significant time-to-market improvements. Moreover, because the platform is standards-based, allowing application portability, it enables TEMs to optimize and protect their investments and ensure that platform changes can be made later without a significant loss in already-developed platforms.

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Solving extreme FPGA high-density computing with AdvancedTCA

By Greg Tiedemann

A new initiative recently authorized by the Federal Communications Commission (FCC) teams satellites with earth-bound communications systems to significantly improve coverage and capacity for voice and data communications. The key technology to enable this coexistence is antenna beamforming, which adaptively forms hundreds of data channels from a satellite, while canceling interference from ground communication systems, via a combination of an array of antennas on the satellite and very sophisticated ground-based computational systems. With this new system, very high-bandwidth data or voice services can be directed to an area on the ground and received by mobile terminals, including small handheld devices. This provides a host of new communications services to out-of-the-way places, or after disasters like Hurricane Katrina.

Here Greg outlines how Mercury Computer Systems leveraged AdvancedTCA to enable a high-speed communications infrastructure – one that delivers the massive computing requirements that make this ground-based beam former a reality.

Leveraging the broad AdvancedTCA ecosystem

Our customer challenged Mercury with solving this difficult beamforming application while using a standards-based system compute platform. To meet the aggressive deployment costs and scheduled objectives, Mercury proposed leveraging the AdvancedTCA ecosystem, to take advantage of I/O and processing infrastructure to handle teraOPS of processing on terabits of data. While a proprietary system could have handled the requirements, it would have denied the customer the economic advantages of adopting a standard and using it to reduce the project risk and shorten time to market. Mercury selected AdvancedTCA as the standards-based platform for three important reasons:

- I/O – AdvancedTCA has unprecedented I/O capacity in the front and rear panels as well as the backplane
- Compute – the form factor is well-balanced teraOPS in a single subrack, though cooling remains a challenging design problem
- The need for a telecom-ready ecosystem to support high availability requirements and remote management

AdvancedTCA's modularity allowed the customer to scale all this I/O and compute capacity to various opportunities. Mercury is using every aspect of modularity in AdvancedTCA from Rear Transition Modules (RTMs) that route the antenna data streams into and out of the system to AdvancedMCs serving as host processors and hard drives.

In addition, the AdvancedTCA Intelligent Platform Management Interface (IPMI) infrastructure can be leveraged to accomplish management, upgrades, monitoring system health, and reporting alarms. These tasks can all be done speaking the same language, although there are different "dialects" within IPMI. Working with our customer and suppliers, Mercury is managing the tremendous amount of information that one can collect from the AdvancedTCA infrastructure and providing the ability to control and act on that information (for example, alarms), gaining a distinct advantage over any other commercially available technology.

> "Mercury worked closely with its chassis partner to achieve more than 200 W per slot."

A high-density FPGA computing solution

Figure 1 shows the two major components of the beam former that Mercury developed in close collaboration with our customer. Maximizing satellite receive power with beam shaping, which enables more antenna gain and less interference, as well as leveraging existing low-power wireless devices, requires:

- 300 Gbps of continuous I/O capacity in each direction. This implies 600 Gbps of intrasystem, bidirectional capacity. This translates to 25 Gbps in each direction per FPGA board with 12 boards in each shelf.
- 15 teraOPS of continuous computing per shelf. The beamforming is accomplished using 28 Xilinx Virtex4 SX-55 FPGAs at 400 MHz.

The Analog Conversion Unit (ACU) and the Beamformer Computational Unit (BCU) make up the central part of the beamforming system.

The ACU comprises 12 Analog Conversion Engines (ACEs) and two host processor modules. Each host processor module has a Gigabit Ethernet base switch and a Pentium M processor and a hard drive that are plugged into AdvancedMC sites. The system is hosted from one slot, with the other slot serving as a backup. The BCU consists of 12 Beamformer Conversion Engines (BCEs), which serve as compute blades for the BCU, and two host processors. Figure 2 shows a BCE block diagram and how traffic flows in through the RTM until being routed out to the FX60s.

As Figure 1 indicates, connectivity between the ACU and BCU takes place via a Fiber-Optic Rear Transition Module (FOM). A front panel analog SMA connector brings the data into

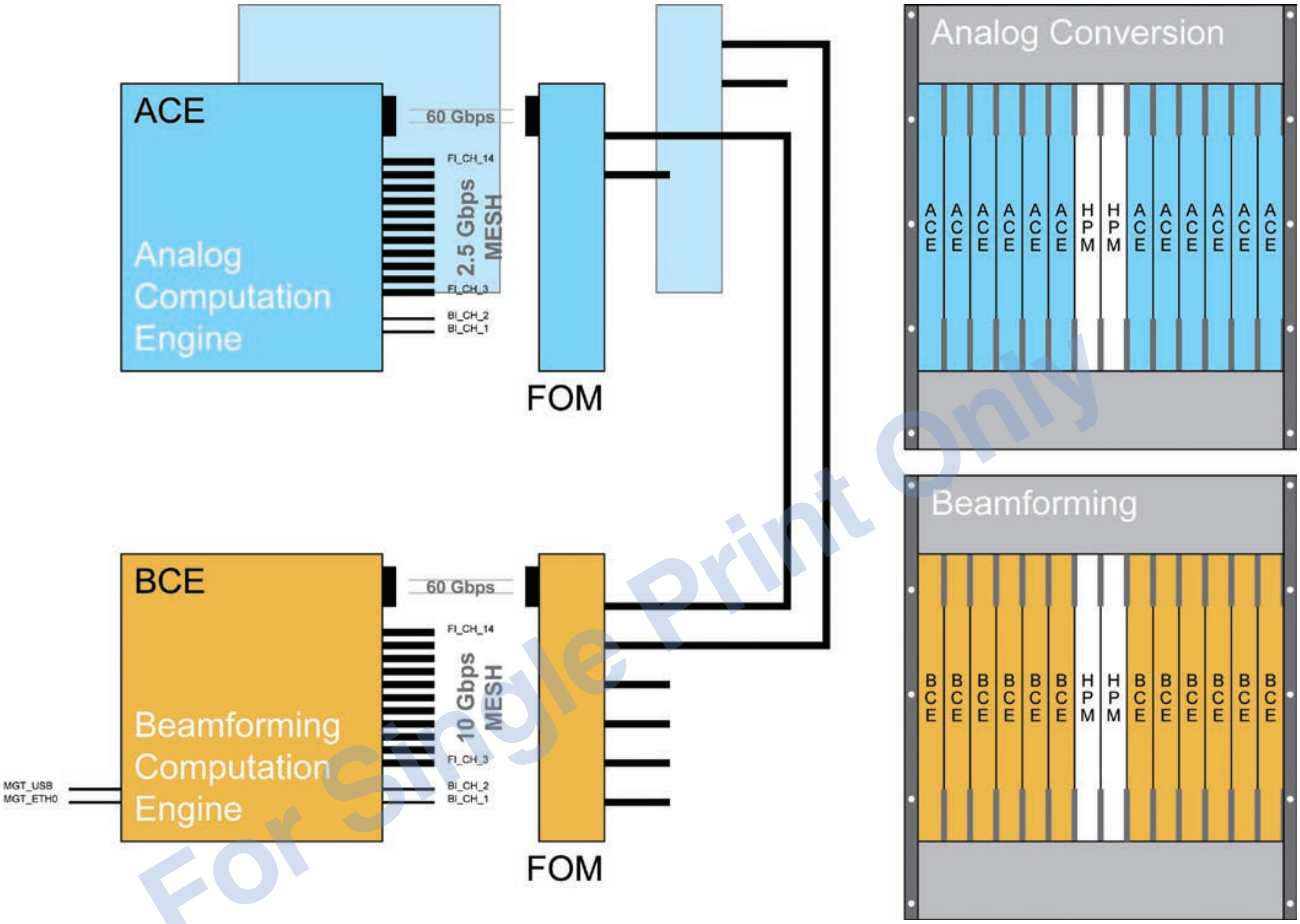

Figure 1

the ACE board from the satellite, where it is converted to digital. The data is sent out of the ACE rear transition module fiber optical (XFP) connectors and transferred to the RTM of the BCE.

Each BCE has 10 FPGAs. In the past customers might have used ASICs, but the advances in FPGA technology have opened the

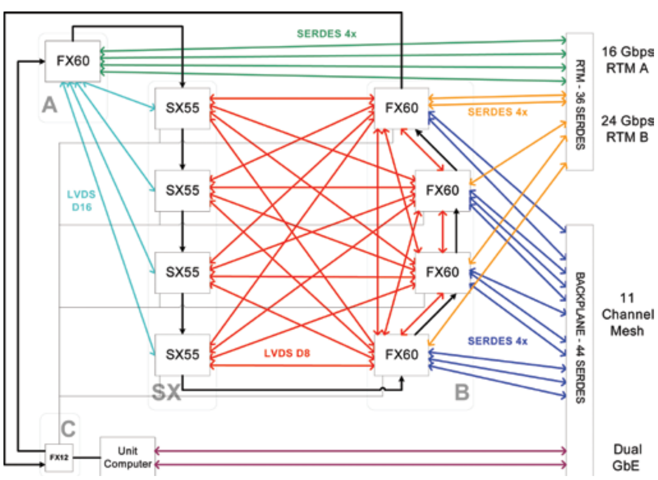

Figure 2

aperture on the possibility of deploying FPGAs for high-end compute demands. An FPGA-based solution aids with time to market and offers the customer the ability to continue to tune applications after the system is deployed.

Opting to go with more than 100 FPGAs in one 14-slot chassis (Figure 3) meant pushing the AdvancedTCA 200 W per slot thermal limits, and we are satisfied with how AdvancedTCA is performing. Mercury worked closely with its chassis partner to achieve more than 200 W per slot. We could have put fewer FPGAs on the board to avoid cooling challenges, but that would have meant additional systems. Early in architecting the solution we had five separate chassis, but succeeded in compressing that to two chassis, thus needing to cool more per slot.

Figure 3

FPGA communications firmware is critical

Mercury developed an FPGA communications infrastructure firmware specifically for this application, making it possible to switch synchronously among the 100 or so FPGAs in real time, with very low latency so that voice quality is maintained.

The FPGA firmware delivered with the system enables the user to focus on the application by handling all the communication between the FPGAs in the chassis and the chassis-to-chassis communication. Within the IP there is an application socket, which presents all the I/O resources to the user after data capture and parallelization has occurred. This application socket is where the user enters their IP and utilizes the communications and control structure provided.

The firmware has built-in link checkers for all communication links within the system. This allows in-field system diagnostics to be run without any additional firmware. Also included within the firmware is the command and control infrastructure, which allows the processing subsystem to communicate to all the FPGA registers. The API enables software engineers to immediately start developing the application to reduce time to market.

The communications' infrastructure is customized for beamforming applications, enabling reconfigurable segmentation and re-assembly of I/O streams in time and space. There are many possible configurations for the IP, which will solve a variety of application domains.

We are also deploying the most advanced platform management software for remote operation, administration, and management of FPGA applications. Our goal is making applications highly available and highly reliable, and improving the serviceability and visibility of field-deployed applications.

Carrier Grade Linux deployed on processors throughout the system makes up the system's Linux Support Package.

More applications

Mercury has found in developing this system that this architecture could open up a number of other applications for AdvancedTCA. For example, beamforming applications are similar to some defense and commercial radar applications. Now a springboard to other applications that involve deploying massive numbers of FPGAs exists. We can do much more with the AdvancedTCA infrastructure than we were initially anticipating, and that bodes well for future growth and a long lifetime for AdvancedTCA.

Greg Tiedemann *is director of business development and systems engineering for Mercury Computer Systems' Communications Computing Segment. Prior to joining Mercury, he spent nearly 10 years with Ericsson. He has a BS in Mechanical Engineering from Tri-State University, Indiana.*

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The multicore revolution

By Tim Van De Walle

The space and power constraints of the Advanced Mezzanine Card format bring unique challenges to board design when considering modern dual core architectures. Tim focuses here on design choices around power system design, memory system design, I/O design options, and layout considerations. The issues will be discussed in light of power and space constraints of an AdvancedMC module and the desire to maximize performance of a dual core design.

Multicore processing is old hat among the desktop computing crowd, with all of the major computer vendors offering multicore consumer desktop systems. More recently multicore processing has been making waves in embedded computing. Many of the well-known embedded software tools providers have been touting solutions designed to simplify multicore software development. On the hardware front Venture Development Corporation predicts that multicore AdvancedTCA blades will increase market share from 1 percent in 2005 to somewhere around 15 percent in 2007. Clearly the embedded world is catching on to the multicore revolution.

What's motivating the impressive growth in multicore processing?

The embedded marketplace is not immune to the demands of increased computing power. In the telecommunications market triple and quadruple play networks are stressing existing architectures, while advances in signal and image processing are driving performance demands in the military and medical markets. In addition to the increase in absolute computational power, more stress is being put at the edge of networks, driving reduced power consumption and performance density. Traditional single core and even traditional discrete multiprocessor approaches simply cannot scale in the face of all of these demands.

Performance density

With new integrated multicore solutions, board designers can achieve densities that were not possible with discrete multiprocessor solutions. In the AdvancedMC and MicroTCA market, discrete multiprocessor architectures are likely physically impossible to implement on a single-width card. The AdvancedMC standard specifies a board size of 180 mm x 74 mm (approximately), however only about 55 percent to 65 percent of that space is available for processing and memory system layout (see Figure 1) after considerations for front panel I/O and AdvancedMC power supply requirements.

With a discrete multiprocessor system two processing cores and a bridge chip would consume roughly twice as much space as an integrated System-on-Chip (SoC) multicore processor. Table 1 gives a rough comparison of the space requirements for similar processing configurations using dual MPC7448s and a single MPC8641D. In addition the discrete multiprocessor system would introduce additional layout difficulties that would cause this solution to use more space.

While discrete multiprocessor systems have been and continue to be successful in AdvancedTCA and CompactPCI blade designs, the multicore SoCs such as the MPC8641D from Freescale offer much higher performance densities and make multicore mezzanine cards a reality.

Configurability

In addition to the high performance densities that can be achieved using a multicore SoC in an AdvancedMC form factor, the end user gains system flexibility and cost savings that are otherwise unachievable.

At the most basic level a multicore processor can operate in Asymmetric Multiprocessing (AMP) mode or Symmetric Multiprocessing (SMP) mode. In AMP mode both cores will be running independent copies of an operating system (or the same operating system) and certain system resources are either partitioned ahead of time, or a method for sharing must be designed. A multicore

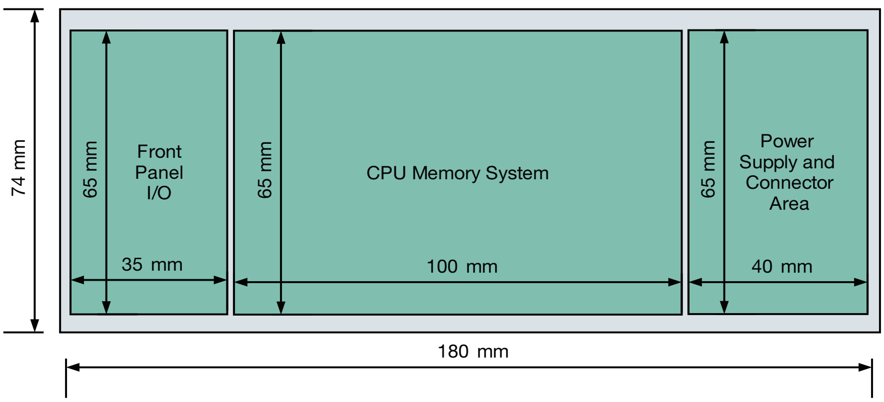

Figure 1

Dual Core MPC7448 System	
Component	**Size**
Core 1 (MPC7448)	25 mm x 25 mm
Core 2 (MPC7448)	25 mm x 25 mm
Bridge Chip	35 mm x 35 mm
Total	**2475 mm²**

Dual Core MPC8641D System	
Component	**Area**
Dual Core (MPC8641D)	33 mm x 33 mm
Total	**1089 mm²**

Table 1

board that can operate in AMP mode offers the system designer several different configurations for balancing system performance. Figure 2 shows some possible system configurations for an AMP multicore card.

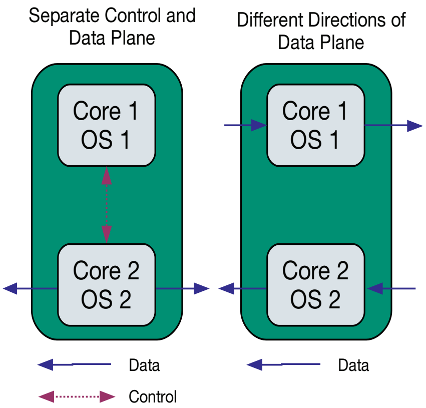

Figure 2

In SMP mode a single instance of an SMP-capable operating system is running across both cores. Resource sharing and load balancing are dynamically handled by the operating system. The SMP configuration will achieve the highest utilization of both processors because it can respond dynamically to load in the system. However, the system designer must decide if dynamic load balancing is acceptable and whether or not the system software is architected to take advantage of an SMP configuration. A multicore board operating in SMP mode will typically be used in higher-end systems that require very high performance control systems. If there is enough computing overhead, however, it can be used to help future proof an application and remove an extra control card from the system.

A carefully designed multicore AdvancedMC card can be configured to operate in several different configurations depending on performance, reliability, and cost requirements. For example, a single-width, full-height AdvancedMC processor board from Embedded Planet, the EP8641A, includes independent banks of DDRII RAM connected to the MPC8641D's dual memory controllers. Configured in this manner the processors' cores can easily be configured to operate in either AMP or SMP mode with simple software changes. When evaluating a multiprocessor card it is important to consider how the I/O resources such as memory controllers, interrupt controllers, and bus interconnects are shared among the cores and how the computing resources can be most efficiently and effectively deployed.

Quickly gobbling the power budget

While the SoC multicore processors in popular use today offer a significant MIPS/Watt advantage, in a small footprint such as an AdvancedMC card power consumption cannot be ignored. The 60 W maximum power for an AdvancedMC card is a significant improvement over the less than 8 W maximum power for PMC cards, yet a multicore card can quickly reach the 60 W limit and challenge cooling demands.

Many of the multicore processors can take up half the power budget when the processor operates near the high end of its frequency spectrum. Combining the power requirements of the processor with high bandwidth memory interfaces and high speed interconnects such as Serial RapidIO, PCI Express, and Gigabit Ethernet quickly eat into the total power budget. In these cases the system designer needs to be aware of the end user requirements and likely usage scenarios to determine realistic power budgets.

Items that can typically be analyzed to optimize power budgets on an AdvancedMC card include I/O such as serial and USB ports, Ethernet, RapidIO, and PCI Express, RAM size and speed, and CPU operating frequency. For example, on an AdvancedMC card it is unlikely that all of the front panel I/O will be in use at the same time that the fabric interface and the processor are operating under peak demand. Therefore the power requirements for these items can be derated or considered separately. Additionally, many of the SoC multicore processors are offered in numerous supply voltage and operating frequency configurations, which can be used to adjust the total power budget. The increased flexibility of system design offered by the latest multicore processors often means that application demands can be met by the lower power devices.

Conclusion

The power and performance advantages of multicore computing have already substantially revolutionized the desktop computing world, and the revolution is rapidly expanding into embedded computing. The SoC multicore processors offer the system designer tremendous computing power and system design flexibility that was previously unavailable. In power and space confined applications such as AdvancedMCs the increased power and design flexibility requires the system designer to carefully consider the end applications in order to completely realize the performance and flexibility improvements.

Tim Van De Walle *is currently the marketing manager at Embedded Planet. He has worked in the embedded industry for more than 10 years. He has held software engineering positions at Motorola and Lockheed Martin. He has an MBA from the Weatherhead School of Management at Case Western Reserve University, an MSE in Electrical Engineering from the University of Pennsylvania, and a BS in Computer Engineering and BA in Philosophy from the University of Notre Dame.*

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AdvancedMC modules build powerful applications

By Thanh Nguyen

Created to support the Advanced Telecommunications Computing Architecture (AdvancedTCA), the Advanced Mezzanine Card (AdvancedMC) specification provides designers with a powerful and flexible basis for creating high-performance applications.

When PICMG defined the AdvancedMC in 2005, it opened the door to a wide range of communications and telecom applications. AdvancedMC modules can serve as the basis of systems ranging from home media gateways to metro-level central offices. They feature a flexible combination of size and performance options with additional features that make them versatile building blocks for system design.

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single Modules	73.8 x 13.88 x 181.5 mm	73.8 x 18.96 x 181.5 mm	73.8 x 28.95 x 181.5 mm
Double Modules	148.8 x 13.88 x 181.5 mm	148.8 x 18.96 x 181.5 mm	148.8 x 28.95 x 181.5 mm

Table 1

AdvancedMC modules come in a variety of sizes. (See Table 1.) A single module measures 73.5 mm x 180.6 mm while a double module measures 148.5 mm x 180.6 mm, with each available in three different heights (Figure 1). Depending on their size, the modules can handle from 20 W to 60 W of power. This combination of size and power capacity means that AdvancedMC modules of considerable complexity and performance can be implemented, providing system developers with great flexibility in partitioning their designs.

Figure 1

The AdvancedMC specification originally targeted telecommunications systems. As a result, modules have been defined to be hot swappable, allowing the repair or upgrade of systems without shutting down. They also include as many as 21 I/O serial packet interface channels, each running at 12 Gbps, and a system management capability based on the Intelligent Platform Management Interface (IPMI). These additional features ensure that the modules support high-reliability designs and can handle demanding, I/O-intensive functions appropriate to their telecommunications origins.

Developers have two ways of combining AdvancedMC modules into system designs. One is the original AdvancedTCA structure. PICMG created AdvancedMC modules to support the AdvancedTCA structure. An AdvancedTCA blade can carry as many as eight AdvancedMC modules, allowing systems based on AdvancedTCA blades to handle large and complex functions.

MicroTCA stretches application range

The second structure that utilizes AdvancedMC modules is the recently released MicroTCA architecture. MicroTCA allows developers to create systems by plugging AdvancedMC modules directly into a backplane, as Figure 2 shows. In effect, it uses the mezzanine module as though it were a blade itself. The architecture addresses mid-level performance applications by providing more cost-effective access to AdvancedMC module capabilities than the full AdvancedTCA structure. Designers can create systems as small as one or two modules using MicroTCA.

Between them, AdvancedTCA and MicroTCA allow developers to create

Figure 2

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systems spanning a wide performance range. In telecommunications, for example, the AdvancedTCA structure permits creation of large central office server systems. An AdvancedTCA shelf can hold as many as 16 blades, each of which can have from 4 to 8 AdvancedMC modules. The modules can each contain a full processor, including memory and high-speed serial I/O, along with USB, control, and storage interfaces. Emerson's KosaiPM AdvancedMC module, for instance, has a 1.8 GHz Pentium M processor, 256 MB, 2 GB of main memory, and two Gigabit Ethernet interfaces to the MicroTCA backplane or AdvancedTCA blade's switch. This capacity enables developers to implement the functionality of several servers on a single blade.

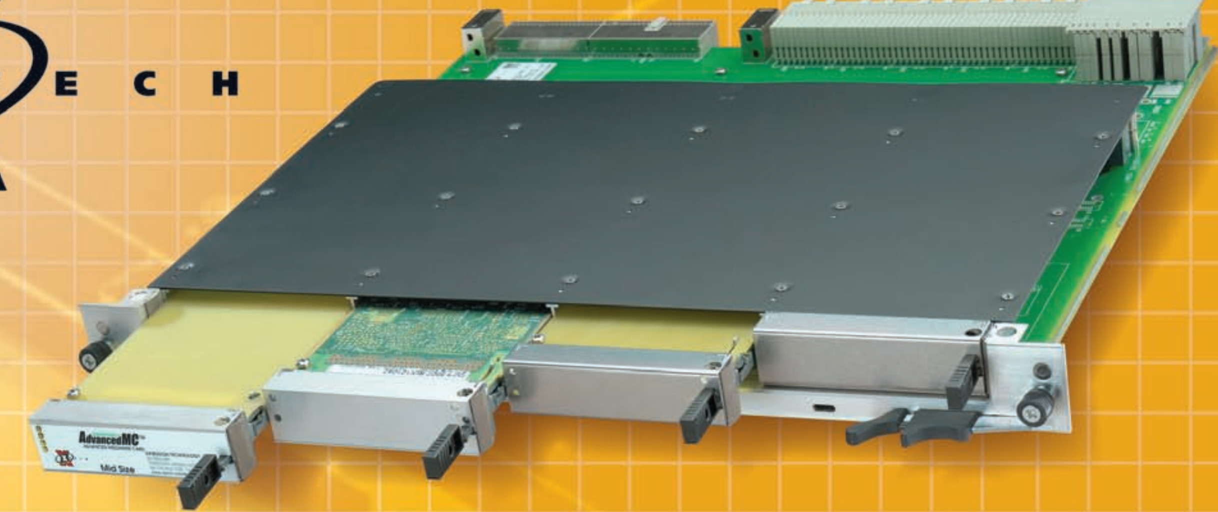
A MicroTCA chassis can employ AdvancedTCA blade processor modules to provide the same functionality as the AdvancedTCA shelf, but with smaller capacity. For example, system designers can create a mini-server using a 12-slot MicroTCA housing. The MicroTCA version offers the same features, uses the same interfaces, and runs the same software as the larger system, but has fewer channels and comes in a much smaller package.

The range of applications that these structures serve is limited only by the types of AdvancedMC modules that are available. Adoption of the AdvancedMC specification by vendors has only just begun, but a variety of functions have already reached the market. These functions include processor modules like the KosaiPM, DSP modules from companies such as Surf Communications, hard disk drives, and E1/T1 line interfaces. Many more AdvancedMC modules are in the works, continually expanding the possibilities for designers and enabling a plethora of applications for MicroTCA and AdvancedTCA systems.

System design possibilities abound

Today's selection of AdvancedMC modules, while not yet extensive, is already enabling many different system designs. For instance, combining processor modules, DSP modules, and T1/E1 line interfaces allows the creation of a media gateway. The DSP modules handle the compute-intensive image and audio compression and decompression, while the processor modules control channel access to the WAN. Designers can create the system using either AdvancedTCA or MicroTCA structures, depending on the channel capacity the gateway requires.

The same processor and DSP modules, combined with mass storage modules, form the basis of a media server, which could provide streaming video on demand to network users. Its functions would include reading the video data from mass storage and decompressing it for distribution



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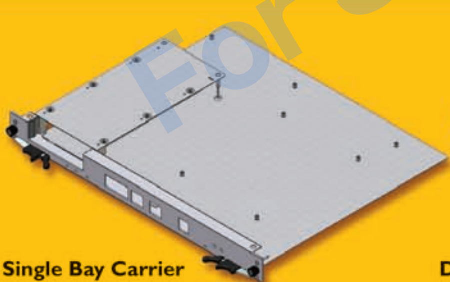
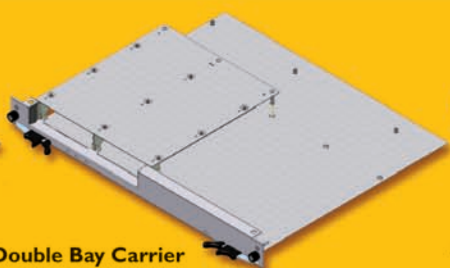
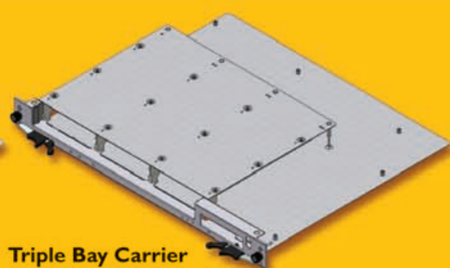
- Die-cast struts and card guides for a more robust system



Single Bay Carrier



Double Bay Carrier



Triple Bay Carrier

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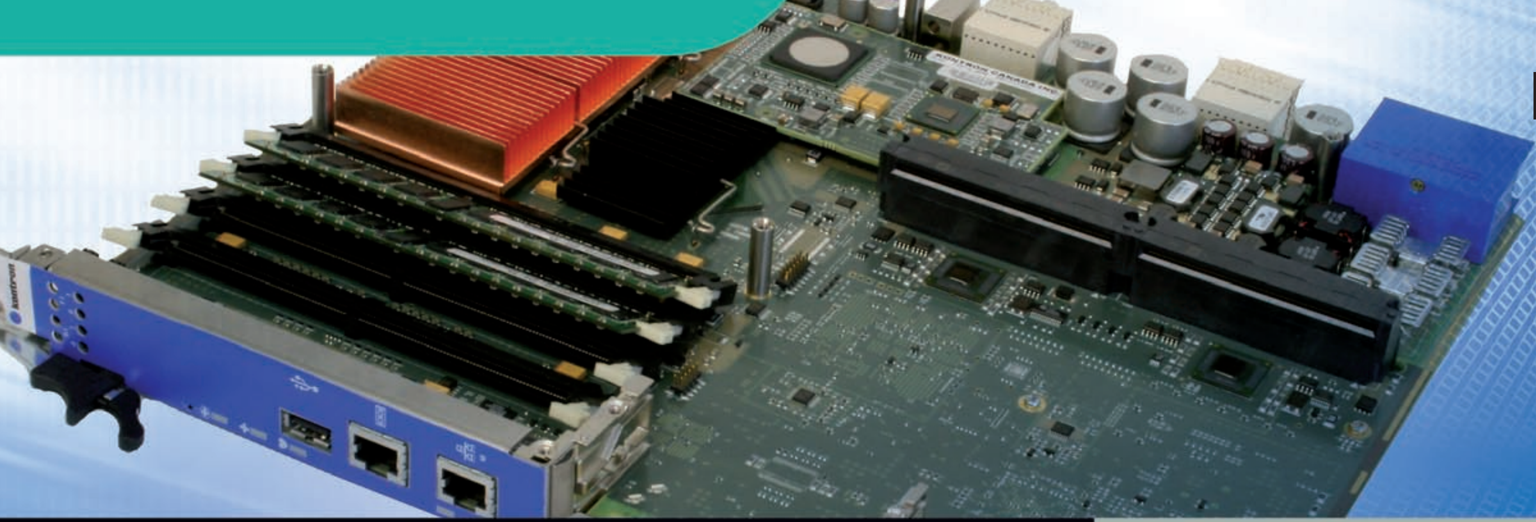

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- Dual Dual-Gigabit on Fabric; SAS interface available

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AdvancedTCA Processor Board
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AdvancedTCA AMC Carrier Board
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Kontron AT8902
AdvancedTCA Base/Fabric Switch
- AdvancedTCA Base / Fabric Interface switch with dual AdvancedMC slot support
- Fabric Interface uplinks & comprehensive protocol support

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1-888-294-4558 - sales@us.kontron.com — EMEA: +49 0 800 7253756 - Asia: +886 2 2910 3532 across a LAN. Such a system might find a home in a hotel, allowing it to offer on-demand movies to guests. Built using the MicroTCA structure, this media server would be compact enough and at a low enough cost to be appropriate even for modest establishments.

Because MicroTCA allows the creation of systems with only a few modules, developers can create systems inexpensive enough for small or home office applications. With just a DSP and processor module, developers could create a video conferencing system for the small office market. The Ethernet interfaces on the processor module handle the connection to the company LAN, while the DSP provides the audio and video codec.

Wireless future for AdvancedMC

Additional applications will arise as new AdvancedMC modules come on the market. One area that is currently receiving considerable attention by module developers is wireless networking. With the addition of a WiMAX interface on an AdvancedMC module, systems such as wireless networking base stations become possible. Large AdvancedTCA systems might serve as a metropolitan base station, while small MicroTCA systems can bring that capability down to a mobile platform size. With the right security features in place, a WiMAX MicroTCA system could be installed in a military vehicle such as a Humvee and serve as a mobile network hub for communications, command, and control.

The AdvancedMC specification is the key to the success of such applications. Developers can take advantage of AdvancedMC modularity to create many different systems with only a few basic module types. This simplifies the stocking and supply of components for system developers and users, reducing the costs of development, production, and ownership. The capacity of these modules means that they can play in high-end applications, while the MicroTCA specification allows them to also serve cost-sensitive applications. Addressing both high-end and cost-sensitive markets provides AdvancedMC modules with an opportunity that many analysts put in the multibillion-dollar range and helps ensure their future as the foundation of communications system designs.

***Thanh Nguyen** is the manager of the product management group and architect at Emerson Network Power Embedded Computing, where he is responsible for the company's AdvancedTCA, AdvancedMC, and signaling protocol product lines, including long-term strategic vision. Thanh has 20 years of experience in the telecom and embedded industry, with a strong emphasis on telecom infrastructure technologies such as ISDN, ATM, MPLS, VoIP, and NPU. Thanh is a graduate of Penn State University.*

To learn more, contact Thanh at:

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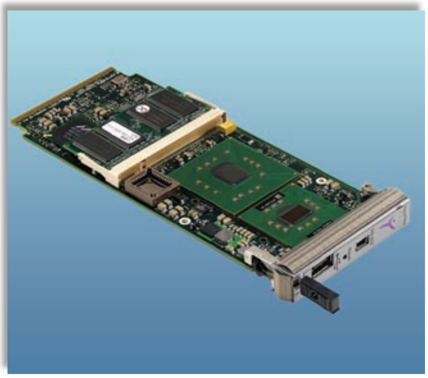

Emerson Network Power RSC# 24990
Model: Half-height KosaiPM

MEN Micro RSC# 30177
Model: F14 cPCI SBC

Diversified Technology, Inc. RSC# 32147
Model: ATC5231

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June 2005

WWW

AdvancedTCA

Company/Model No.	Processor Type	Processor Speed	PICMG 2.16	Rugged	RoHS
ADLINK Technology www.adlinktech.com					
aTCA-6891	Xeon	2.8 GHz			•
Continuous Computing www.ccpu.com					
ATCA-XE20	Dual LV Xeon	2.8 GHz			
Diversified Technology www.atcatogo.com					
AdvancedTCA Node	Xeon	3.06 GHz			
ATC5231	Dual LV Xeon	3.06 GHz			
ATC5232	Dual LV Xeon	3.06 GHz			
ATS2148	PowerQUICC III	1.3 GHz			•
Embedded Planet www.embeddedplanet.com					
EP8548A	MPC8548 PowerQUICC III	1.5 GHz			
Emerson Network Power Embedded Computing www.artesyncp.com					
KatanaPPB	PowerPPC 7447A or 7448	1.0 GHz			•
KatanaQp	Dual PowerPC MPC7447A or MPC7448	1.3 GHz			•
Half-height KosaiPM	Pentium M	1.8 GHz			•
Pm8560	MPC8560 PowerQUICC III	1.0 GHz	•		•
GE Fanuc Embedded Systems www.sbs.com					
ATCA-7820 CPU Blade	Xeon LV	2.0 GHz			
Hewlett-Packard www.hp.com					
bc2100	Dual Xeon	2.8 GHz			
Intel www.intel.com					
MPCBL0001	Dual Xeon	2.0 GHz			
MPCBL0010	Xeon LV	2.8 GHz			
MPCBL0020	Pentium M	2.0 GHz			
MPCBL0030	Dual Xeon	2.8 GHz			
MPCBL0040	Dual LV Xeon	2.0 GHz			
MPCBL0050 SBC	Xeon LV 5138	2.33 GHz			•
Kontron www.kontron.com					
AT8000	Dual Xeon	2.0 GHz			•
AT8001	Xeon	2.8 GHz			•
AT8020	Dual Dual-Core Xeon	2.0 GHz			•
Mercury Computer Systems www.mc.com					
PCR-150	Pentium M	1.4 GHz			
NMS Communications www.nmscommunications.com					
MG-7000A	PowerPC				
Sun Microsystems www.sun.com					
CP3010 SPARC	Single or dual UltraSPARC IIIi	1.1 GHz			

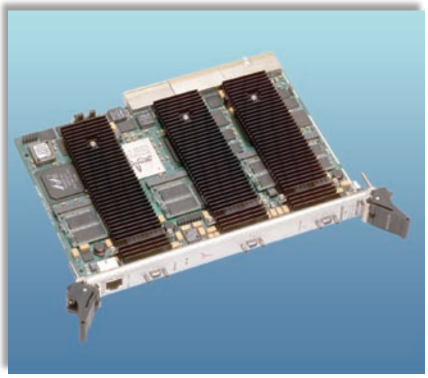
www.compactpci-systems.com/products

CompactPCI

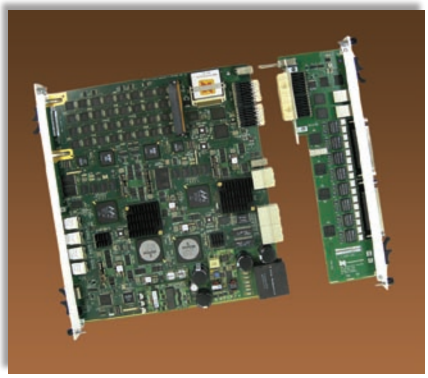
Company/Model No.	Processor Type	Processor Speed	PICMG 2.16	Rugged	RoHS
ADLINK Technology		www.adlinktech.com			
cPCI 3840	Pentium M	1.6 GHz			
Advanet		www.advanet.co.jp			
A6pci8019	Pentium M	2.0 GHz	•		•
Advantech eAutomation Group		www.eAutomationPro.com			
MIC-3321	Pentium M	2.0 GHz		•	
MIC-3390	Pentium M	2.0 GHz	•		
Aitech Defense Systems		www.rugged.com			
C901	PowerPC 7448	1.4 GHz		•	
C901L	PowerPC 7448	1.0 GHz		•	
C903	PowerPC	600 MHz		•	
S950	750FX	733 MHz			•
Alphi Technology		www.alphitech.com			
Actis CSBX-3545	PowerQUICC	1.2 GHz			
Concurrent Technologies		www.gocct.com			
PP410/03x 2xPMC SBC	Core Duo	2.0 GHz	•	•	•
TP 30x/32x	Pentium M	1.8 GHz			
Continuous Computing		www.ccpu.com			
cPCI-CD1215	Core Duo	1.5 GHz			
FlexCompute cPCI-PM1116	Pentium M	1.6 GHz			
FlexCompute cPCI-PM2118	Dual Pentium M	1.8 GHz	•		
Curtiss-Wright Embedded		www.cwcembedded.com			
SCP/DCP-1201	Core Duo/Solo	1.67 GHz		•	
SCP/DCP-122	750FX	800 MHz+			
SCP/DCP-124	PowerPC 7447a/7448	1000 MHz/1200 MHz		•	
Cyclone Microsystems		www.cyclone.com			
CPCI-824	PowerPC 440GX	667 MHz			
Dynatem		www.dynatem.com			
C3PM	Pentium M	1.8 GHz		•	
C3PM / C3RM	Pentium M	1.4 GHz		•	
CPM1	Pentium M	1.8 GHz	•	•	
CRM1 Rugged SBC	Pentium M	1.4 GHz	•	•	
Embedded Planet		www.embeddedplanet.com			
EP425M	XScale IXP425	533 MHz			
EP8343M	MPC8343E PowerQUICC II Pro	400 MHz			
EP834xM	834x (MPC8343 or MPC8347)	667 MHz			
EP85xxM	PowerQUICC III 85xx	1.0 GHz			
Emerson Network Power Embedded Computing		www.artesyncp.com			
Katana 3750	PowerPC PPC750FX	800 MHz	•		
Katana 3752	750GX	1.0 GHz	•		
Katana750i	750FX	800 MHz	•		
Katana752i	PowerPC 750GX	1.0 GHz	•		
GE Fanuc Embedded Systems		www.gefanucembedded.com			
C2K Single Board CP	PowerPC G4	1.0 GHz	•	•	
CK5	7447A G4	1.0 GHz			

Kontron RSC# 30188
Model: CP306-Value

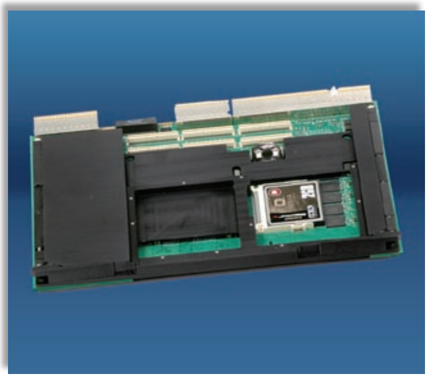
GE Fanuc Embedded Systems RSC# 32178
Model: C2K Single Board CP



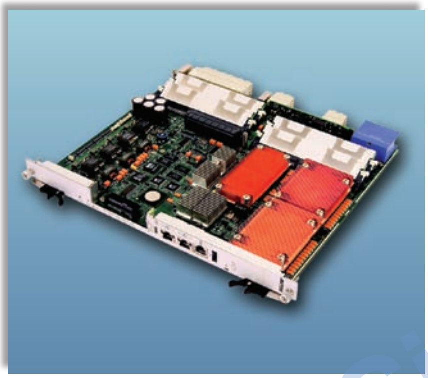
Emerson Network Power RSC# 30612
Model: Katana3750



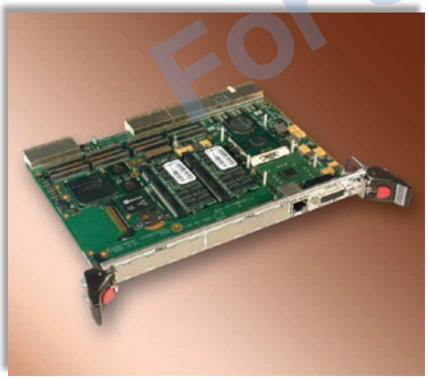
NMS Communications RSC# 32169
Model: MG 7000A



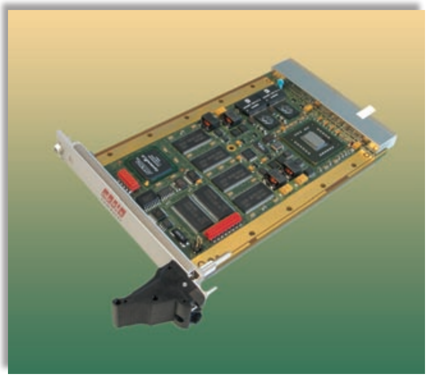
Dynatem RSC# 30374
Model: CRM1 Rugged SBC



Intel RSC# 32449
Model: MPCBL0050 SBC



Concurrent Technologies, Inc. RSC# 32181
Model: PP410/03x



Alphi Technology RSC# 32276
Model: Actis CSBX-3545

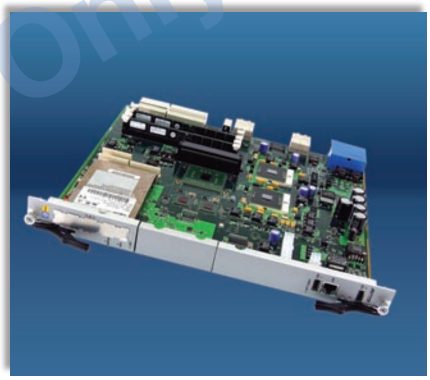
CompactPCI

Company/Model No.	Processor Type	Processor Speed	PICMG 2.16	Rugged	RoHS
GE Fanuc Embedded Systems (continued)		www.gefanucembedded.com			
CL9	Celeron/Pentium	600 MHz/1.8 GHz			
CP9	Pentium M	1.8 GHz			•
CPCI-7055	750FX or 750GX PowerPC	1.0 GHz	•		
CPCI-7088	Pentium M	1.8 GHz			
CPCI-7506	Celeron M/Pentium M	1.3 GHz/1.8 GHz			
CPCI-7806	Celeron M/Pentium M	1.3 GHz/1.8 GHz			
CPCI-7808	Pentium M	1.8 GHz			
CR3	Celeron	650 MHz			
CR4	Pentium M	1.4 GHz		•	
CR7	Celeron/Pentium III	566 MHz/1000 MHz		•	
CR9	Pentium M	1.8 GHz			•
CT7	Celeron/Pentium III	566 MHz/850 MHz			
CT9	Pentium M	1.8 GHz			•
CV1	7447A G4	1.0 GHz		•	
RL4	MPC 755/IBM PPC	400 MHz/750 MHz			
General Dynamics		www.gdcanada.com			
PC3010	Pentium M	1.8 GHz		•	
PC6020	Pentium M	1.6 GHz		•	
General Micro Systems		www.gms4vme.com			
C161 Aurora	Pentium III	1.0 GHz			
C165 Miser	Celeron	850 MHz			
C265 Condor	Pentium M	2.0 GHz+	•		
CC61x Rock	Pentium M	1.4 GHz		•	
C267 Eagle	Pentium M	2.0 GHz			
C512 Freedom	PowerPC	800 MHz			
Inova		www.inova-computers.de			
ICP-CM/ICP-PM	Pentium M	2.0 GHz	•		
Intel		www.intel.com			
NetStructure ZT 5515	Pentium 4M	1.2 GHz	•		
Interface Concept		www.interfaceconcept.com			
IC-e6-cPCIa	MPC7447A/MPC7448	1.0 GHz/1.4 GHz			•
IC-e6-cPCIb	1 or 2 MPC7448	1.0 GHz/1.4 GHz			•
Kontron		www.kontron.com			
CP303	Pentium III M	933 MHz			•
CP303-V	Celeron	1.0 GHz			•
CP306-V	Celeron M	1.8 GHz			
CP307	Core Solo/Core Duo	2.0 GHz			•
CP320	MPC8240	250 MHz			•
CP321	MPC8245	330 MHz			•
CP605	Pentium 4 M	2.2 GHz	•		•
CP620	750CX(E)	400/600 MHz	•		•
CP6000-Value	Celeron	1.0 GHz	•		
CP6010	Dual Xeon LV	2.4 GHz	•		•
CP6011	Pentium M	2.0 GHz	•		•

CompactPCI

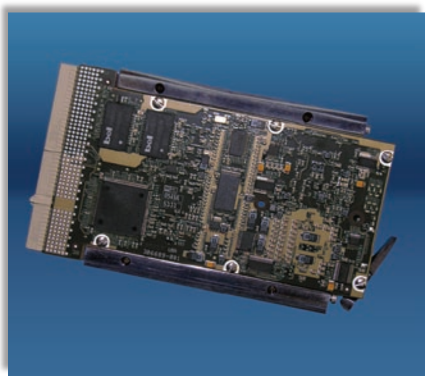
Company/Model No.	Processor Type	Processor Speed	PICMG 2.16	Rugged	RoHS
CP6012 Core Duo	Core Duo	2.0 GHz	•		
CP6500-V	ULV/LV Celeron	400 MHz/1.0 GHz	•		•
DT64	Pentium III	1.26 GHz	•		
MEN Micro		www.menmicro.com			
D3A/D3B/D3C	MPC8245	300 MHz			
D4	Mobile Pentium 4	2.2 GHz			
D5C	MPC8540	800 MHz			
D6	Pentium M	2.0 GHz		•	
D601 cPCI SBC	Pentium M	1.4 GHz		•	
F9	Pentium M	1.8 GHz		•	
F11	Pentium III/Celeron	933 MHz/650 MHz			•
F11N	Pentium III/Celeron	933 MHz/650 MHz			•
F12	MPC5200	384 MHz		•	
F13	PowerQUICC III	800 MHz		•	
F14	Pentium 4 M	2.0 GHz		•	
F15	Core Duo	2.0 GHz		•	
F17	Core 2 Duo	2.16 GHz		•	
F206N	Nios II	2.0 GHz		•	
Mercury Computer Systems		www.mc.com			
CCR-100 SBC	Pentium M	2.0 GHz	•		
CCR-200 SBC	Pentium 738/745/755	2.0 GHz	•		
CLA-100	UltraSPARC IIi+	650 MHz			
CP3-102	Dual PowerPC 7448	1.4 GHz		•	
CX6-200	Dual-Core Xeon	1.66 GHz			
Motorola Inc., Embedded Communications		www.motorola.com/computing			
CPCI-690+	750GX	1.0 GHz	•		
CPCI-6190	750GX	1.0 GHz	•		
CPCI-7145	Pentium M	1.8 GHz	•		
CPCI-7147	Pentium M	1.1 GHz	•		
CPCI-9120	IXP2400	600 MHz	•		
NEXCOM International		www.nexcom.com			
Peak 870VL2	Pentium 4	3.8 GHz			•
Performance Technologies		www.pt.com			
CPC5505	Pentium M	1.8 GHz	•		
CPC5564	Opteron 940	2.2 GHz	•		
Radstone Embedded Computing		www.radstone.com			
CP1A	7448	1.4 GHz	•	•	
IMP1A	775/7410	500 MHz			
IMP2A	7448	1.4 GHz			
SBE		www.sbei.net			
SAS iBlade	MPC7447A PowerPC	1.0 GHz	•		

Cyclone Microsystems RSC# 32168
Model: CPCI-824



GE Fanuc Embedded Systems RSC# 32180
Model: ATCA-7820 CPU Blade

Continuous Computing RSC# 31421
Model: FlexCompute cPCI-PM1116



General Dynamics RSC# 32209
Model: PC3010

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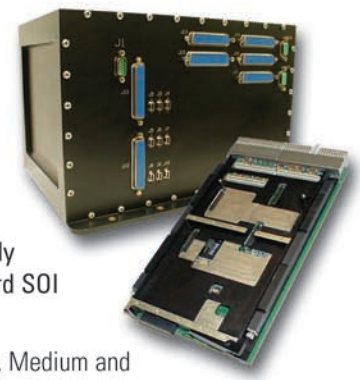

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*Total space applicability...*Aitech embedded products and sub-systems for space are ideal for Low, Medium and High Earth Orbit applications, lunar and Mars robotic vehicles and much more. Our products are used in the Space Shuttle, CEV program, MIR Space Station, International Space Station and other high profile satellite programs where highest performance and reliability are required.

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CARRIER BOARD: PMC

Dynamic Engineering
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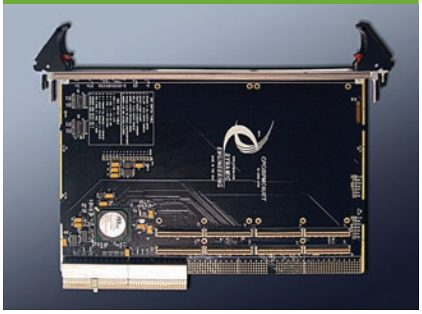
CPCIBPMC6U-ET **RSC No: 32278**



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www.compel.it
ATCA Chassis **RSC No: 32472**

Rack suitable for housing a combination of electronic boards in quantities of 16 pieces (23-inch width) or 14 pieces (19-inch width) • Special fans allow dissipation up to 200 W for the allocated signal board, the fans handling and control boards, and also the entire alarm and control system • Manufacturing tolerances for the single elements have been reduced with respect to the standard, with the aim of eliminating any critical aspect within the standard, linked to using the Root Sum Squared (RSS) probabilistic method for calculating the coupling tolerances

I/O: MULTIFUNCTION

Radstone Embedded Computing
www.radstone.com
MFIO-C6 Multifunction I/O **RSC No: 32281**

Rugged CompactPCI multifunction I/O card • MPC8270 PowerQUICC II processor • Eight analog inputs • Seven open collector 250 mA outputs • 48 LVTTL I/O channels • Five LVDS output ports • Five LVDS input ports • Two 10/100BASE-T Ethernet channels • Six serial ports • Designed to deliver maximum security with its 3-axis accelerometer to enable tamper detection, and secure instant erase SRAM, in which the contents are automatically destroyed at power-off or as a result of some key event • Occupies only a single slot, and thus represents a very cost-effective solution • Recognizes the requirement for today's military applications to interface to a variety of sensors, switches, and indicators, and delivers a high level of functionality as well as the flexibility for customers to selectively map their individual requirements

WIRELESS: GSM/GPRS

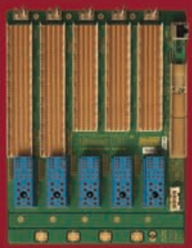
Inova Computers, Inc.
www.inova-computers.de
GSM/GPS Platform **RSC No: 32515**

Combining a PCI-serial controller with the latest communications module from Wavecom has produced a compact platform packed with all GSM/GPRS/GPS functions • An additional "SPIM" serial translation module provides RS-232, RS-422, RS-485, or IBIS communication while dedicated driver software permits integration under a range of popular operating systems • Robust TNC-R connectors form the physical interface to GSM or GPS antennae and front-panel LEDs indicate communication status

"If you would hit the mark,
you must aim a little above it."
-Henry Wadsworth Longfellow

cPCI/2.16

cPCI Express



ATCA

MicroTCA

PICMG compliance is just our starting point

Many in the industry can develop a basic PICMG-compliant backplane. But, with newer technologies like AdvancedTCA, CompactPCI Express, and MicroTCA, you want to go with the leader. We've led the PICMG backplane evolution and with our focus on signal integrity, quality, and innovative design, we'll continue to lead the way. With Elma Bustronic, you get good old-fashioned hard work, perseverance, and a drive for perfection. We don't just meet PICMG specifications, we aim higher.

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