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Embedded COMPUTING DESIGN

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EMBEDDED INDUSTRY PRODUCT REVIEW

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Process control,
Industrial automation,
Medical, Consumer,
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Communications

TECHNOLOGY FEATURE:
Hybrid digital signal controller enables next-generation automotive control systems

SPECIAL FEATURE:
Switch-fabric backplane technology

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As we approach 2004 ...

Bonnie I. Crutcher

We certainly can look back at 2003 and say it was a good year. Thanks to all of our vendors, advertisers, authors, and subscribers, *Embedded Computing Design* has definitely made an impact on the embedded community. In spite of the slow-down in the economy, the embedded industry continues to survive due to wireless technology boosting the ever-increasing needs of consumers, the continued development in the automotive and medical sectors, and the military and aerospace product sectors in support of homeland security, etc.

This special winter issue of ECD features a review of some of the most innovative products in the embedded world today. We have categorized these products by industry to appeal to the variety of professionals within our readership who are looking for such products for their development projects. If you do not see what you're looking for in this review, you can do an online advanced product search at www.opensystems-publishing.com.

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We expect the coming year to be another great year as we bring you more new product information, greater technical editorial, and a fifth issue – an embedded product catalog, scheduled for the spring. Visit www.embedded-computing.com to view the 2004 editorial calendar and to learn what's ahead for next year.

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INDUSTRY NEWS

Analog Devices integrates four 65-MSPS analog-to-digital converters in a single chip

Analog Devices Inc. has unveiled its new quad analog-to-digital converters (ADCs). Four ADCs are integrated onto one chip to meet the needs of high-density, space-constrained systems such as medical imaging systems, or space-constrained, multi-channel applications such as wireless communications base stations. Using serial, Low-Voltage Differential-Signaling (LVDS) data outputs, Analog Devices is able to integrate four ADCs onto a single chip, creating a solution that is compact, fast, cost-competitive, and power-efficient. The LVDS outputs dramatically reduce pin count, package size, number of board traces, and substrate noise.

"The demand for increased system resolution and speed is driving the number of ADCs used in these systems higher, so manufacturers are striving to pack more converters into smaller spaces," said Kevin Kattmann, product line director for High-Speed Converters, Analog Devices, Inc. "The serial LVDS digital outputs allow the new quad ADCs to radically simplify board layout, enabling more data conversion paths to be routed on a board."

Visit www.analog.com for more information.

IBM's Symphony technology embeds intelligence in blade servers to automatically meet business needs

IBM has announced a new computing system based on blade servers and IBM software designed to automate and reduce the cost of running an IT infrastructure.

The new offering, IBM Web Infrastructure Orchestration, can reduce the time it takes to deploy new applications or add extra capacity from weeks to hours and, at the same time, can double the utilization of compute resources.

"Providing automation technologies is the easy part, but bringing intelligence to automation is where customers can really start to see benefits. This new offering does that for the first time," said Jeff Benck, vice president of eServer BladeCenter, IBM. "This blade system and software combination brings intelligence to customers' data centers, helps drive down the overall cost of IT, and eliminates low-utilization of systems."

For more information about IBM, visit http://www.ibm.com.

Integration with embedded tool chains a must-have for test automation vendors

Embedded, test-automation-tool end users surveyed by VDC report that they are looking for test solutions that will work well with their current development environments and tools, and do not disrupt existing work habits. Although "ability to test software on target" was cited by almost 60 percent of respondents as the top selection criteria, end users reported that integration with existing development tools ranked second and was only 4 percent behind. This, coupled with over a third of end users citing "familiar interface," indicates that embedded developers and test engineers are looking for tools that will not require major changes to the way they work.

The leading test automation tools selection criteria are (in rank order):

- Ability to test software on target
- Integration with existing development tools
- Ability to test software on host development platform
- Familiar interface
- Automatic test case generation
- Defect tracking capabilities
- Easy to learn test scripting language
- Platform independence
- Integration with existing configuration management software

"Test automation vendors need to provide seamless integration with the most popular software development tools," said Chris Lanfear, Director of VDC's Embedded Software Research Group. He adds, "Developers are not looking for test tools that will slow down their work or force them to change their existing tool chains."

VDC is a technology market research and consulting firm that specializes in industrial and commercial electronics, computing, communications, software, and power systems markets. For more information, visit www.vdc-corp.com.

TECHNOLOGY PARTNERSHIPS

Kineto Wireless selects GoAhead's availability and management middleware

GoAhead Software has announced the selection of its integrated suite of reliability middleware by Kineto Wireless for its INC-5501, the key component behind the Kineto Mobile over Wireless LAN (MoWLAN) solution for service providers. GoAhead is providing Kineto with a key enabling technology that will help ensure their system meets the traditional telecommunications industry standard for 99.999 percent system uptime.

"We chose GoAhead for two reasons," said John Perry, vice president of engineering for Kineto. "First, high availability is an absolute must-have for our system, and GoAhead's SelfReliant delivers on that requirement. Second, by implementing GoAhead's commercial-off-the-shelf product, we can devote more resources to value-added application development rather than underlying platform services, thereby saving time and money."

For further information, visit www.goahead.com and www.kinetowireless.com.

Transmeta selects Fujitsu Semiconductor as the first foundry for its 90nm generation of Efficeon processors

Transmeta has announced that it has selected Fujitsu as the first foundry for its 90nm (90 nanometer = 0.09-micron) generation of Efficeon processors. Engineering teams from the two companies have been working closely together to port the Efficeon design to Fujitsu's CS100 90nm CMOS process, which features transistors with an industry-leading 40nm physical gate length. Volume production for the 90nm version of Efficeon is slated for the second half of 2004.

Transmeta's 90nm Efficeon processors will offer a strong performance upgrade path for customers launching systems based on the 0.13-micron generation of Efficeon processors.

To learn more about Transmeta, visit www.transmeta.com.

GET Engineering partners with Dolch to offer portable NTDS analyzers worldwide

GET Engineering Corporation has announced that it has partnered with Dolch Computer Systems, Inc. to deliver portable NTDS analyzers worldwide.

GET Engineering manufactures Naval Tactical Data Systems (NTDS) products that are deployed in tactical applications of all classes of U.S. Naval and NATO vessels. Dolch will provide GET with rugged laptop and luggable units. Under this partnership, GET will be able to deliver portable units that have the unique ability to monitor, debug, and analyze NTDS information that is passed through data channels. The portable analyzers can quickly analyze hardware and software performance, analyze peak traffic, evaluate timing and verify information design specifications.

"GET selected Dolch because of their ability to deliver computers that were portable, rugged, and offered the best performance in the industry," stated Robert Ruhe, chief executive officer of GET Engineering. "Dolch computers allow users to analyze NTDS data whether they are shipboard or in a land-based test facility. This partnership will provide an ideal solution for anyone using NTDS technology."

For more information, visit http://www.getntds.com and http://www.DolchPR.com.

CONFERENCES & AWARDS

ChipWrights' visual signal processing innovation earns Frost & Sullivan's 2003 Excellence in Technology Award

ChipWrights has announced that it has received Frost & Sullivan's 2003 Excellence in Technology of the Year Award for its pioneering work in Visual Image Signal Processors (VISPs). ChipWrights' ViSP technology offers OEMs a new kind of DSP that combines high performance, full programmability, scalability, low power, and low cost to deliver powerful digital imaging solutions.

"There is clearly a need for new digital signal processors to handle the imaging problem," said John Redford, Chief Technology Officer, "While many DSPs have been used for imaging, most were originally designed to serve the communications market. They are less efficient at imaging than an architecture that was designed from the ground up specifically for it."

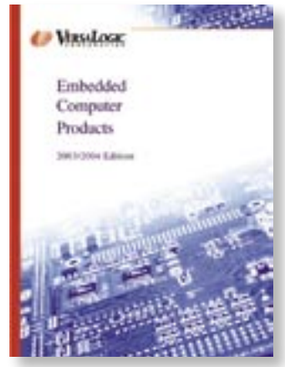
Frost & Sullivan Excellence in Emerging Technologies Awards Banquet was held in Boston on September 24. It honored companies and individuals for technical developments that have the opportunity for the fastest growth in their industries. The award recipients have identified emerging trends before they have become the standard in the marketplace and have created advanced technologies that will catalyze industries in the near future. For further information, visit www.frost.com.

Additional information about ChipWrights is available at www.chipwrights.com.

MEDIA & EDUCATION

New embedded computer products catalog

VersaLogic Corp. has announced the release of their latest embedded computer products catalog. The catalog provides details on the company's three product lines: PC/104, STD 32, and EBX. These embedded computer platforms are designed for rugged applications where reliability and long-term availability are critical. A special section on VersaLogic's engineering capabilities and quality assurance program is also included. Embedded engineers looking for long-term, off-the-shelf availability and robust engineering support will find the catalog a very convenient selection guide. For more information and to request a copy, send e-mail to info@VersaLogic.com or visit www.VersaLogic.com.



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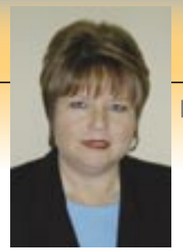

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Linux news

By Bonnie Crutcher

SnapGear announces embedded Linux support for new Intel gigabit network processors

SnapGear Inc., a leader in embedded Linux security, has announced Linux platform support for network processors based on Intel XScale technology. SnapGear will add support for the Intel IXP2400, Intel IXP2800, and Intel IXP2850 network processors. The optimized Linux kernel provides wire speed throughput while delivering security functions such as firewall and multi-VPN support.

"Intel continues to focus on providing cost-effective, power-efficient network processor solutions that extend from small office equipment to service providers' core switching equipment," said Doug Davis, General Manager, Intel Network Processor Division. "Working with companies like SnapGear helps ensure broad support for embedded Linux for networking appliances and secure Internet communications."

For more information, visit www.snapgear.org.

NTT Data Intellilink joins OSDL

The Open Source Development Labs (OSDL) has announced that NTT Data Intellilink, a subsidiary of NTT Data, one of the largest systems integrators in Japan, has joined the lab as its newest member.

NTT Data Intellilink, which partners with NTT Data and the NTT group companies on enterprise systems support, was an early champion of open source software solutions. The firm has expertise in open source and Linux-based systems, including feature and performance tuning, deployment, office automation, data base implementation, Web serving, middleware, and more.

"We're pleased to have NTT Data Intellilink, one of Japan's most important systems integration companies, working with us as a new member to advance Linux in the world's second largest economy," said Stuart Cohen, CEO of OSDL. "We look forward to NTT Data Intellilink's contributions working with OSDL, customers, and the Linux development community as we broaden our commitment in Japan."

Visit OSDL on the Web at www.osdl.org.

LynuxWorks' LynxOS-178 onboard Bombardier Challenger 300 aircraft

Rockwell Collins is using LynuxWorks' LynxOS-178 as the embedded Real-Time Operating System (RTOS) in the Adaptive Flight Display systems onboard the Bombardier Challenger 300 aircraft. The aircraft recently received FAA, JAA, and Transport Canada certification and is completing flight tests in anticipation of first aircraft delivery.

"The deployment of LynxOS-178 in the Bombardier Challenger 300 aircraft demonstrates how our collaboration with Rockwell Collins has led to the development of ground breaking technology for the military and aerospace industry," said Bob Morris, vice president of sales and marketing for LynuxWorks.

More information is available at www.lynuxworks.com.

MontaVista Software advances enhanced Linux platform for telecommunications and networking

MontaVista Software, Inc. has announced MontaVista Linux Carrier Grade Edition 3.1 (CGE), the next generation of the company's carrier-grade Linux operating system and development environment.

MontaVista Linux Carrier Grade Edition 3.1 advances earlier versions of CGE with support for key emerging industry standards designed for high availability and telecommunications. It also adds support for the IBM PowerPC architecture. CGE 3.1 combines full support for the PICMG 3.0 Advanced Telecommunications Computing Architecture (AdvancedTCA) technology with support for key, high-availability APIs from the Service Availability (SA) Forum. CGE 3.1 implements APIs from the SA Forum's Application Interface Specification (AIS) for clustering. Other highlights of the new product are increased support for standards including a Native POSIX Thread Library (NPTL). The third release of MontaVista Linux Carrier Grade Edition includes an expanded ecosystem.

Additional information is available at www.montavista.com.

Wind River hops on embedded Linux bandwagon

Wind River has launched its first official support for embedded Linux. For its initial foray into the embedded Linux market, the company is targeting its $4,000 visionProbe II hardware bring-up tool at embedded Linux system-level software development. Company officials say they plan a step-by-step approach toward embedded Linux, suggesting more Linux-related announcements lie ahead for the embedded software giant.

Late in July 2003 there were some hints that Wind River might be planning a strategic shift toward Linux when Wind River Chairman Jerry Fiddler was quoted in the *San Jose Mercury News* as saying, "Far from running from Linux, most commercial companies like Wind River are trying to figure out how to embrace it and provide the long-term support that mainstream customers require." Wind River had taken a pretty absolute stance against Linux, according to Senior VP of Products Dave Fraser. "But, after much analysis, the conclusion is that there's a business opportunity, that Linux is a massive force, and it's here to stay in the embedded market."

For more information, visit www.windriver.com.

Implementing fault tolerant systems with Windows CE .NET

By Nat Frampton and Dr. Richard Lee

A variety of applications ranging from industrial control to home entertainment appliances share a common goal – the goal of delivering highly available services on lower cost software and hardware. Users of these products expect a degree of reliability significantly greater than that which desktop computers can deliver. The growth in the capability and reliability of platform hardware enables increasingly rich services from a single device. As complexity increases, software errors become an important cause of failure. Improving dependability requires that systems detect and remediate software errors without loss of service. This article will discuss the basic concepts and approaches to software fault tolerance for building robust, reliable embedded applications, and will describe how Microsoft Windows CE .NET can support such systems.

Microsoft Windows CE .NET has proven to deliver stable, real-time operating system services, making it an increasingly popular software platform for deploying complex solutions. Throughout the past four years, Windows CE .NET has been the catalyst for building systems that deliver Web integration, elaborate user interfaces, and data collection on both specialized and commercial hardware platforms.

Building critical systems for flight control or life support, for example, require carefully engineered hardware and software to achieve the rigorous dependability levels. However, development costs can be quite considerable when trying to achieve these levels of performance. Therefore, reaching zero failures might not be the goal of development for reasons of cost.

For example, a rare state of a system's hard drive after a power failure might result in a dialog box presenting an incorrect message. If users can tolerate such a glitch in the system, then developers still consider the product shippable. For the many applications where developers can manage system failure, they can create reliable solutions based on both software and hardware off-the-shelf subsystems and keep within budget constraints.

System dependability

Dependability of a computing system is the ability to deliver trustworthy service. Applications might emphasize different attributes of dependability, including:

- Availability: readiness for correct service
- Reliability: the continuity of that service
- Safety: the avoidance of catastrophic consequences
- Security: the prevention of un-authorized access

The function of a system, is what the system is intended to do, as described by the functional specification. A failure occurs when the service does not comply with the specification. An error is a system state, which may lead to failure. An error is detected if an error message or signal is produced within the system, or latent if not detected. A fault is the cause of an error and is active when it results in an error; otherwise, it is dormant. Software faults are persistent, not transient, though they may be hard to reproduce and are always due to flaws in the system design.

Fault tolerance is the ability of a system to deliver correct service in the presence of faults through error processing – removing the system error state – and by treating the source of the fault.

A system achieves fault tolerance through redundancy. Reliability improves when things fail independently so that a failure in one part is not likely to happen concurrently with failures in the parallel components, thus increasing the probability of a correct result.

System software achieves fault tolerance through algorithmic diversity, computing the action through independent paths, and judging the results. This adds complexity to the system, and will only improve system reliability if the gains made by the added code are not offset by the new faults. It is OS independent other than there being enough speed and space to run the extra tasks.

Building fault tolerant software

Creating fault tolerant behavior in a hardware-software system is a complex process. The classification of failures and their consequences are unique to the services provided.

Approaches for achieving a particular level of dependability vary. Fault prevention in the design phase, and fault removal through maintenance, are important means for delivering reliable software. Reducing the time required to restart a service may improve the overall availability more than would an equivalent investment in fault reduction. At Vibren, fault prevention takes place in the design phase through code reviews and walkthroughs. In addition, fault remediation through testing and maintenance remain important and cost-effective parts of the process of delivering reliable software.

Specification and partitioning

Successful projects always begin with the thorough specification of service functionality, performance, dependability, and any special service modes, such as fail-safe shutdown. A key part of the specification is the identification and classification of faults that the system must tolerate or otherwise remediate. The specification should define fault and error scenarios and consider system response when faults occur in coincidence. A careful specification is essential in making an informed choice when allocating limited development resources between fault avoidance and fault tolerance efforts.

Partitioning the system into subsystems defines the independent error containment boundaries where a fault in one subsystem can be prevented from propagating errors to other subsystems. Here, CE .NET, with support for multiple processes running in protected memory, helps enforce subsystem independence. Partitioning should reflect the hierarchy of fault tolerance, identifying those faults handled locally, and those that impact several subsystems. The specified dependability requirements are then apportioned to the appropriate subsystem.

Designing for tolerance

The Recovery Block (RB) or acceptance test-based design makes use of a primary and one or more alternate program blocks, each of which perform specified operations, but in different ways. The RB program tests the primary code block results for correctness and invokes alternate code blocks when failure is detected, as shown in the code example in Figure 1.

```
CurrentMethod = PrimaryMethod( );

do {
  result = CurrentMethod();

  if (AcceptanceTest(result) == OK)
    return result;

} while (CurrentMethod =
NextAlternameMethod());

fail();
```

Figure 1

For the RB design to improve reliability over the primary method alone, developers must carefully design and implement the acceptance test. An imperfect test might decrease reliability by reporting failure when the primary method yields correct results. Additionally, the serial execution of the alternate modules can compromise execution deadlines in a real-time environment.

N-Version Programming (NVP), or the voter-based approach, uses parallel execution of N>=2 independently developed, functionally equivalent software versions. The output from all versions is examined to determine the correct output by vote. The voter logic does not need to understand the details of the application and might be more simple and general-purpose than the analogous acceptance test code.

Both RB and NVP depend on design diversity, an expensive process with the potential to inject new logic errors into the system. Programs often fail under a particular combination of input values. Introducing small changes in the input values may be sufficient to allow the software to execute without failure. This deliberate perturbation of the input can be done serially, followed by an acceptance test in data diverse analog of the recovery block approach, or a vector of perturbed data can be fed through the algorithm with a voter selecting the correct result. The latter approach, sometimes called N-copy Programming or NCP because of its similarity to NVP, might have considerably complex voter code if the perturbed input data results in different but acceptable outputs.

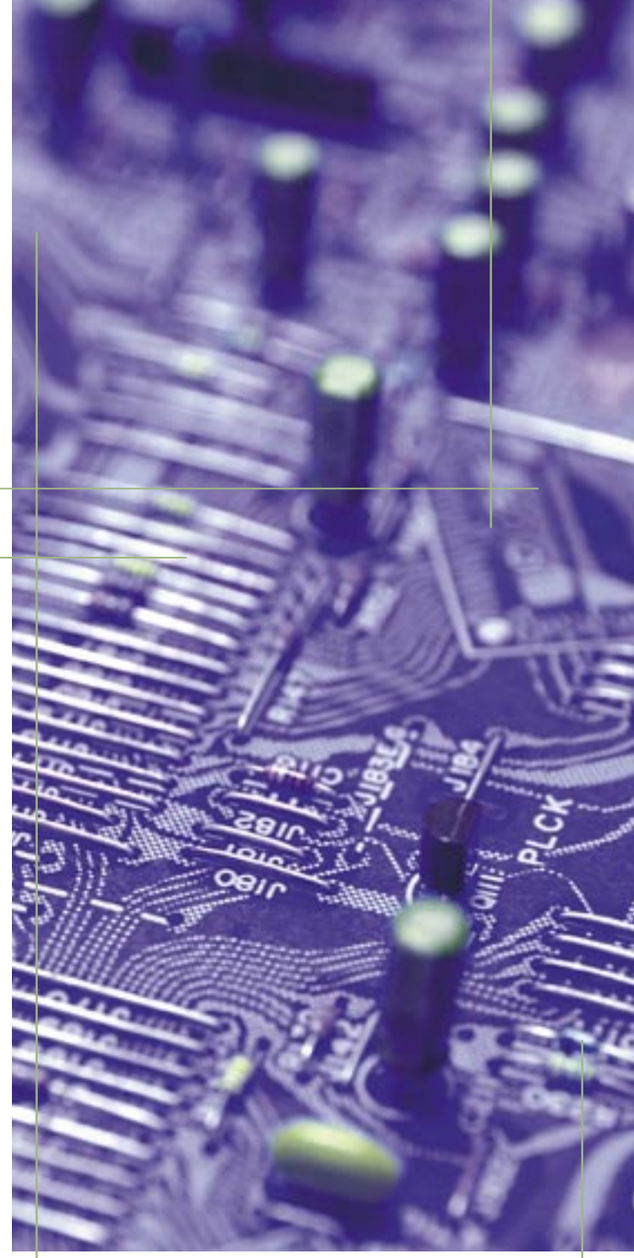
Software faults are an increasingly important cause of failure in complex embedded systems built from off-the-shelf software and hardware components. Designing in a framework for detecting faults and recovering from errors may be a cost-effective manner to improve system reliability.

Since entering the embedded community, Microsoft Windows CE has enabled a new class of complex and robust embedded software products. With complexity comes the need to acknowledge and deal with software faults. Microsoft has provided a rich framework of operating system features and capabilities that may be leveraged to improve system reliability through software fault-tolerant design. Understanding these design requirements will be imperative to ensuring the reliability and dependability of the system.

For more information about implementing fault tolerant systems with Windows CE .NET and to view a longer, in-depth version of this article, visit www.vibren.com.

Factors that influence the decision to change to switch-fabric backplane technology

By Jeffrey L. Small



Making the decision to convert to a switch-fabric backplane can be daunting. In this increasingly mechanized world, backplanes must also keep up with increasing bandwidth demands. This challenge of meeting bandwidth demands has spurred several backplane technologies, including multi-point and point-to-point, and now switch fabric has joined the lot as the newest system in the industry. Although fabrics will indeed be the heart of network switches and routers in the near future, it might or might not be timely for designers to make this change. This article will provide system designers with an overview of the costs and rewards of making this paradigm shift and will aid them in facilitating the decision-making process, ultimately determining whether such a change is truly necessary.

Existing architectures

Bandwidth has been, and will continue to be, a key issue when working with backplane technology. The constant demand for high performance has pushed bus-based systems to the limit. Backplanes are often serviced by one of several bus systems, including multi-drop, parallel bus and shared bus, shared memory, and point-to-point systems. Multi-drop backplanes are ones in which the driver sends the data to more than one receiver, whereas point-to-point systems are ones in which the driver sends data to only one receiver.

Parallel or shared bus architectures were once the workhorse of the industry for a number of reasons. For example, parallel backplanes can provide higher throughput over relatively short distances, albeit at relatively slow speeds. Additionally, although loading on the bus increases by adding parallel data lines, data throughput can be increased with relative ease. However, this comes at a cost. Due to the number and size of devices needed for a parallel system, power requirements are often prohibitive. Shared bus systems are confined to low-bandwidth applications because a data packet can be blocked from transmission by another transition taking place on the bus. Since the driver card communicates with all receiver cards, it allows only one data packet to be transmitted at a time. The widely used Peripheral Component Interconnect (PCI) standard is an example of a bus-based architecture, which is limited to 64 bits at 133 MHz.

In order to combat this initial bandwidth problem, multi-port shared memory systems arrived on the scene in the late 1980s. This type of architecture allows for

simultaneous memory access for each output sending data. Although it would appear that these systems were the answer to the ever-demanding problem of bandwidth, shared memory systems, too, are both difficult and expensive to implement.

Throughput requirements demanded a solution to the limitations of a parallel, multi-point backplane. Hence, in the late 1990s, serial point-to-point backplanes became a popular method for data transmission. The ease of design, combined with faster transmission frequency, seemed to be a solid answer to the pitfalls of other bus systems. However, the popularity of point-to-point systems was short-lived as technology quickly passed the practicality of such systems in favor of switch fabric systems.

Overall, the bus architecture itself places limits on:

- Operating frequency
- Signal propagation delay
- Electrical loading

Propagation delay limits the physical distance a bus can span, while electrical loading limits the number of devices it can connect. Pragmatically speaking, cables cannot increase physical distances.

Since many of these architectures are riddled with pitfalls, the industry has begun to turn to switch-fabric architecture. In fact, many would argue that both the present and the future of the industry are in this protocol. Before jumping on the switch-fabric bandwagon, however, it is first important to introduce many of the topologies of switch fabric and the benefits and disadvantages of each.

Switch-fabric architecture

Although all switch fabrics are not equal, they generally provide both the power and flexibility needed to build cutting-edge communications equipment and offer a degree of scalability and reliability not found in the previously mentioned bus-based ICs.

The term "fabric" is accurate in describing this architecture, as any single node can connect to any other node through data paths that resemble the woven fibers of cloth material (Figure 1). End points function as a type of bridge to existing components. Thus, open-switch architecture allows many devices to engage in the transactional process of communication, meaning the components simultaneously act as both a sender and receiver of information. Many existing topologies can support ever-scalable bandwidth. With switch fabric, when one route fails, traffic is redirected onto an alternate route. Using point-to-point connections, a single end-point failure does not affect the rest of the system. Contrasted with a bus model, in which a single poorly functioning device can diffuse the entire bus, the advantages of a switch fabric seem obvious. Furthermore, the point-to-point connection with many switch fabrics facilitates device addition and removal.

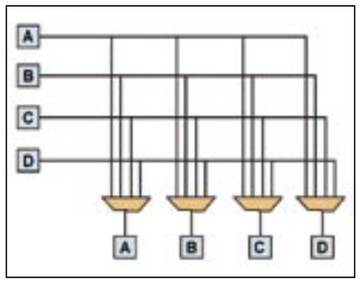


Figure 1

Basic switch-fabric topologies

A truly comprehensive discussion of switch fabric is not possible in this article, as many topologies exist, each with a history and its own set of costs and rewards. The following paragraphs, however, at least introduce the basic topologies and the benefits of each.

Ring topology is a popular approach to configuring networks (Figure 2). Data packets flow in one direction with each node first receiving the data and then transmitting it to the next node in the sequence. Ease of design and lack of data backlogs (bottlenecks) make this topology attractive. However, if a single channel between any two nodes fails, then the entire system ceases to function. Dual ring and multiple ring systems also exist, which can increase the integrity of the system should a channel or node failure occur.

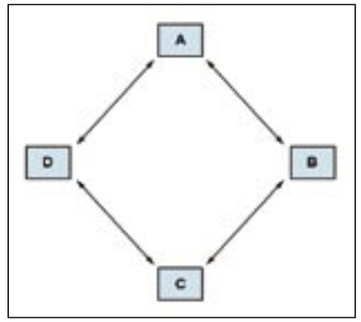


Figure 2

Star topology is centralized and supports only one fabric slot on the backplane (Figure 3). The dual star supports two fabric slots on the backplane, providing redundancy. This system is generally easy to control, as all traffic originates from the hub of the star. Similar to other structures, however, the star network is susceptible to data backlog and bottlenecking, as well as failure problems at the central site. Star topologies have lower bandwidth than mesh topologies but are more cost effective to design and maintain.

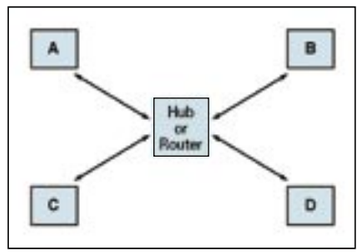


Figure 3

Mesh topology takes the star concept a step further (Figure 4). As interconnects are added to eliminate dead branches in a star network, a point is reached when all nodes have connections to all other nodes. At this point, the hierarchy disappears and each node can become an end point, a router, or both. Each node switches its own traffic, and all nodes are equal in a peer-to-peer system. Many in the industry argue that mesh topology fabrics are the topology of choice.

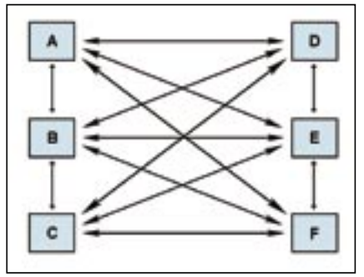


Figure 4

Transitioning to switch fabric

At face value, it appears that all signs point to yes when deciding to transition to a switch-fabric architecture. However, there are several factors to take into consideration before making such a paradigm shift. The first and possibly most important issue deals with design complexity. Jumping from a traditional parallel or point-to-point backplane to a switch fabric requires massive design efforts that often take months or even years to perfect. One key concern facing designers is the complexity associated with the layout of the switch matrix itself. One must consider matters of protocol dependencies, control and overhead requirements, and redundancy in case of failure.

Additionally, cost may indeed prove prohibitive when implementing a switch fabric design. Large chipsets and complex hardware combined with sizeable design teams and expensive design tools can add up to an unrealistic cost-to-throughput ratio. These costs can be slightly diminished, however. Interconnect speeds can be user-definable – scalable from 10 Mbits/sec to 2000 Mbits/sec per node. Thus, it is possible to start with lower-cost components and then upgrade as needed. Obviously, these lower-cost pieces are also lower speed. As a result, this cost-cutting measure might not solve the initial problem of speed.

Moreover, time to market may be a factor. With competition always increasing, transitioning to switch fabric may force a company into a non-competitive standpoint. It might, therefore, be more advantageous to redesign existing architecture to create additional generations, and thereby generate increased revenue with minimal R & D cost.

Finally, as with any backplane design, signal integrity is a primary concern. The

> "Although all switch fabrics are not equal, they generally provide both the power and flexibility needed to build cutting-edge communications equipment and offer a degree of scalability and reliability ..."

SIDEBAR

STARFABRIC

StarFabric opens the door to system disaggregation

By Tim Miller

For the last few generations of computers and communication systems, the predominant system interconnect has been a parallel bus structure, exemplified by the ubiquitous PCI bus. The speeds of these buses have increased to keep up with system demands. However, limitations in the number of connections and length of runs still exist, causing a demand for higher availability and guaranteed Quality of Service (QoS). This demand has spurred the development of switch fabrics and serial interconnects, such as StarFabric, which can handle different data types and deliver native QoS. Additionally, because StarFabric comprises a network of switches with point-to-point connections, it can offer a virtually limitless number of nodes.

System designers have come to appreciate that switch-fabric serial interconnect solutions provide greater architectural freedom, eliminating the performance bottlenecks, physical scaling, and system partitioning limitations of bus-based architectures. In addition, these interconnect solutions give rise to new types of architectures such as the functionally *disaggregated* system.

Disaggregation allows the architect to completely separate each system element into its own node in a switched fabric. As such, all system function elements, including processor elements, I/O boards, storage elements, and system management boards, directly connect to the serial switched interconnect. This model provides the freedom to mix and match system components to most optimally meet the needs of specific applications and users.

Disaggregation provides many benefits, including:

- High availability: A designer can make every element (including the fabric) of a system redundant.
- Ease of upgrade: As the performance or capacity demands on a functional element increase, a designer can simply upgrade to more or higher performing elements.
- Longer product life cycle: A designer can extend the life cycle of systems almost indefinitely through functional upgrades, and can add new functionality to existing disaggregated systems.

System disaggregation, however, places substantial requirements on the underlying interconnect technology. First, the interconnect technology must support processor-to-processor communication. This includes support for multiple processor types, such as x86, PowerPC, etc., and a range of other processing devices including microcontrollers, DSPs, NPUs, and application-specific processors such as security accelerators.

Second, the interconnect must provide for processor-to-device communication. As noted earlier, the types of devices that the interconnect must support are vast, including networks, storage, and many other application-specific I/O devices. The interconnect should be capable of handling control as well as data-plane traffic. For this reason, the system requires seamless support for PCI.

Finally, these systems process and move massive amounts of data. Thus, the interconnect must provide very high throughput. Today, 2.5-Gbit/sec links are required, and in the future, 10-Gbit/sec links will be the standard.

StarFabric is the first example of a production-quality, off-the-shelf switch interconnect that meets the requirements of system disaggregation. As disaggregation evolves to higher performance and higher speed interconnects, StarFabric will become the model for the PCI Express and Advanced Switching (AS) standards activities. With full PCI compatibility and four times the physical layer speed available with StarFabric, the PCI Express Base specification allows reuse of all software, but is limited in addressing model and scalability. The AS specification complements the Base specification by providing a higher level of capabilities already available in StarFabric's advanced features, such as peer-to-peer multiprocessing, message passing, and multiple address domains.

StarFabric chip-level components shipping today include the StarFabric six-port Switch and the PCI-to-StarFabric Bridge. Samples of the TDM-to-StarFabric Bridge are currently available. Designers have incorporated these components into an array of PCI cards, CompactPCI cards, and SBCs. Backplanes, chassis, and enclosures support these components, forming a rich and complete StarFabric solution.

Although originally developed by StarGen, the StarFabric Trade Association owns and manages the StarFabric architecture. The StarFabric Trade Association is an open-membership, non-profit industry organization that includes more than 25 leading communications and systems manufacturers. Tim Miller currently serves as president for the association. For more information, visit www.starfabric.org.

more complicated the design, the harder it is to control crosstalk, reflections, and power-supply noise. Thus, sophisticated routing techniques must be adhered to in order to ensure a clean, error-free environment. Since bus-based backplanes are commonplace and have been so for some time, expertise in the form of design, personnel, and support is ubiquitous and available to all in the industry.

To switch or not to switch

Current bus systems have likely reached their maximum potential. Additional improvements to these aging, bus-based systems will run headlong into the physical limitations set forth by voltage slew-rates and transmission-path characteristics. Switch fabrics are quickly becoming the heart of network switches and routers, as multiple advantages exist with this architecture. However, these advantages come at a cost, and not just a financial one. Transitioning to switch fabric may not be the most practical choice for all organizations. It is, therefore, incumbent on the designer to consider all factors before taking on a challenge of this intensity and magnitude. ECD

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RapidIO delivers low latency and high bandwidth for multi-computers

By Thomas Roberts

The RapidIO interconnect design accommodates the next-generation performance and transport requirements for chip-to-chip and board-to-board communications within embedded computer systems. Targeted for an initial bandwidth of between 1 and 12 Gbytes/sec per device pair, RapidIO technology is particularly well suited to applications that must meet stringent latency constraints and exceed the performance capabilities of a single processor.

RapidIO offers tremendous potential for increasing the bandwidth and, hence, overall performance of computing systems using multiple processors. This article will examine tests on a multi-computer system to exploit the potential of RapidIO. The test data validates the performance claims made by the RapidIO community and demonstrates the architecture's maturity for use in real-world applications.

Unlike other next-generation I/O technologies that augment or displace PCI or Ethernet, RapidIO technology fills the full spectrum of interconnect needs within an embedded system, starting with the microprocessor bus. Designers can integrate RapidIO interfaces directly into communications processors, digital signal processors (DSPs), Field Programmable Gate Arrays (FPGAs), and host processors enabling low-latency, tightly coupled multi-computing. The steady and predictable increase in microprocessor clock speeds has driven system bandwidth requirements beyond the capabilities of any bus architecture. RapidIO provides a direct memory-mapped interface, evolved from microprocessor buses, which designers can implement into part of an FPGA or into a small corner of a microprocessor.

The RapidIO Trade Association, a non-profit corporation governed by member companies, administers RapidIO as an open standard and directs its future development. RapidIO provides high data bandwidth as well as message passing services in a shared memory model. It is transparent to application and operating system software, does not rely on device drivers, and is amenable to software-managed programming techniques.

RapidIO specification layers

The RapidIO specification comprises three partition layers: logical, transport, and physical. This multilevel partitioning scales and accommodates future enhancements while maintaining compatibility with legacy RapidIO technology.

Logical layer

The logical layer specification defines the overall protocol and packet formats. This layer is physically independent and can transmit data over anything from serial to parallel interfaces, from copper to fiber media. The logical layer contains the information necessary for end points to initiate and complete a transaction, such as the destination address and the size of the transaction.

Transport layer

The transport layer specification provides the necessary route information for a packet to move from end point to end point.

Physical layer

The physical layer specification describes the specifics of the device level interface, such as packet transport mechanisms, flow control, electrical characteristics, and low-level error management.

Physical interfaces

The RapidIO specification defines two physical interfaces: parallel and serial.

Parallel interface

The specification refers to the parallel physical interface as the 8 or 16-bit, link-protocol end-point specification. The 8/16 LP-LVDS, Low Voltage Differential Signaling (LVDS), typically has 8 or 16 data bits in each direction along with clock and frame signals in each direction. The parallel interface is suitable for chip-to-chip and some board-to-board communication across standard printed circuit board technology at throughputs around 10 Gbits/sec.

Serial interface

For pin-sensitive implementations, RapidIO defines a serial interface that uses differential current steering drivers based on those defined in the 802.3 XAUI specifications. Engineers developed this signaling technology to drive long distances over backplanes.

RapidIO performance in a fully functional system

Engineers can now make true system performance tests of RapidIO. For example, Mercury Computer Systems' ImpactRT 3100 (Figure 1), a CompactPCI-based multi-computer, implements the RapidIO parallel physical interface over an active backplane. The peak data transfer performance of a parallel RapidIO link as implemented in that system is 622 Mbytes/sec in one direction, or 1.244 Gbytes/sec in two directions. Designers ran a series of tests to determine how actual measured performance compared to this theoretical value.

Designed to address high-end signal and image processing applications, the ImpactRT 3100 system served as a system-level RapidIO test harness. The system consists of 19, 6U RapidIO-enabled slots for quad-processor boards, one RapidIO-enabled slot to serve a RapidIO-PCI bridge board, and one standard CompactPCI slot for the system host board running Windows 2000. Each PowerPC processor in the system has a direct connection to the RapidIO switch fabric, resulting in a theoretical bisection bandwidth of roughly 10 Gbytes/sec. Up to 40 fiber-optic interfaces in the rear of the system support the input data stream for an aggregate peak of up to 10 Gbytes/sec. However, designers did not exercise these fiber-optic I/O modules during the RapidIO performance testing.

Figure 1

"It is transparent to application and operating system software, does not rely on device drivers, and is amenable to software-managed programming ..."

SIDEBAR

RapidIO

New RapidIO flow control extensions for data plane applications enable immediate development of robust, high-utilization communication systems

By Sam Fuller and Greg Shippen

The RapidIO Trade Association recently released a set of extensions to the base RapidIO protocol. These extensions, which have been in development for 18 months, will be able to control congestion that sometimes occurs in high-utilization data plane applications. These extensions complement the link-based flow control mechanisms already included in the RapidIO architecture and support the development of larger and more complex RapidIO-based systems, such as media gateways, radio network controllers, and routers used in mobile networks.

Work on the flow control extensions began in early 2002 at the instigation of major system OEMs that were interested in deploying the RapidIO interconnect as a system-wide combined control and data plane interconnect. They were concerned that, in complex systems, sole reliance on the link-based flow control mechanism might expose the system to issues such as second-order, head-of-line blocking that, in the worst case, could lead to performance collapse.

A task group performed extensive simulation work with queue-based system models of the RapidIO interconnect. Using expected traffic patterns, the group evaluated various proposed flow control solutions. After review of the simulation results and the impact of the proposed changes to existing RapidIO devices and infrastructure, the group settled on a relatively simple directed XON/XOFF mechanism as the preferred solution.

The task group found this mechanism to keep mean packet delay much closer to an ideal system with infinite buffers than link-flow control alone. For example, simulation models showed that as network utilization increased from 70 percent to 90 percent, the mean packet delay increased by only 22 percent over the ideal versus 89 percent when they used link-flow control alone.

Processor board

The quad-processor board itself represents a complex packaging challenge. Each 6U processing board contains four PowerPC G4 Compute Nodes (CNs) and a RapidIO switch. Each G4 CN consists of a 1-GHz PowerPC 7445 with 256 or 512 Mbytes of SDRAM and a CN ASIC, which provides the interface to the RapidIO fabric for each CN. The board also includes three, off-board RapidIO links from the RapidIO switch. Two of these links use the J4 pins of the board's CompactPCI connector, where they can join with a RapidIO interlink module. The third RapidIO link uses the J5 pins, where it can connect with a rear transition module for very high-bandwidth fiber-optic I/O. (See Figures 2 and 3.)

Figure 2

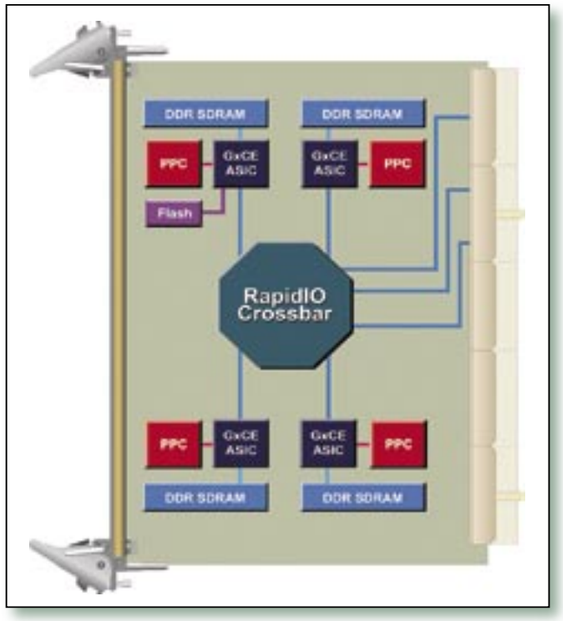

Figure 3

"Each 6U processing board contains four PowerPC G4 Compute Nodes (CNs) and a RapidIO switch."

Designers built the active backplane around an 8-port RapidIO switch. These switches reside both on the physical backplane and on each board in the system. Figure 4 illustrates the RapidIO switch fabric topology on the backplane in the test harness system. Passing data between processors on different boards involves routing it through the switch on the board to a switch onto the active backplane, and then either to a switch on another board or to another backplane switch, which in turn routes the data to a board. Thus, the data packet can parse through up to four switches.

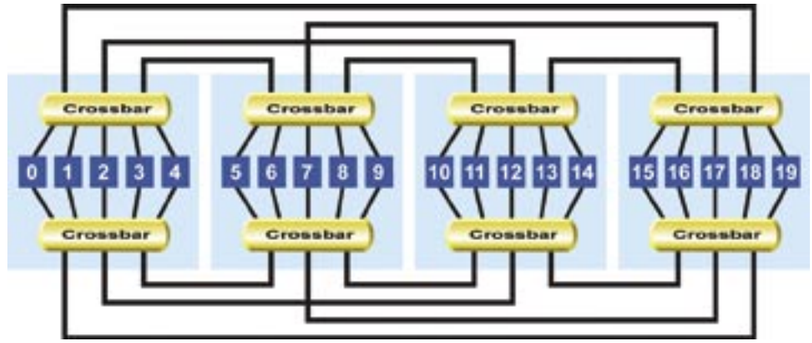

Figure 4

Measured RapidIO system performance

Mercury conducted unidirectional and bidirectional tests exchanging 4000 chained 1-Mbyte data transfers between PowerPC end points. Two conditions were tested: the first was a packetized memory write that did not require a response from the receiving node (NWRITE), while the second condition did require a response (NWRITE_R). Engineers conducted these tests in such a way as to minimize the impact of other activities that can take place within fabric controllers. Thus, the experiment assumed that each command packet fetch consumed approximately 250 nsecs, no snoop activity affected the DCACHE, and the impact of DDR refresh was minimal.

The unidirectional NWRITE test achieved a measured performance of 585.4 Mbytes/sec, or 94 percent of the theoretical raw-data capacity of the RapidIO link. Bearing in mind that the potential overhead consumes 3 percent of the link's bandwidth, this measured performance of 94 percent raw capacity is even more impressive. The bidirectional test achieved 73 percent of theoretical performance. The decreased data rate is due largely to the additional overhead of bidirectional traffic and falls well within the expected range of performance.

The second test employed a memory-write function that waits for a response from the receiving node. This state represents real-world conditions most closely, since applications typically must verify the receipt of data transferred between end points. The RapidIO test harness provided the option of setting the number of outstanding responses allowed before shutting down the memory-writes. This is a coarse method of flow control that permits up to 16 writes to go unacknowledged.

SIDEBAR

The extensions, which introduce a new logical layer transaction type called Congestion Control Packets (CCP), are transparent to existing RapidIO switch devices, and designers can easily implement them within RapidIO end points. The RapidIO architecture design easily supports enhancements such as these flow control extensions.

The RapidIO Trade Association also recently announced the integration of the Advanced Fabric Interface working group into the Trade Association, and formed a RapidIO task group to create the data streaming specification for data plane applications. The primary responsibility of this group is to define standard transaction formats for the transport of typical data plane transaction payloads across interoperable RapidIO fabrics. Example payload types would include ATM cells, Ethernet packets, and SONET frames.

While RapidIO devices already can provide transport of these data types either as messages or as memory-to-memory transfers, the additional specification work provides a standardized approach. The purpose of this approach is to aid in the development of broadly interoperable RapidIO-based semiconductor devices and subsystems.

The diagram to the right in Figure 1 shows how the flow control extensions and the data plane extensions enable the RapidIO interconnect architecture to solve virtually all interconnect needs within embedded computing systems.

While it is true that the operational characteristics of control planes and data planes are different, it is quite feasible to develop an interconnect framework that supports both applications well. RapidIO accomplishes this task by providing a partitioned specification hierarchy of physical, transport, and logical transaction layers.

The RapidIO Physical Layer offers a reliable flow-control managed link technology based on established differential driver technology, which such organizations as IEEE and OIF standardize.

The RapidIO Transport Layer offers a simple and elegant system-mapping model, which supports the single-system connectivity of hundreds to thousands of devices.

Several Logical Transaction Layers are available that provide support for PCI-like I/O transactions, Ethernet-like messages, transactions to support coherency between cache-equipped microprocessors distributed through a system and, now in development, support for encapsulated transport of streaming data types like Ethernet and ATM.

An advantage of the RapidIO architecture is its optimization of low-bit overhead versus robust functionality. Other approaches have much higher transaction overhead

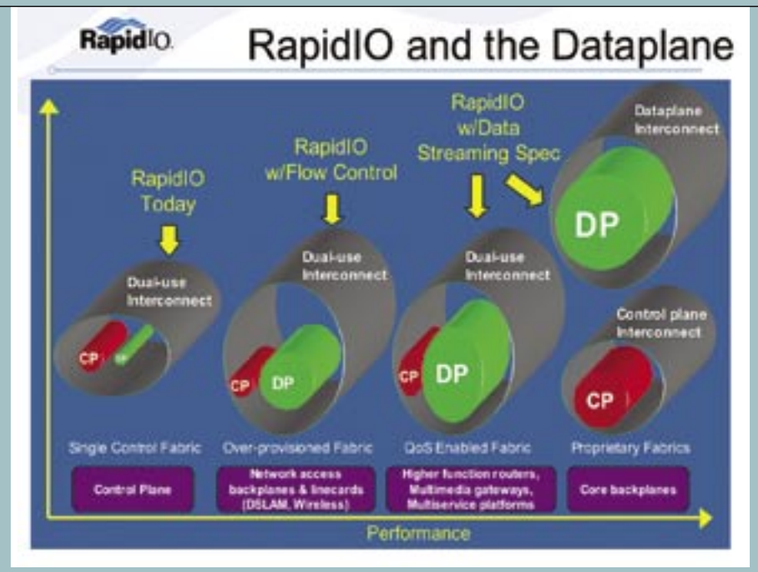

Figure 1

either in bits, on the wire, or in software. These result in lower effective utilization. Another advantage is the ability to encompass control and data path applications under one specification hierarchy. This reduces the overall investment in maintaining multiple types of interconnects within a system domain.

The widespread use of the open standard RapidIO technology within embedded computing systems will greatly simplify the system development task. A common set of wires and protocols throughout the system will allow for the virtualization of I/O and will allow companies to not waste resources developing ASICs or FPGAs to bridge a variety of incompatible buses but rather to focus their resources on their own unique value propositions.

Contact the RapidIO Trade Association directly for more information.

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Table 1 lists the performance obtained under each of four outstanding-response settings. Predictably, the one-outstanding-response case provides the lowest performance, since the sending node must wait for confirmation following each transfer that it sends. Conversely, performance varies little between the 4, 8, and 16-response case, in both the unidirectional and bidirectional tests.

Outstanding Responses	Unidirectional Data Rate	Bidirectional Data Rate
1	146.39 Mbytes/sec (23%)	283.32 Mbytes/sec (23%)
4	558.63 Mbytes/sec (90%)	732.10 Mbytes/sec (59%)
8	576.41 Mbytes/sec (93%)	744.70 Mbytes/sec (60%)
16	576.66 Mbytes/sec (93%)	745.90 Mbytes/sec (60%)

Table 1

The most notable finding from these tests is that unidirectional performance in the 8 and 16-response conditions comes very close to the theoretical maximum performance of the RapidIO link, especially when overhead is considered. Thus, tests have proven that the RapidIO link can deliver the capacity anticipated by the specification.

Unique capabilities with RapidIO

For designers with high-end bandwidth and processing challenges, a RapidIO-based system offers unique capability solutions. The RapidIO interconnect was introduced with the promise of ample data transfer capacity for the most demanding embedded-real-time multiprocessing applications. RapidIO systems can deliver data transfer rates very close to the architecture's theoretical maximum performance, in real-world conditions. ECD

Thomas Roberts *joined Mercury Computer Systems in 1999 and has more than 20 years of experience in systems engineering and technical marketing with IBM, Nixdorf, Data General, Digital Equipment, and Compaq. Tom holds an MBA from the University of Kansas and a B.S. in engineering from Cornell University.*

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Automation revolutionizes embedded systems diagnostics

By Joseph Skazinski

*One of the biggest challenges facing embedded device vendors is building custom hardware and software that meets expected performance, cost, and feature requirements. A major contributor to this challenge is the need to write new software to enable and control custom hardware. According to a 2002 survey by Embedded Market Forecasters (*Minimizing Risk and Maximizing Opportunities in the New Economy, *Krasner and Andrews), many final embedded designs fall short of expectations in key categories, such as performance, functionality, and features. According to the research, 71.5 percent of all designs were not within 30 percent of pre-design performance expectations. Equally alarming, embedded device vendors who build custom software suffer from project completion delays averaging four months. Fortunately, there is new technology available that overcomes many of the obstacles associated with embedded systems development. This article provides an overview about automated embedded systems diagnostics, and how this new technology helps meet the challenge of designing custom software and hardware for embedded devices.*

Obstacles of an effective diagnostics process

While it may seem plausible that running the final software application on custom hardware is sufficient for testing designs, this assumption has flaws. In many instances, the application is incomplete or unstable when the hardware design is completed and ready for verification. This methodology can also be problematic because engineers often build applications with the assumption that the hardware is functioning properly. Applications are typically not well suited for diagnostics, i.e., they cannot easily break down tasks to identify design flaws more readily. A hardware problem may trigger an application failure but give no indication of the actual problem. Therefore, the system might simply crash.

In response to this challenge, companies have attempted to build proprietary diagnostics software that minimizes the efforts of supporting new hardware. This task requires one or more senior software engineers who also know hardware. Unfortunately, these individuals are not easy to hire or easy to spare from other development efforts.

To verify hardware designs successfully, software must be able to exercise all components. Additionally, the software must verify that each component operates in conjunction with the other components connected via the internal bus architecture. Developers must test all Integrated Circuits (ICs) FPGAs, and ASICs for adherence to the hardware bus specification, such as PCI, VME, or others. Another crucial test point involves the determination of performance characteristics. For the purposes of hardware validation during functional or manufacturing tests, it is essential to have test suites that validate the entire board automatically, uniquely identifying and logging individual errors.

Automated diagnostic software takes the driver's seat

New, off-the-shelf diagnostic software designs slash the cost of building custom embedded systems. This technology provides a ready-to-run diagnostics platform for embedded systems, automating the time-intensive steps required to support custom hardware. To efficiently verify new hardware designs, software must provide comprehensive verification and fault isolation capabilities. The solution is an automated test suite that fully exercises all board components while providing individual test execution for fault isolation. Complete test coverage is also essential, for example, exercising a board as it might function in demanding and disparate customer environments. Customizing tests in the form of scripts built from an extensive library of test primitives, and incorporating advanced test services, such as data streaming and data validation, might accomplish this exercise.

Building the bridge to custom configurations

A major impediment to commercialization of embedded software, including diagnostics, is the sheer variety of board designs. A design's processor, memory, bus architecture, and I/O peripherals can all vary. Finding a way to support the myriad permutations of hardware components is essential to developing embedded systems software efficiently.

The process of automatically creating custom software to support custom hardware begins by creating libraries that support the processor, bus architecture, and other components. Designers build these libraries while adhering to an overall layered architecture, exposing individual interfaces for use by the higher-level libraries and services. Designers also expose the interfaces to these libraries to the diagnostics user who can execute functions at the interpreter or retrieve them from internally written code. This configuration allows for the extension of the overall system capabilities to support proprietary ASICs, FPGAs, or other ICs.

Steps for creating custom diagnostics

The first step in creating diagnostics for a custom hardware design is acquiring the hardware configuration data for the particular platform. This step requires processor and component types of data, as well as hardware layout data, such as the memory map. Many times, a hardware specification document already has this information. Figure 1 illustrates the process required to create the final diagnostics application.

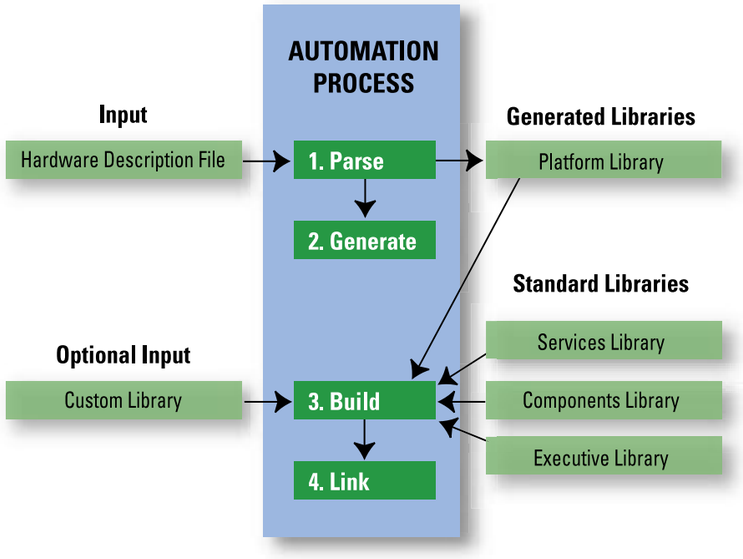

Figure 1

The next step is to use the configuration data as input into a process that pulls from three primary libraries: executive, components, and services. The executive library provides the operating system and command interpreter. The components library contains software to initialize and control all chips and buses on the hardware platform. The services library provides higher-level test applications that mimic the final application in behavior, but take into account a large number of variations. Designers then create a customized intermediate library for the target platform that supports the basic input/output functionality required by the executive and higher-level software components. With these items in place, designers can then build a final executable image that they can download to the target and program into the appropriate memory source, such as Flash memory.

> "Finding a way to support the myriad permutations of hardware components is essential ..."

When the target system resets, or cycles the power, the diagnostics interpreter executes using a serial port for communications to the end user via a terminal emulation program. From this interface, the end user has the ability to interactively execute test cases, either one at a time, or in one or more groups of test cases. The designer can interactively verify the new design or run an endless looping service for compliance testing, including measuring emissions, temperature, power ranges, and more.

With this process, a user need only deliver a hardware specification, or at a minimum, the hardware configuration data, to work with off-the-shelf diagnostic software. If one needs to extend the capabilities of the diagnostics platform, one can write custom routines and automatically include them in the platform for execution at the interpreter. One can archive scripts written for a platform and use them in the future on similar platforms that take advantage of the latest technology. For companies collaborating in the same fashion, they can extract custom scripts from the target, e-mail them to the collaborating site, download them to the target, and execute them. This time-saving feature allows execution of the same test on various platforms for problem isolation. Because of the relatively simple interface, support staff or even customers can use these scripts to report problems in the field.

The off-the-shelf software solution

Designing complete embedded systems from scratch is becoming a luxury that most companies cannot afford. While there are Commercial-Off-the-Shelf (COTS) hardware components on the market, until now, there have been no COTS software solutions with sufficient capability to thoroughly validate custom hardware designs. With the advent of new and innovative technology, support is now available for comprehensive diagnostics that suit custom hardware needs. It comes down to this: Using COTS software diagnostics enables a design team to save significant time and cost in the development of custom hardware designs, therefore delivering the quickest return on investment for the company's embedded device future. ECD

***Joseph Skazinski** is president and co-founder of Kozio, Inc. Joseph and his team launched Kozio in 2002 to deliver embedded diagnostics software using an innovative process. He holds a B.S. in computer science from Michigan Technology University and has more than 14 years of experience in the storage and aerospace industries, focusing heavily on embedded software.*

***Kozio, Inc.** is a technology pioneer in automating embedded systems diagnostics for custom hardware designs. kDiagnostics, its flagship software product, provides advanced diagnostics services for end-to-end hardware validation, including external devices. By building test libraries for all major processors and buses, Kozio provides embedded system vendors, contract manufacturers, and embedded consulting firms with a solution that greatly reduces the cost of verifying new designs and validating manufactured devices.*

Contact the company directly for further information.

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Hybrid digital signal controller enables next-generation automotive control systems

By Ross Bannatyne

In this article, Ross will discuss a new category of electronic hybrid controller that combines the most useful attributes of Microcontroller Units (MCUs) and Digital Signal Processors (DSPs). This new category of product is particularly well suited for use in electro-mechanical systems that require high-end computational functionality as well as the ability to control actuators, such as motors, in real time. Ross will also discuss automotive braking and steering systems, as they are good examples of applications that implement this new technology.

Evolution of the hybrid controller

The diagram in Figure 1 depicts the evolution of the hybrid controller. Designers sometimes call the hybrid controller a Digital Signal Controller (DSC). The DSC is a hybrid of DSPs and MCUs and coexists alongside these devices. The diagram also illustrates the Microprocessor Unit (MPU) – a highly integrated processor that does not contain on-chip integrated peripherals, such as memory arrays.

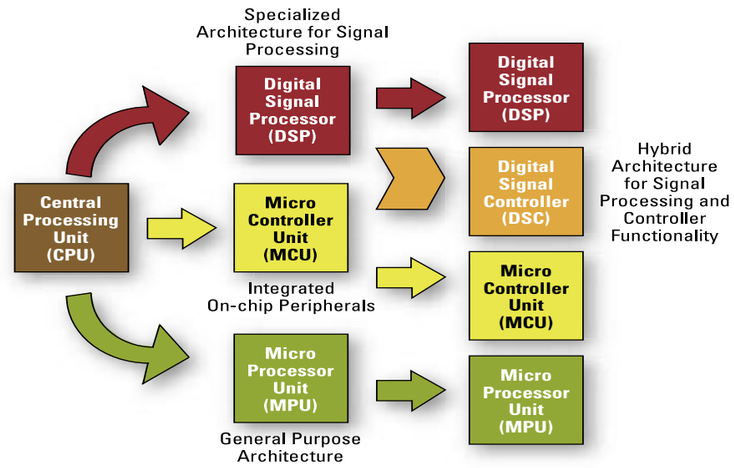

Figure 1

The optimization of MCUs enables them to perform an array of logical, diagnostic, and arithmetical operations on almost any combination of input data from various sources, while DSPs are very efficient at repetitive, numerically intensive tasks. The specific features that define a DSP or an MCU product make it clear that the same hardware is evolving on both types of devices. The DSC is simply a logical progression in the evolution of these product categories. The DSC has evolved due to the requirement for a device that is cost effective in applications that need both an MCU and a DSP. The DSC will replace both chips. Motor control is an example of such an application that can benefit from a DSC. For this reason, many of the peripheral features that designers integrate onto DSCs, such as Pulse Width Modulation (PWM) timers and A/D converters, are also necessary for the effective control of motors.

The advantages of integrating controller and processor functions into a single DSC chip are the usual ones that have been driving such integration in recent years:

- Reduced overall component cost
- Reduced board space
- Reduced logistical controls
- Increased reliability

The benefit of merging all of these features into a single architecture rather than taking a coprocessor approach, i.e., an MCU with a DSP coprocessor onboard, is that this architecture requires only one software program. This approach greatly simplifies the development task and reduces additional overhead, such as the requirement for MCU and DSP development tools, learning curves, etc. The single algorithm includes orientation for both the control portion and the signal-processing portion.

New architecture, new applications

The Motorola 56F8300 family is a good example of the new generation of DSCs. The engineering community has adopted it for use in real-time, electro-mechanical systems that require high performance control capability as well as DSP-level signal processing performance. Two typical applications are brake-by-wire systems

and electronic power steering systems. Manufacturers are adopting these advanced systems for state-of-the-art automobiles.

Currently, there is a trend toward implementing direct-assist electric motor steering systems from the more conventional electro-hydraulic power steering systems. As chassis control for steering systems becomes more complex, it might require more fast math capability in addition to micro-controller functionality. The algorithmic controller must now provide capabilities such as control-oriented instructions, higher code density, and easy programming capability, which use high-level languages. Some designers have considered DSPs to provide these capabilities but are finding that the highly integrated devices that provide both digital signal processing capabilities as well as microcontroller capabilities might be a better fit.

Motorola specifically developed the 56F8300 to address the needs of such systems as well as a variety of automotive motor control applications. Engineers implemented a Harvard style architecture, which uses both a load/store bus for data and an instruction bus for instructions, and which provides three 16-bit data address buses and three 16-bit address buses. Most microcontrollers use a Von Neumann style architecture, which implements a single bus for both data and instructions. The Harvard architecture is more powerful, as it supports parallelism in fetching data and instructions. Figure 2 shows a die photograph of the 56F8300 controller.

Figure 2

There is a high expectation that, in the near future, electrical systems will replace today's standard braking systems, which use hydraulic fluid. Although there are still some challenges to overcome to realize this vision, the expected advantages of such a system over a conventional hydraulic system are such that the motivation to develop *brake-by-wire* is strong. Some of the identifiable advantages are:

- No brake fluid (ecologically friendly and reduced maintenance)
- Lighter weight
- Fuel economy (pad clearance control)
- Increased performance (brakes respond more quickly)
- Minimized brake wear (more control of friction material application)
- More simplistic/faster assembly and testing (modular structure)
- More robust electrical interfacing
- No mechanical linkages through bulkhead (enhanced safety)
- Electronic architecture is more easily upgradeable
- Consistent characteristics of pedal, constant travel
- Significantly fewer parts than a hydraulic-based system

Each wheel would likely have a motor controlled actuator with an associated control circuit. Because of the requirement for accurate motor controls, communications between different nodes, and complex failsafe algorithms, developers consider the 56F8300 as an important part of the system. Some of the specific features of the 56F8300 that are useful in the brake-by-wire application are the timed I/O features, such as the quadrature decoder for motor shaft position tracking, PWM with programmable dead time, and different edge alignment modes. The PWM timer module generates the waveforms that control the motor speed and direction in the by-wire system. The module includes a feature for PWM waveform dead-time distortion correction. When the PWM outputs are driving a motor control half-bridge circuit, the top and bottom output pairs must never be active at the same time, as this occurrence will result in short-circuiting V_{dd} with ground. Dead time ensures a delay between the activation of one of the PWM outputs in a pair and activation of the other output in the pair.

Another optimized peripheral module that the DSC can use is the A/D converter. In motor control applications, designers commonly use a vector control algorithm. This algorithm requires two simultaneous conversions on A/D converter input channels. The specific design of the A/D converters on the 56800 family allows for accurate vector measurement by incorporating high resolution, fast sampling, and simultaneous sampling.

Future expectations

The emergence of a DSC category of devices was inevitable, given the growth in popularity of DSP techniques in applications such as automotive by-wire systems. The main benefit that this hybrid solution offers is the ability to function as both a signal processing engine and a controller unit. This functionality would have previously required both an MCU and a DSP – a luxury for which few designers can budget. In addition to the reduced chipset cost, having only one programmable device for which to write software and to debug is another significant benefit.

The industry expects that availability of such products will further popularize the use of signal processing algorithms in embedded control applications and will drive down the cost of products that had previously required expensive components and lengthy development efforts. Further advanced automotive systems that are likely to implement such technology in the near future are collision avoidance systems, drowsiness detection systems, and integrated chassis control systems that electronically integrate steering, braking, and suspension systems. ECD

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Ross graduated with honors in Electrical and Electronic Engineering from the University of Edinburgh. He also attended the University of Texas at Austin where he graduated from the Option II Executive MBA program. Ross has authored more than 100 publications including the books, Using Microprocessors and Microcomputers, *Prentice Hall, 1999, and* Electronic Control Systems, *Society of Automotive Engineers, 2003. Ross holds one patent for a signature analyzer circuit for failsafe automotive systems.*

Motorola's Semiconductor Products Sector *creates DigitalDNA system-on-chip solutions for a connected world. The company's strong focus on wireless communications and networking enables customers to develop smarter, simpler, safer, and synchronized products for the individual, work team, home, and automobile. For more information, contact Motorola directly.*

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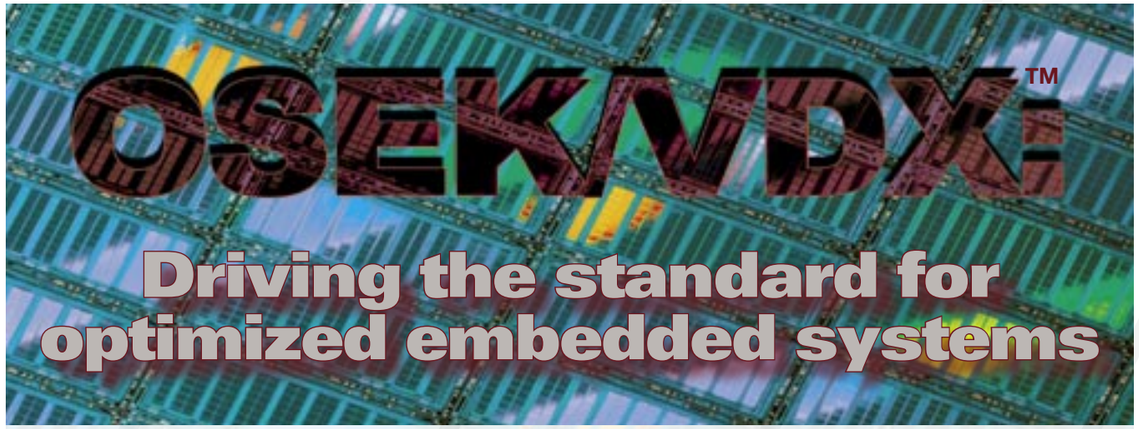

By Michael O'Donnell

The embedded engineering community has recognized OSEK/VDX as an optimal standard for creating embedded applications. Its primary use has been in the automotive industry, but designers have applied it to other industries ranging from storage applications to household appliances. In this article, Michael discusses the history of OSEK/VDX as well as the capabilities enabled by the operating system specification. He will describe technologies that best adhere to the standard, and will instruct the reader in what to look for when selecting a vendor of OSEK/VDX technology, as well as suggest resources for further education.

What is OSEK/VDX and where did it come from?

A consortium of mostly European automotive companies created the OSEK standard in 1993. The consortium's goal was to address the high recurring costs in developing and redeveloping Electronic Control Unit (ECU) software and to improve the compatibility of those applications. In 1994, OSEK merged with VDX, a similar initiative in the French automotive industry. The two standards bodies presented their harmonized OSEK/VDX standard in October 1995. Since then, OSEK/VDX has gained broader recognition in the industry, and a steering committee that includes Adam Opel, BMW, DaimlerChrysler, PSA, Renault, Robert Bosch, Siemens, and Volkswagen currently manages it.

It is important to note that OSEK/VDX is a standard, not a technology. For purposes of simplicity, OSEK/VDX will sometimes appear as OSEK throughout this article. OSEK/VDX includes the following specifications:

- OSEK Operating System (OS) defines a standard interface for a single-processor operating system and offers the necessary functionality to support event-driven control systems. The OSEK OS is the primary focus of this article.
- OSEK Communication (COM) defines a protocol for inter-task and inter-module communications among deeply embedded systems.
- OSEK Network Manager (NM) defines protocols for managing networks during runtime. The NM provides standardized features, which ensure the functionality of inter-networking by standardized interfaces.
- OSEK Run-Time Interface (ORTI) enhances interoperability and portability by defining a common interface for any microcontroller platform and any OSEK vendor. ORTI allows different development tool vendors to debug various OSEK implementations. In addition, an ASCII interface for the ORTI file makes extensions easy and manageable.
- OSEK Implementation Language (OIL) is the configuration language that allows embedded designers to describe the complete OSEK system for system configuration and generation. OIL creates readable, archivable ASCII text files and is the key to enabling interoperability between different OSEK OS vendors.
- Time Triggered OS (OSEKtime) is an emerging standard that extends the OSEK OS specification to allow systems designers to sequence applications and communications (via FTCom) on local and remote controllers as if they were running on the same controller.
- Fault Tolerant Communication (FTCom) usually represents part of an OSEKtime implementation and defines a standard interface for fault tolerant communication.

All these specifications tend to move forward independently of one another. The consortium and participants in the working groups

are often common among the technical committees. However, the timing of the releases of each different specification does not necessarily synchronize with the other specifications. To sustain a high-level of interoperability between these separate and continually changing parts, the standards body introduced the concept of a *binding level*. These binding levels correlate the various independent releases of the specifications into a group, which uses a common base. In this way, a developer can review the specifications of the different OSEK technologies and select the single specification to match their needs. If multiple technologies are required, they can peruse the various documents and determine the binding level that most closely matches the requirements of their end system.

Furthermore, any vendor who uses the OSEK/VDX trademark must meet OSEK certification requirements set by the standards body. The certification process ensures that different implementations conform to the specification. This is helpful to those purchasing OSEK/VDX technology because it allows the buyer to select from only those vendors whose products are portable and interoperable with other OSEK tools.

Why is OSEK/VDX important to the embedded market?

Portability and reliability are perhaps the biggest advantages the OSEK standard offers. With OSEK, designers write applications to a standard application protocol interface (API) and not to a unique operating system, so it's easier to switch from one processor to another. In addition, a static kernel is the basis of the OSEK operating system, rather than a dynamic one, which means an application contains only the specified capabilities and requirements. This configuration greatly reduces the amount of testing needed to ensure the optimum performance of the application.

"To sustain a high-level of interoperability between these separate and continually changing parts, the standards body introduced the concept of a *binding level.*"

Integration is another key benefit of the OSEK/VDX specification. OSEK enables tools from a variety of industries to interoperate, in part, through the OIL specification. OIL creates a system template of which any tool capable of processing an OIL file can read. For instance, an application development tool can read an OIL file generated by a software-modeling tool. The application development tool then produces an OSEK implementation designed for the targeted microprocessor. In this case, OSEK enables a high-level tool to interact with a low-level capability, which demonstrates how integration between disparate tools increases the value of both technologies. The result is a greater choice of products for customers, cost savings for vendors, and accelerated time to market.

A range of industries can leverage the OSEK/VDX OS. For example, the storage application and home appliance markets often have strict requirements for high performance and low memory footprint systems. The OSEK specification is ideal for developing applications that require operating systems with a footprint below 5 Kbytes. In some OSEK OS implementations, it is possible to fit an OS into less than 700 bytes of code. Due to OSEK's wide application and strong worldwide adoption, it has attracted the interest of technology leaders throughout the embedded systems community. More than 50 of these companies, including Metrowerks, a Motorola company, have joined the OSEK technical committee to ensure OSEK/VDX continues to evolve in a positive way.

However, since the automotive industry created OSEK/VDX for its own market, it has perhaps made the most use of the specification. Today, for example, designers commonly use it for controls such as body application, air-bag deployment, chassis integration, and power-train systems. In fact, many automotive OEMs require an OSEK OS as a mandatory component for controller software that they receive from a supplier. In the future, as deeply embedded applications become ubiquitous, the specification might evolve to take advantage of Memory Management Units (MMUs). As higher end microcontrollers decrease in price and become more widely used, the OSEK standards committee or a group of vendors should consider how to apply the specification to the memory management market.

As a widely supported standard, OSEK has significantly reduced the time and costs associated with integrating ECU applications from different Tier 1 suppliers. Now manufacturers can choose from several vendors writing software to the same standard. The results have been higher quality vehicle controls, reduced costs due to integrated and reusable software, and increased innovation throughout the industry. In addition, as environmental regulations increase the cost and complexity of power-train systems, OSEK/VDX technology helps extend the life of existing systems and reduces the risk of migrating to new technology. Above all, improved vehicle reliability and reduced development costs – two critical needs for auto manufacturers – have been the biggest business and technical advantages for the industry.

What's under the hood?

The OS is the first component of the OSEK/VDX standard and defines an operating system API and a set of services. The OS is statically defined, which is especially important to industries where safety and reliability are critical. A static implementation means that a designer can include only the features and capabilities they want in order to contain the implementation. This reduces complexity and unknown factors and increases the ability to adequately test the system. By contrast, a dynamic specification is more open and flexible, and therefore subject to more risks.

Overall, the OSEK OS kernel specification enables high-performance, portable, and scalable applications that use minimal resources and can adhere to stringent real-time requirements. Figure 1 illustrates the relationships between the objects that make up the operating system.

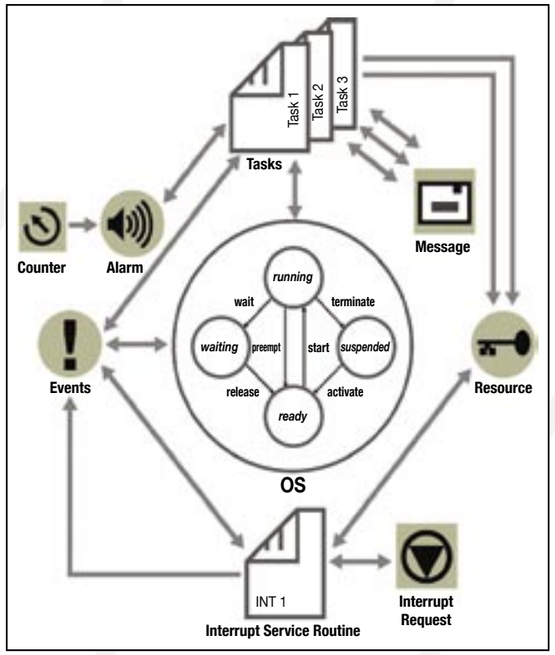

Figure 1

Tasks

There are two categories that describe tasks: basic and extended. The main differences between the two types of tasks are the number of states they support in their state machines and their ability to support event services. In the OS specification, there are four defined states in the state machine:

- Suspended
- Ready
- Running
- Waiting

Basic tasks do not support a transition to the waiting state. In addition, they do not support event services for transitioning to this state. The developer, therefore, chooses between basic and extended tasks depending on the necessity of the waiting state.

The four "conformance classes" defined by the specification allow scaling of the OS to the application demands while still enabling code reuse. These conformance classes are basic, BCC1 and BCC2, and *extended*, ECC1 and ECC2. The primary difference between classes 1 and 2 is the number of tasks they can activate at one time. BCC1 allows only basic tasks and is limited to one activation request per task and one task per priority. BCC2 allows multiple requests for task activation and more than one task per priority. The same is true for ECC1 and ECC2, but they include extended tasks, as described above. Although basic tasks may sound less sophisticated, many embedded application developers find that they can produce complex applications with tighter code using only the BCC1 conformance class.

Each conformance class includes either a standard status or extended status attribute for error checking. In standard status, the OS performs only a few system tests. Whereas, in extended status, the OS has more comprehensive reporting requirements. Therefore, it is better able to reveal development errors. Due to the overhead in the operating system and increased memory usage when using extended status, the OSEK/VDX standards group recommends using it only in the design and debug phase of development rather than in the final product because it puts less demand on RAM and processor resources. It also results in a more finely tuned system. By finding and correcting application errors early in the development process and then transitioning to standard status checking, developers can reduce the total product development costs and limit the memory and performance overhead in the final product.

Tasks can also be *preemptive* or *non-preemptive*. The OS allows an application to comprise a number of independently scheduled tasks, and it can schedule them through fixed priority preemptive scheduling. This means the OS will interrupt one task in favor of a higher priority task. The OS will resume the original tasks once the processor has completed all the high-priority tasks. The *non-preemptive* option allows a task to run its course without interruption from other tasks. This option helps protect access to shared data. The system can also be a combination of preemptive and non-preemptive tasks, which permits a mixed-mode scheduler. The developer can assign this combination anywhere in the system.

"Although basic tasks may sound less sophisticated, many embedded application developers find that they can produce complex applications with tighter code using only the BCC1 conformance class."

Interrupts

The OS defines two categories of interrupt service routines (ISRs). There is one main difference between them: category 1 interrupts do not include OS system calls, and category 2 does include them. The hardware schedules the interrupts and it can interrupt both preemptable and non-preemptable tasks. If an interrupt routine activates a task, then the OS schedules the task after the end of all active interrupt routines. The latest release of the OSEK OS specification has simplified ISR processing, but there are challenges regarding rescheduling of tasks after termination of a nested set of ISRs. Designers should investigate these issues early in the requirement process to ensure they meet product-timing requirements.

Events

Events are *owned* by and linked to extended tasks. Events are used to synchronize different tasks and for signaling between tasks. Any task, including basic tasks, can set an event. However, only the owner task can either clear the event or wait for the event.

Resource management

Resource management controls access to shared resources such as memory and hardware. Within this specification, OSEK enables a priority ceiling protocol to prevent two tasks or ISRs from occupying the same resource at the same time. The priority ceiling protocol also addresses the problems of *priority inversion* and *deadlock*. *Priority inversion* occurs when a lower-priority task delays the execution of a higher-priority task. When the system is *deadlocked,* it means the task cannot execute because it is waiting interminably for mutually locked resources.

The priority ceiling protocol statically assigns priority ceilings to each resource in the early stages of development. To prevent other tasks from running while another has locked a resource, this protocol temporarily increases the priority of the task that has locked the resource. However, any task with a priority higher than the highest priority task with access to the resource can still run.

> "If an interrupt routine activates a task, then the OS schedules the task after the end of all active interrupt routines."

Alarms and counters

The OSEK OS also defines alarms and counters, which synchronize task activation with recurring events. This feature supports portability and code reuse by allowing separation between the timing and functional behavior of a task.

The OS can define alarms as either single alarms or cyclic alarms. It also provides services to cancel alarms and to get the current state of an alarm. The OS statically assigns an alarm to one counter, one task, and one action. The action could be to either activate a task or set an event. Counters are measured in ticks and can represent time or number of pulses received, for example. Each implementation provides at least one timer counter and can schedule periodic events as well. An API specific manipulates other counters to each implementation of the OSEK OS. The standards group included the counter API in the 1.0 version of the specification, but they removed it from the 2.2.1 version by request, due to the complexity of timer interfaces among various microcontrollers.

Error handling and hook routines

OSEK/VDX provides minimal runtime error handling because in a static system, runtime errors are rare. OSEK provides enough error handling via extended return functionality to debug applications in the initial development stages. Then, it can turn off error handling to eliminate the extra code after release of the product.

Hook routines are part of the operating system and the OS can use them as diagnostics during system startup or system shutdown, as in the case of a severe error. The OS uses the hooks to build testing algorithms for application-dependent debugging purposes and, therefore, they have a higher priority than all tasks. The OS will call one hook routine on an error occurrence. However, the specification does not allow hook routines to call most operating system services. This restriction is necessary to reduce system complexity.

What should a designer look for in OSEK/VDX technology?

How does a designer choose the right tools? When the time comes to select an OSEK/VDX vendor, the vendor's product should be OSEK-certified. This requirement ensures that the product has met the rigorous requirements of the OSEK standards body. In addition, the designer will be able to fully leverage the key advantages of OSEK/VDX: high performance, small memory footprint, and reliability.

Next, look for a vendor that works across several platforms, e.g., 8, 16, and 32-bit microcontrollers. The vendor not only should support integration between industry-leading tools and technologies, but also should have a Capability Maturity Model (CMM) rating of Level 3 or above. This rating indicates that the vendor employs a manageable and repeatable software development process resulting in end products with few defects. This is important for those working in an industry where safety and reliability are critical.

Also, look for a flexible business model to meet the needs for low, medium, and high-volume applications. When comparing vendors, it's important to have elasticity in this space if your embedded applications require a small footprint and high reliability. Finally, the vendor's technology should support the ORTI specification and integrate with the compiler for easier system debugging.

Metrowerks, for example, offers a robust, OSEK-certified OS that they developed in accordance with the Software Engineering Institute's (SEI) highest CMM rating. In addition, Metrowerks offers deterministic scheduling for its OSEK/VDX implementation. Deterministic scheduling employs repeatable, mathematical techniques to evaluate and determine the worst-case system load, which dramatically improves the end product. Designers use these proven mathematical tools in a user-friendly graphical format to accelerate design and test time using *worst-case* and *what-if* analysis. When a developer designs and tests systems using deterministic scheduling, they can tune the processor and memory configurations to provide maximum capabilities with minimized costs. Figure 2 provides a checklist of features to look for in development tools.

Buyer's Guide Checklist:
What to look for in OSEK/VDX development tools:

- OSEK-certified
- Capability Maturity Model® (CMM)-rated software process (level 3 or above)
- Flexible business model for low, medium, and high-volume applications
- High-performance
- Integrated with compiler
- Support for a broad range of microcontrollers
- Small memory footprint
- Integration with industry-leading tools

Figure 2

Where to go from here

To learn more about the OSEK specification and how to fully leverage its capabilities, refer to the following resources:

- **www.osek-vdx.org**
  This is the primary Web site for the OSEK/VDX specification and provides details on all the specifications.

- **www.CodeWarriorU.com**
  To learn how to develop embedded applications, CodeWarriorU provides Web-based training on OSEK/VDX application development.

- ***Programming in the OSEK/VDX Environment,* by Joseph Lemieux, 2001.**
  This book explains how to develop OSEK/VDX applications and addresses the three main components of the standard: the OS, COM, and NM. Readers can learn about the standard in its entirety or refer only to those sections that cover the specifications they're implementing. A fourth section details input/output programming, of which the specification does not explicitly cover. ECD

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Metrowerks Corporation *creates CodeWarrior software and hardware products and services for developers with a particular focus on automotive, consumer electronics, wireless, networking, and communications industries. As a leading OSEK/VDX technology provider, Metrowerks supports 8, 16, and 32-bit microcontrollers and offers an OSEK-certified operating system that's been developed in accordance with the Software Engineering Institute's highest CMM rating, level 5.*

Founded in 1985, Metrowerks is an independently operating subsidiary of Motorola, Inc. For more information, contact Michael or the company directly.

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By Markus Levy

Processor performance drives in-car entertainment

Once upon a time, a car was just a car – a form of transportation – plain and simple. Then came the age of electronics, and the semiconductor content of an automobile began to grow for applications from antilock brakes to dashboard controls. Now the use of electronics in automobiles is becoming more pervasive with the advent of in-car entertainment devices such as rear-seat DVD players.

The automotive *infotainment* space combines a wide range of technologies, such as speech recognition, navigational mapping, wireless connectivity, and DVD playback. Regardless of specific features, however, infotainment systems need to incorporate enough processing performance to meet consumer expectations and automotive industry requirements. To meet price points where infotainment becomes *standard equipment*, system designers will further need to specify a microprocessor that can single-handedly and simultaneously execute many of these applications.

> "... infotainment systems need to incorporate enough processing performance to meet consumer expectations and automotive industry requirements."

The specific features and horsepower needed by that central command processor will depend on the type and number of jobs at hand. Keeping in mind that cars have a longer life cycle than consumer electronic products, infotainment system designers will need to provide adequate headroom in their products so that the consumer can add in new functionality with simple software upgrades.

Processor vendors are already competing for the big business that could come out of automotive infotainment systems. Some infotainment applications that will be especially demanding on processors' capabilities are media streaming for MP3 and MPEG. Speech recognition will also become a key feature.

EEMBC has recently announced digital entertainment benchmarks that will help to evaluate processors for a variety of applications, including automotive infotainment. These new benchmarks include:

- MP3 decode
- MPEG-4 video encode and decode
- MPEG-2 video encode and decode
- Cryptography algorithms that represent tasks involved with eCommerce transactions, such as those that consumers will make from their cars

While these benchmarks will be able to test a processor core's computational ability, they will also have a significant

impact on the processor's caches and system memory, and thereby will provide a detailed analysis of processor strengths and weaknesses.

These benchmarks will help evaluate three directions taken by processor vendors in the embedded industry, particularly in the area of infotainment. The first direction is the use of application-specific hardware, like an MPEG-4 accelerator, that will perform a single task within the system. The drawback here is lack of flexibility. The second direction is the use of faster processor cores. Cores designed to run above 500 MHz would be able to perform well on these benchmarks using the brute force method. Run any processor at a high enough clock speed and it will be able to get the job done. The third direction is to use a combination of high-performance processor and application-specific hardware.

None of these directions is a novel concept. System designers have been using function-specific coprocessors for decades. However, the ideal application-specific hardware for an infotainment system is one that is optimized to do the job but also has enough flexibility to change over time.

Contact EEMBC directly for more information about membership and certification.

OSDL UPDATE

Carrier Grade Linux V2.0 is out – Why you should care

2.0

By Mika Kukkonen

OSDL's new Carrier Grade Linux (CGL) V2.0 Requirements Definition is now out. The document is much bigger than the first version we published last year. It's now 146 requirements contained in 105 pages. We are addressing a much larger scope with the addition of clustering and security sections.

More than 40 people from 12 companies representing different areas of the CGL ecosystem participated in the creation of the document. We had important contributions from big names in the communications industry, the IT industry, and Linux distributions, including Alcatel, Cisco, Ericsson, HP, IBM, Intel, MontaVista Software, Nokia, and SUSE LINUX. Working together, we've given the market a well-defined blueprint for the use of Linux in communications infrastructure products.

So those are the raw facts. Nevertheless, in this article I want to get my feet off the ground and present some high-flying personal opinions about why the work we have done is important and how it will benefit everybody, including the non-corporate people in the Linux community.

First, let's get the basic truth out: CGL is partly about the money. It is about the money that network equipment providers (NEPs) like Alcatel, Cisco, and others will save by using Linux in their next-generation communications products. That money is important, because those NEPs will cut costs by shifting from a relatively expensive in-house or proprietary operating system and instead invest in the Linux ecosystem to make the open source operating system good enough for their own use. That NEP investment today will save them a lot of money in the future. That may sound like something straight out of a TV ad – "Buy now and save!" – but it's also true.

But CGL is not only about the money, but also about enhancing Linux – improving both the kernel and the software stack used in Linux distributions. While some of the features in CGL V2.0 may seem specific to the communications industry, most of them apply just as much to other uses of Linux. These are features as important in big data center computers as well as my laptop computer. Additionally, CGL, simply by existing, gives companies a good reason to work on those features and see them getting into the mainline kernel and major Linux distributions.

In the communication industry space, or ecosystem as I like to call it, OSDL's CGL working group serves as a catalyst. It is a neutral place where companies that contributed much of the CGL V2.0 Requirements Definition can work on shared problems, and is also open to all companies that want to be a part of the "Linux revolution" in the communications industry.

In the communications industry, we are indeed seeing a revolution as customers and vendors move from the old "we build it all in-house" to a Commercial-Off-the-Shelf (COTS) world where everyone agrees to use common industry-proven building blocks for their infrastructure to save money and time.

Several major Linux distributions have already pledged their support for CGL V2.0, and I believe the third party software vendors are also waking to the idea of building products on top of CGL features. To help that process, we have also defined a new process called CGL registration for the Linux distribution companies.

From the beginning, the most important goal of that process was to make registration as cheap as possible for the Linux distribution companies to implement. So we have defined a simple self-registration process, which just asks that Linux distribution companies show publicly how they have met the most important CGL V2.0 features.

The only way OSDL will be involved in the process is to publicize a Web page that lists links to Linux distributions where they post their own registration results. OSDL is a big believer in the Open Source development process, and we believe that open peer review is the best way for all the major players to show the status of their registration work.

Linux is a community effort. The OSDL CGL working group is, in my opinion, also a community. In addition, I would very much like to believe that the working group is a valuable member of the larger Linux community. Our work is to make Linux go to a space where its use seemed at best silly just a few years ago – I have first hand experience with this. I invite both the members of the communication industry who are not on the CGL working group, as well as the members of the larger Linux community, to take a closer look at our work. We want you to be involved in the work we are doing. We want your contributions, at whatever level of involvement you wish, because Linux is here to stay.

You can download your free copy of the new OSDL CGL 2.0 Requirements Definition at www.osdl.org/docs/carrier_grade_linux_requirements_definition_version_20.pdf.

For more information about OSDL, contact:

Open Source Development Lab, Inc.
15275 SW Koll Parkway • Suite H • Beaverton, OR 97006
Tel.: 503-626-2455 • Fax: 503-626-2436
Web site: www.osdl.org

Windows XP Embedded Advanced

By Sean D. Liming
Published by RTC Books

Highlights from the Table of Contents:

- Welcome to Windows XP embedded
- Development requirements
- XPe tools overview
- Headless systems & remote management
- Enhanced write filter
- Message box interception and error reporting
- Shells
- Smaller images and faster boot-time
- Remote debugging
- Booting from flash and other media
- Tips-n-tricks
- System level definition files
- Device update agent command language

Windows XP embedded, or XPe, is a tool suite that is used mainly as an operating system in a variety of forms. Devices such as kiosks, ATM machines, and palm-held organization devices take advantage of its ease of use and logical interface. The program is based on the Windows XP core, and this book covers a wide range of different topics relating to XPe.

While much of the pages are filled with very technically oriented information, the main idea behind this book is to give the reader the tools, knowledge, and know-how to actually understand how and why the system is working. Liming does this with clear and concise explanations, walkthroughs, tables, diagrams, coding examples, and many other learning aides to convey his ideas.

The beginning chapters cover the basics of XPe. There is a history section with background knowledge on the subject, along with a rundown of the development requirements. This includes hardware, software, network, and installation overviews. At that point, things get off to a fast start. Diving into many different specified topics, there is a plethora of information in this book. Although there are many specific and detailed areas that Liming extensively covers, he also touches on more broad subjects, such as debugging and quickening boot-time, in great detail.

There is also a great deal of troubleshooting information within these pages. Areas such as database management are full of useful information. Some of the best parts of the book are the sections focusing on optimization. There's a very handy Tips-n-Tricks section, along with a chapter entirely dedicated to putting all your newfound knowledge together effectively. Sean Liming has compiled a wealth of knowledge inside the pages of this book. Tipping the scales right at 700 pages, anyone who has a genuine desire to gain knowledge of XPe can find something useful inside.

About the author

Sean D. Liming is the Windows XP Embedded manager at A7 Engineering. He is the author of Windows NT Embedded Step by Step, *and received his B.S.E.E. from California State Polytechnic University, Pomona.*

For information on how to obtain a copy of *Windows XP Embedded Advanced,* ISBN# 0-929392-77-9, contact:

RTC Books
927 Calle Negocio • Suite G • San Clemente, CA 92673
E-mail: books@rtcgroup.com
Web site: www.rtcbooks.com

Embedded developers' demand and requirements for commercial OSs and software development tools

Volume 1: Current practices and emerging requirements in the automotive vertical market

By Venture Development Corporation

Today, manufacturers of automobiles need to look beyond design of the simple radio, or automatic windows and locks. They must face the demands for new safety, comfort, and convenience features, and increasing entertainment demands from consumers. As a result, electronics in cars today consist of a number of subsystems, and the components of these subsystems need to communicate in real time with each other and the driver.

Complex interrelationships now exist between partnerships and strategic alliances and the automotive suppliers. OEMs continue to consolidate their base of suppliers to meet pricing pressures, and suppliers are establishing global partnerships with semiconductor, wireless connectivity, and consumer electronics companies to add value to electronics solutions.

Report highlights

VDC analysts found that the electronics technology in automobiles is driving innovation with increasing numbers of Electronic Control Units (ECUs). Results indicate that software has increasingly become more important and complex in supporting new functionality due to increasing numbers of ECUs.

Analysts also found that automotive OEMs are challenged by the growth in complexity of embedded software applications due to increased functionality and connectivity requirements. The use of Design Automation Tools (DAT) provides OEMs with a new process for analyzing and validating their products through use of executable models.

VDC estimates that the shipment of dynamic systems design tools in 2002 was by far the largest product category of the automotive industry. Analysts predict that this product category will remain the largest through the forecast period as automotive engineers continue to embrace the use of graphical design methods to rapidly visualize the system, exchange information, and accelerate the development process between OEMs and suppliers.

Software integration from multiple suppliers and configuration management for in-vehicle software will increasingly become more important to OEMs, especially as consumer electronic devices find their way into the vehicle and require wireless connectivity and interfaces.

For embedded developers in the automotive industry, selecting the microprocessor is predominantly the first component selected.

Market overview

For purposes of this report, VDC researchers analyzed the following product categories to determine current and future market trends in embedded OS and software tools for the automotive industry.

- Embedded operating systems
- Software development tools
- Design automation tools
- Test automation tools

Following is a list of companies that VDC included in the research for this report:

- Altium/Tasking
- ARM
- Artisan Software
- Enea Embedded Technology
- ETAS
- Express Logic
- dSpace
- Green Hills Software
- IAR Systems Software
- IBM/Rational Software
- I-Logix
- LynuxWorks
- Mentor Graphics/Accelerated Technology
- Metrowerks
- Microsoft
- MontaVista Software
- Motorola
- Programming Research
- QNX
- Telelogic
- TestQuest
- The Mathworks
- Timesys
- Viosoft
- Wind River Systems
- Automotive manufacturers (i.e., GM, Ford, Daimler Chrysler, Toyota, etc.)
- Major automotive suppliers (i.e., Delphi Automotive, Visteon, OnStar, Johnson Controls, TRW Automotive, Yasaki, Harman/Becker Automotive, etc.)

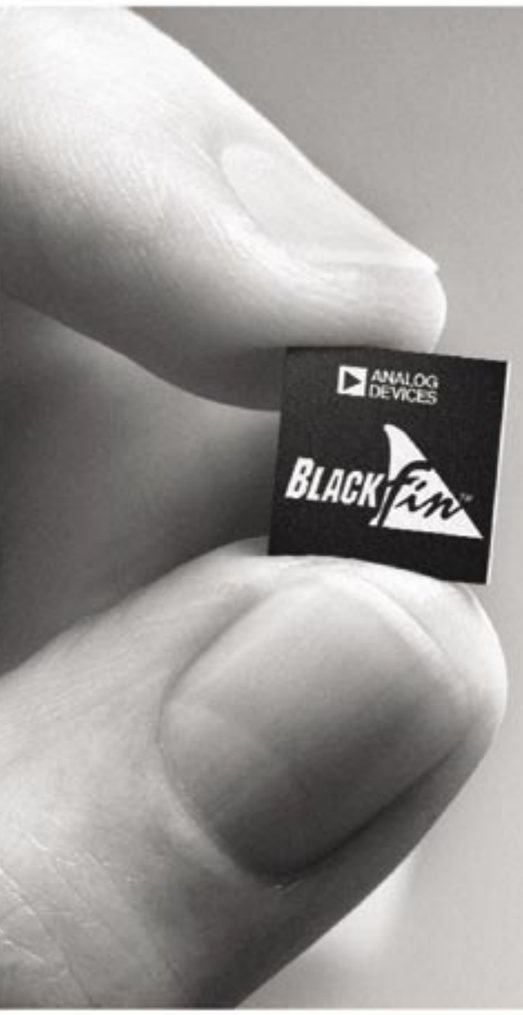
Major report sections

Major sections of this report include the executive summary, industry structure, product descriptions and trends, vertical market estimates and forecasts, end-user trend analysis, requirements, and market development recommendations.

For more information about this market study and to purchase a copy, contact:

Venture Development Corporation
One Apple Hill Drive • Suite 206 • Natick, MA 01760
Tel.: 508-653-9000 • Fax: 508-653-9836
E-mail: info@vdc-corp.com
Web site: www.vdc-corp.com

Performance like never before.



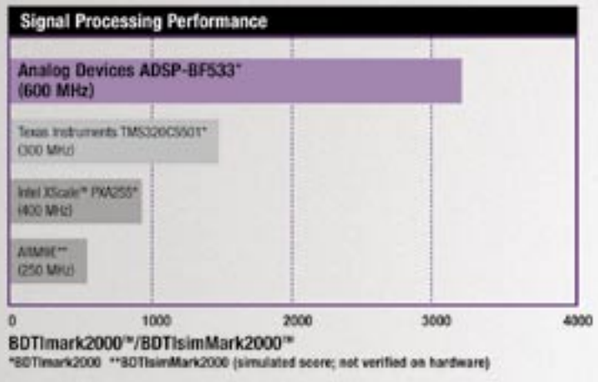
From $4.95 and 50 mW to 600 MHz and 1.2 GMACs. The new Blackfin® Processor is here.

Available today, the next generation of Blackfin Processors deliver breakthrough signal processing performance and power efficiency. The Blackfin Processor combines best-in-class digital signal processing with RISC-like programmability—meeting the computational demands and power constraints of today's demanding embedded media applications.

Blackfin Processor Capabilities

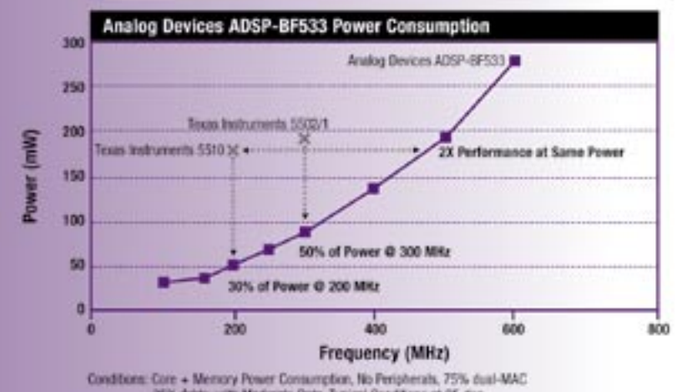
600 MHz/1.2 GMACs
D1/VGA 30 fps MPEG4 decode
CIF 30 fps MPEG2 encode/decode
40 G.729AB voice channels

Signal Processing Performance

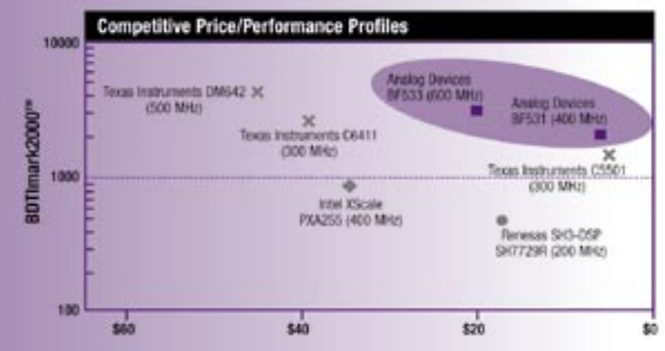


BDTImark2000™/BDTisimMark2000™

*BDTImark2000 **BDTisimMark2000 (simulated score; not verified on hardware)



Conditions: Core + Memory Power Consumption, No Peripherals, 75% dual-MAC 25% Adds, with Moderate Data, Typical Conditions at 25 deg



- Ideal for embedded audio, video and communications applications
- Industry-leading benchmarks: highest frequency dual MAC architecture (600 MHz), highest MMAC/$, lowest mW/MMAC (0.15 mW/MMAC at 300 MHz)
- Dynamic Power Management and on-chip regulation: increases battery life by more than 2X, at the same performance, as the nearest competitor
- On-chip RAM: from 52 to 148 KBytes
- Three Blackfin Processors for any task:
  ADSP-BF531 (300 and 400 MHz)
  ADSP-BF532 (300 and 400 MHz)
  ADSP-BF533 (500 and 600 MHz)
- Small footprint (12mm x 12mm) enables new portable handheld appliances
- Processing power without the high price: 300 MHz Blackfin Processor for just $4.95 @ 10 kU
- Supports all major embedded real-time operating systems

BDTi BENCHMARK PARTNER

The BDTImark2000/BDTisimMark2000 provide a summary measure of DSP speed. For more info and scores see www.BDTI.com. Scores © 2002/2003 BDTI.

Visit **www.analog.com/blackfin533** to:

- Order samples
- Download a free VisualDSP++™ Test Drive
- Get your 600 MHz Blackfin EZ-KIT Lite™ evaluation board and software today

ANALOG DEVICES

RSC #49 @ www.embedded-computing.com/rsc

Embedded industry trends

By Matt Cicciari

Ubiquitous availability of new technologies and advances in connectivity have put new business requirements on *embedded* systems. No longer can these systems be *dedicated-function* or *special-purpose,* operating in isolation from the rest of the computing environment. Technology alone is no longer a competitive advantage.

Costs and flexibility benefits of Commercial Off-the-Shelf (COTS) hardware that include standard technologies, such as 1394/FireWire and USB, have driven developers away from proprietary and non-standard components. Advances in networking – the Internet, standards, wireless, costs – allow organizations to continue to increase productivity and streamline operations by connecting islands of embedded systems with the enterprise. Think about the implications of just a couple of examples like Radio Frequency Identification (RFID) on retailers (such as the hard plastic tage on leather jackets in stores) and manufacturers, and control systems that use wireless mesh networks to ensure high availability and real-time reporting and updates.

The trend toward standards that are technology rich is not limited to hardware platforms. Operating systems and applications are more off-the-shelf with the ability to readily support unique embedded needs; for example, hard-real-time headless operation and footprint optimization. Suppliers of these products can no longer compete on feature and function alone, but need to deliver complete solutions that reduce the OEM's time and cost to market.

These trends and business requirements cut across many major vertical markets including consumer electronics, industrial control and automation, medical, military/aerospace, and process control. Developers and OEMs of embedded systems to these markets face many new challenges as a result. In today's embedded business environment, there are four overriding competitive themes that drive key business decisions:

- Increased Time-to-Market (TTM) pressure
- Shrinking resource allocation
- Reduce hardware and software costs
- Increase Return-on-Investment (ROI)

Increased time-to-market pressure

Every day companies face the challenge to get products to market faster than the competition, and even faster than the previous day. As a result, companies must look for new ways to shorten the product development cycle. There is a growing urgency to get it right the first time and to not waste time with costly *what-if* scenarios.

Shrinking resource allocation

The simple business strategy of the last couple of years has been to *do more with less*. Less time, fewer personnel, fewer resources, and yes, less money, are just some of the shortages that companies face each day.

Reduce hardware and software costs

The latest trend for companies building embedded products has been a shift toward obtaining COTS hardware and software. This, in addition to reusing existing hardware for new projects, is helping to reduce the infrastructure costs for companies striving to compete.

Increase ROI

It almost goes without saying that companies are looking to get more out of their investments. It is no longer acceptable to break even. In order to be successful, companies are asking to get much more out of everything they do. There is no room for waste.

Companies that can find the right combination of answers to these concerns will find themselves atop the list of successful, profitable companies. The following embedded industry product review will potentially be the next step in the process of identifying winning solutions to extend a significant competitive advantage.

***Matt Cicciari** is a senior product marketing manager for Venturcom at the Waltham, MA location. Contact Matt at mcicciari@vci.com for more information.*

***Venturcom** is a provider of software products and services to companies that design embedded systems and enterprise solutions. Venturcom's embedded solutions include RTX™, the real-time extension for Windows, and Phar Lap ETS®, a small footprint real-time operating system and development environment package. Venturcom's enterprise product line, BXP®, allows corporations to reduce Total Cost of Ownership (TCO) through remote boot and centralized image management and deployment of client systems. For more information about Venturcom, its services, and products, visit www.vci.com.*

Nallatech, Inc.

12565 Research Parkway
Orlando, FL 32826

NALLATECH

BenNUEY-PC104+

www.nallatech.com

The BenNUEY-PC104+, based on the PC/104-*Plus* standard, combines unparalleled off-module I/O, flexible FPGA device support, and exceptional bandwidth capabilities for next-generation embedded system designs. By replacing the traditional ISA connectors in the PC/104-*Plus* stack with a new, high-density connector, the BenNUEY-PC104+ provides the high levels of interconnectivity required to interface up to 56 million gates of FPGA capacity using the latest Virtex-II FPGAs from Xilinx. Supplied as standard with two FPGAs, the first is a Virtex-II device, with a choice of 2V3000, 2V6000, or 2V8000 FPGAs. The second FPGA comes pre-configured with firmware for PCI interfacing and board control, supporting a simplified and accelerated design process. In addition, three DIME-II module slots provide flexible expansion capability that enables developers to construct fully customized embedded systems using standard products. The BenNUEY-PC104+ includes a separate power distribution card, which ensures that all the power requirements of the FPGAs in the system are fulfilled. As the PC/104-*Plus* connector can supply only a fraction of the current needed in such high powered systems, Nallatech has provided an additional power connector to each carrier card, which can be connected directly to a power source to become the main current path.

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For more information, visit www.nallatech.com.

FEATURES

- PC/104-*Plus* form factor
- Three DIME slots for logic & I/O expansion
- Up to 7 Virtex-II FPGAs
- PCI FPGA pre-configured with PCI (32-bit/33 MHz) core
- 8 Mbytes of onboard ZBT SRAM
- Up to 66 single-ended IO signals through ultra SCSI connector
- 11 point-to-point buses, two distributed buses, and one 122-bit wide pipeline bus
- Three onboard programmable clock nets
- Fixed oscillator socket or user input connector
- Supports triple DES bitstream encryption
- Software support for Windows, Linux, and VxWorks C/C++ development
- Includes API software

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Targa Systems

2081 Merivale Road, #200
Ottawa, Ontario K2G1G9 • Canada

VME25 Flash Disk

www.targasystems.com

Targa's solid-state 6U VME Flash Disk has been designed specifically to replace hard disk drives in rugged aerospace and military environments. The 6U VME board is available in a single-slot board (up to 30 Gbytes) and in a dual slot configuration, with capacities up to 90 Gbytes. Both convection-cooled and conduction-cooled units are available. The VME25 Flash Disk design meets demanding military standards and is suitable for a wide range of airborne and ground applications. The VME25 is available in Fast and Ultra SCSI, as well as ATA and I/O memory-mapped interfaces. A version is also available in the CompactPCI 3U and 6U form factors.

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For more information, visit www.targasystems.com.

FEATURES

- No moving parts
- Conduction-cooled
- Convection-cooled
- Capacities up to 90 Gbytes
- MTBF 500,000 hours
- Fast access times
- Low power consumption
- Write protect
- High-speed erase
- All solid state

Technobox

PMB 300 • 4201 Church Road
Mt. Laurel, NJ 08054

3923

www.technobox.com

The 3923 is a FlexATX Processor PMC (PrPMC) carrier and development platform. This carrier board provides two PMC sites plus three PCI card slots (two 64-bit and one 32-bit). Using the 3923, a designer can work with a single PrPMC, dual PrPMCs, or a PrPMC and PMC for hardware and/or software development. All PCI slots are keyed for 3.3-volt signaling. The PCI bus will run at 66 MHz, if all PCI cards assert 66 MHz enabled. At least one PMC site must be populated with a PrPMC running in monarch mode. Site A's rear I/O is directed to connectors for a floppy disk and/or external IDE device. The rear I/O for site B is directed to a DIN connector that emulates P2 of a VMEbus board. Each site has a fan to cool the mounted PrPMC or PMC. LEDs provide status for memory, configuration, I/O access, power, PCI interrupt, and bus mastering activity.

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For more information, visit www.technobox.com.

FEATURES

- FlexATX platform for PrPMC development and/or delivery
- Dual PMC sites allow various configurations with PrPMCs and PMCs
- Slots for three PCI cards (two 64-bit, one 32-bit) rear I/O access for external IDE or floppy drive
- Auxiliary cooling for PMC sites

Technobox

PMB 300 • 4201 Church Road
Mt. Laurel, NJ 08054

4044/4068 PCI-X to PMC-X Adapter

www.technobox.com

The 4044 is a passive adapter that permits operation of a standard 32- or 64-bit PCI-X card in a PMC-X slot. One PCI-X edge finger connector supports keying for 32-bit 5V signaling PCI cards. A second edge finger connector supports keying for 32-bit or 64-bit 3.3V signaling PCI-X cards. A universal 5V/3.3V signaling PCI-X card can be used in either position. An 8-layer design assures optimal performance when using the adapter with high-speed PCI-X boards. Six 20-pin box connectors provide an interface for a logic analyzer to access the full 64-bit PCI-X bus. The pin out of these connectors support HP 01650-63203 termination adapters. Color-coded test points are also provided to allow supply voltage measurements.

LEDs monitor power supplies and key signals. Logic provided on the board decodes the PCI-X bus cycles into memory RD/WR, I/O RD/WR, and configuration space RD/WR, with associated LEDs providing indication of status. Pulse-stretchers allow visible detection of short-lived events. Furthermore, a novel analog circuit provides a voltage (0 to 1 VDC) proportional to the bandwidth utilization of the PCI bus. Schottky diodes are used to minimize signal undershoot and other transmission line effects. An optional Roboclock® PLL clock buffer (P/N 4051) can be added to the board to allow skewing of the front edge of the PCI clock +/- 4 ns (in 1 ns steps) to optimize setup and hold times on the PCI-X bus. The setting is controlled using a rotary switch on the board.

A build option (P/N 4068) includes a 10 watt, 5-to-3.3 volt DC-to-DC converter.

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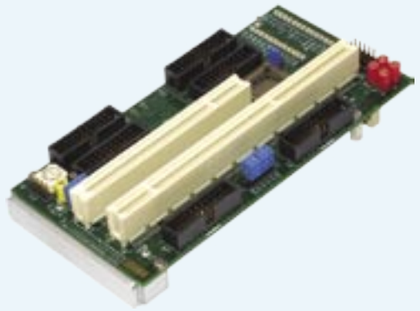
For more information, visit www.technobox.com.



FEATURES

- Adapts 32 or 64-bit PCI cards to a PMC site
- Supports PCI 33/66
- Supports PCI-X 66/100/133
- 8-layer design for optimal performance
- Logic analyzer headers (compatible with HP 1650-63203 termination adapters)
- Access to JTAG chain between host and PCI card
- LEDs convey PCI bus operation(PCI bus command code decoded for individual LEDs)
- Supports bandwidth measurement
- Schottky diodes minimize undershoot and transmission line effects
- LEDs display power, bus signals, and bus cycles
- Optional PLL clock buffer for +/- 4ns skewing of PCI clock
- Optional build with DC-to-DC converter to support 5-volt systems

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Advantech Embedded Computing

15375 Barranca Parkway, Suite A-106
Irvine, CA 92618
Toll Free: 1-800-866-6008

PCM-7220

www.advantech.com/risc

The PCM-7220 series Application Ready Platform (ARP) integrates Intel's PXA255 processor and Windows CE .NET or Embedded Linux solution in a 78mm x 104mm (3" x 4") compact form factor. It is designed to provide customers with a high-performance subsystem board based on Intel's XScale™ technology with character of ready-to-run, compact, and flexible expansion to meet versatile application needs. Certified platform functionality offers fast and flexible Customized To Order Service (CTOS). The PCM-7220 offers customers a fast time-to-market and flexible reference platform that is fully customizable. All functionality has been completely certified and can be leveraged to customize various hardware specifications and system optimization needs based on customers' requests. This solution platform, based on Intel's XScale technology, offers rich I/O interfaces and high performance, along with an Intel PXA255 processor complete with a 32-bit, and up to 400-MHz speed, SoC engine. It also reserves interfaces for flexible configuration that will exceed expectations for high performance vs. cost. Expand your versatile needs through the ARM Module Interface (AMI-120). Through this unique open expansion interface, AMI-120, the full line of AMI solution modules offers similar expansion functionality as the PC/104 to x86 platforms. The AMI modules interface is also open to customized solution modules as well.

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For more information, visit www.advantech.com/risc.

FEATURES

- RISC 2.5" ready-to-run SBC with an Intel PXA255 processor
- Windows CE .NET/Linux Platform integrates with Advantech software solution including Bootloader, device driver, OS kernel, and system utility in a pre-installed package on either onboard Flash or CF card
- Multiple boot options through the onboard Flash, extended memory module, or CF card
- Extended temperature (Advantech Phoenix models) available as optional models
- Full power management for ultra-low-power performance (Normal – <2.5 W/Suspend <200 mW)
- AMI-120 interface for quick function applications
- SM bus interface for battery powered applications
- Evaluation kit integrating 5.7" STN QVGA panel, touchscreen, battery pack, 8DI & 8DO/8 x 8 matrix key pad (hot key) is available for project feasibility evaluation
- Industrial mobile device platform
- Distribution data management
- Touch-base human machine interface
- Medical and security controller or data entry operator interfaces

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EL Technology Inc.

46750 Fremont Blvd., #104
Fremont, Ca 94538

IPC-BAE7

www.ELT-IPC.com

The IPC-BAE7 is a high performance PC/104 CPU module that supports VIA Eden series processors with clock speeds up to 800 MHz. For ultimate performance capability, the IPC-BAE7 packs all the functions of a versatile system, including a VIA VT8606 VGA. Chipset supports CRT and LCD with shared system memory up to 32 Mbytes and Intel 82559ER Ethernet. System memory is provided by one SOMIMM socket that accommodates up to 512 Mbytes SDRAM. Watchdog timer, digital I/O, USB, IDE, FDD, parallel and serial ports, and CompactFlash socket also come with this board. Also, the IPC-BAE7 power operates at only 5V.

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Send your inquiry to sales@elt-ipc.com.

FEATURES

- VIA Eden series CPU
- Supports CRT, 18-bit TFT LCD
- Intel 82559ER Fast Ethernet digital I/O (4 × in, 4 × out)
- CompactFlash

RSC #56 @ www.embedded-computing.com/rsc

VMETRO, Inc.

1880 Dairy Ashford, Suite 400
Houston, TX 77077

Vanguard

www.vmetro.com

The Vanguard is a family of PCI, PMC, and CompactPCI bus analyzers designed for debugging, testing, and validating of next-generation PCI-X and PCI boards and systems. The analyzer is able to capture and display all bus activity in PCI-X/PCI-based systems up to 133 MHz with powerful trigger and store qualifiers, and offers real-time statistics to measure system performance. The analyzer assists the designer from the beginning of the design through the integration phase. For hardware engineers, the analyzer displays bus timing in waveform or list form, giving the hardware designer a view of the bus behavior. For software engineers, the state analyzer provides an easy-to-read overview of the bus transactions. For system integrators, the analyzer provides performance monitors, comparative analysis, and behavior qualification. The exerciser acts as a PCI-X or PCI master target, with 8 Mbytes of memory or interrupter, for emulation of not yet available devices. The protocol checker detects 71 PCI-X or 45 PCI protocol errors to determine if bus devices are violating the specification. The compliance test uses all functions of the Vanguard to qualify ASICS, components, motherboards, expansion cards, and systems compliance with the PCI/PCI-X Local Bus Specification.

.....
For more information, visit www.vmetro.com.

FEATURES

- PCI, PMC, or CompactPCI form factor
- 0-133 MHz PCI-X and 0-67 MHz PCI support
- 2 Msample trace buffer at 256 bits
- Concurrent and independent operation of all functions
- 3.3V or 5V support
- USB or Ethernet communication
- Eight word recognizers and 16-level sequencer for defining trigger events
- Pre-defined and user-defined statistics
- Basic exerciser or enhanced exerciser with PCI-X error injection
- Automatic protocol and compliance checker

RSC #57 @ www.embedded-computing.com/rsc

Aurora Technologies, Inc.

10 Mupac Dr.
Brockton, MA 02301
Tel.: 508-588-6110

AURORA TECHNOLOGIES
A Carlo Gavazzi Group Company

Saturn 8520 PCI Multiport Serial Controller

www.auroratech.com

The Saturn Multiport, an eight-port PCI communications controller, provides the performance and reliability needed for high-speed serial communications. Supports data transfer rates up to 256 Kbits/sec synchronous and 230.4 Kbits/sec asynchronous, full duplex.

The Saturn Multiport supports SPARC Solaris, Rev. 7, 8, and 9; Solaris x86, Rev. 2.6, 7, and 8; and Linux (kernel build 2.4.17 and above).

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Visit www.auroratech.com for more information.

FEATURES

- Eight ports from one PCI bus slot
- Each port is assignable for synchronous or asynchronous communications
- Synchronous data transfer rates up to 256 Kbits/sec and asynchronous data transfer rates up to 230.4 Kbits/sec, full duplex, simultaneously on all ports
- Supports SPARC Solaris, Rev. 7, 8, and 9; Solaris x86, Rev. 2.6, 7, and 8; and Linux (as of kernel build 2.4.17 and above)
- Interface options include:
  -RS-232
  -RS-422/485 with DB-25 connectors via an external breakout box
- Compatible with Sun synchronous communications protocols
- Optional Aurora synchronous communications protocol software for Sun Solaris include X.25 and HDLC LAPB

RSC #58 @ www.embedded-computing.com/rsc

EMBEDDED INDUSTRY PRODUCT REVIEW

COMMUNICATIONS

Aurora Technologies, Inc.
10 Mupac Dr.
Brockton, MA 02301
Tel.: 508-588-6110

AURORA TECHNOLOGIES
A Carlo Gavazzi Group Company

StarFabric Development Kit

www.auroratech.com

This StarFabric Development Kit is designed to aid you in your StarFabric application development and reduce time to market. The kit integrates Aurora's CP-SFX8 Fabric Card with CG Mupac's 2.17 backplane and 585 Series eight-slot, portable, aluminum enclosure.

Aurora's PICMG 2.17 compliant CP-SFX8 6U Fabric Card lets you implement a centralized fabric topology in a CompactPCI chassis. It features efficient, low (less than 3μsecs) latency design and offers aggregate bandwidth of 40 Gbits/sec. The PMC site operates in monarch or non-monarch mode. The card is compatible with MS Windows and Linux.

Highly serviceable and maintainable, the 9U-high 585 Series from CG Mupac features a flush card cage accommodating eight 6U x 160mm CompactPCI boards housed in a vertical orientation. The backplanes support IPMB as specified in PICMG 2.9 rev. 1.0, 5.0, or 3.3-volt keying and Hot Swap. Optional 1101.11 compliant 80mm transition I/O cards are supported. Included are: one 5.25" x 1.63"; one 3.5" x 1.0" accessible peripheral bay; one 3.5" internal bay 320W autosense ATX power supply; dual 50/90CFM fans; accepts Pentium, Celeron, or Pentium II/III CompactPCI SBCs; Hot Swap compliant.

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Visit www.auroratech.com for more information.

FEATURES

- Aids you in your StarFabric application development
- Reduces time to market
- 15.75" (H) (9U) x 9.2/11.6" (W) x 11.7" (D) chassis (400mm x 234/296mm x 297mm)
- Eight-slot, 7U CompactPCI backplane with front & rear I/O
- Features up to eight links to the backplane and two front panel links with chassis
- Supports up to four node cards within the chassis

RSC #59 @ www.embedded-computing.com/rsc

GE Fanuc

12090 South Memorial Parkway
Huntsville, AL 35803

Embedded Systems

Intel Pentium M CompactPCI SBC (VMICPCI-7806)

www.gefanuc.com

GE Fanuc's VMICPCI-7806 single-slot CompactPCI SBC features the latest Intel Pentium M processor, operating at 1.1. or 1.6 GHz. Fully compliant with PICMG 2.16 CompactPCI Packet Switching Backplane (CompactPCI/PSB) specifications, the VMICPCI-7806 offers the robustness, reliability, and hot-swap features required for demanding embedded computing applications.

As a universal CompactPCI SBC, the VMICPCI-7806 is capable of supporting applications as either a system slot controller or a peripheral slot controller. The PCI-to-PCI bridge interface to the CompactPCI bus is automatically configured to operate as either a transparent or non-transparent bridge. This implementation is fully compliant with PICMG 2.0 Rev. 3.0, PICMG 2.1 Rev. 2.0, and PCI-to-PCI Bridge Architecture Rev. 1.1.

The VMICPCI-7806 features a wide range of I/O and storage interfaces through the front panel as well as the backplane J3 connector to ensure maximum flexibility. A 64-bit, 66/33-MHz PMC site and 32-bit, 33-MHz PMC site enable further I/O expansion.

Supports operating systems such as Windows 2000/Windows XP and Linux.

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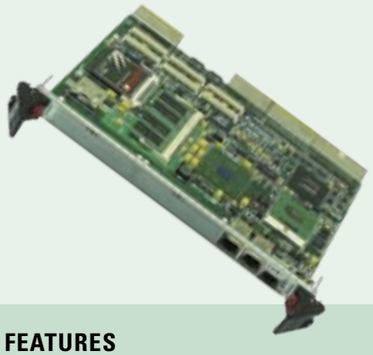
For more information, visit www.gefanuc.com/embedded.



FEATURES

- Intel Pentium M processor at 1.1 GHz and 1.6 GHz
- 1 Mbyte of L2 cache
- Up to 2 Gbytes DDR SDRAM
- Two Ethernet controllers support 10/100/1000Base-TX interfaces
- Two USB 2.0 ports
- Serial ATA support
- Two high-performance, 16550-compatible serial ports
- Fully supports PICMG 2.16
- Two PMC expansion sites
- Universal 64-bit/66-MHz CompactPCI bus interface
- IPMI 1.0 support
- IDE and floppy drive interfaces

RSC #60 @ www.embedded-computing.com/rsc

General Standards Corporation

3208 Whitesburg Drive SW • Huntsville, AL 35802
Tel.: 1-800-653-9970 • Fax: 256-880-8788

General Standards Corporation
High Performance Bus Interface Solutions

PMC-SIO4

www.generalstandards.com

The PMC-SIO4 is an easy-to-use, four-channel, full-duplex RS-422/485 serial board. Each channel can operate at up to 10 Mbits/sec. Optional 32-Kbyte FIFO buffer for both transmit and receive data on each channel (256 Kbytes total) provides for a smooth and efficient interface between the serial interfaces and the PMC host computer. The board is based on the Zilog Z16C30 high-speed integrated Universal Serial Controller (USC), which supports asynchronous, isochronous, bisync, monosync, HDLC, SDLC, external sync, and 9-bit protocols. The USC chip provides full duplex operation with baud rate generators, digital phase-locked loop for clock recovery, and a full duplex DMA interface. The board only requires simple read/write statements to operate. This board is available on all form factors, including PCI, CompactPCI, VME, and PC/104-*Plus*. See our Web site for more details.

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E-mail: sales@generalstandards.com for more information.

FEATURES

- Four full-duplex serial channels
- Either RS-422/485 or RS-232 interface available
- VxWorks™ and WinNT™ drivers available
- Up to 10-Mbits/sec synchronous operation on each channel
- Up to 1-Mbits/sec asynchronous operation on each channel
- Up to 32-Kbyte FIFOs for transmit and receive of each channel (eight FIFOs total)
- Serial channel cabling via front panel of host
- Built-in self-test capability verifies proper operation of the card
- Supports asynchronous, bisync, SDLC, HDLC, and 9-bit protocols
- Parity and CRC error detection
- DMA to/from Zilog Z16C30 (USC) to onboard FIFOs
- DMA to/from onboard FIFOs to PMC host
- Programmable selectable data rates via onboard baud rate generator per channel
- Sync word selection allows an interrupt upon the reception of a user-specified character
- Extensive interrupt signaling capability
- VxWorks™ and WinNT™ drivers available

RSC #61 @ www.embedded-computing.com/rsc

Interphase Corporation

2901 N. Dallas Parkway, Suite 200
Dallas, Texas 75093
Tel.: 214-654-5000 • Fax: 214-654-5500

45NS PMC Network Security Acceleration Module

www.interphase.com

The new 45NS (PMC) network security acceleration module from Interphase is designed to free up host CPU cycles used for embedded security software processing in today's VPN, gateway, secure router, firewall, IAD, and general-enterprise-network access servers. Integrating the Interphase security accelerator card into these applications will increase network efficiency and response times by offloading bandwidth-intensive IPSec and SSL security protocol processing from the host CPU, and the hardware-based architecture of this solution will provide a new level of reliability to network security applications. By providing intelligent packet processing, the 45NS module can perform a variety of functions for addressing the complex security needs of today's enterprise and carrier grade systems, including header analysis, payload extraction, compression, encryption, authentication, and packet assembly.

Based on the specialized Hifn 7854 security processor, the 45NS module accelerates basic security algorithms including DES, 3DES, MD5, SHA-1, RC4, and AES. Other product features include support for full duplex OC-3/STM-1 (155-Mbits/sec) rates, true random number generation, a 64-bit/66-MHz PCI bus with universal signaling, 64 Mbytes of private memory for security session data and parameter storage, and support for up to 512K simultaneous sessions.

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For more information, visit www.interphase.com.

FEATURES

- Intelligent packet processing for IPSec and SSL acceleration, offloading host CPUs of process-intensive network security functions in next-generation applications such as VPNs, firewalls, secure routers, IADs, gateways, and enterprise network access servers
- Specialized Hifn 7854 network security processor enables support for up to 512,000 simultaneous sessions
- Supports all major security and compression protocols, including IPSec, 3DES, AES, and SHA
- Modular design for a variety of environments, including PCI, CompactPCI, VME, and proprietary architectures
- Functions performed to offload host CPUs from bandwidth-intensive security processing: header analysis, payload extraction, compression, encryption, authentication, and packet assembly
- Support for full duplex OC-3/STM-1 (155 Mbits/sec) rates, true random number generation, 64 Mbytes of private memory, public key support with built-in public key processor
- Software development tools for Linux utilizing the FreeSWAN IPSec stack
- Custom development also available

RSC #62 @ www.embedded-computing.com/rsc

EMBEDDED INDUSTRY PRODUCT REVIEW

COMMUNICATIONS

Interphase Corporation

2901 N. Dallas Parkway, Suite 200
Dallas, Texas 75093
Tel.: 214-654-5000 • Fax: 214-654-5500

4531S Intelligent PMC T3/E3 Communications Controller

(passive also available)

www.interphase.com

The 4531S PMC ATM over T3/E3 communications controller is designed for carrier-class telecommunication networks supporting the most demanding ATM applications in broadband Internet access and integrated voice and data over carrier and enterprise ATM backbones. This ready-to-use, single port T3/E3 line interface is fully standards-compliant and features software development tools to facilitate immediate integration into CompactPCI, VME or other custom telecommunication platforms. Featuring a powerful MPC8260 RISC onboard processor at 200 MHz, high performance architecture, and advanced ATM functionality, the 4531S is the industry's best choice for a powerful PMC I/O solution in high availability servers driving next-generation wireless broadband telecommunications. A passive, more economical T3/E3 solution is also available with Interphase's 4531.

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For more information, visit www.interphase.com.

FEATURES

- Gateway-on-a-card capable for bridging of ATM and Ethernet networks on a single slot
- Motorola's MPC8260 (PowerQUICC II) onboard processor at 200 MHz
- ATM protocol support for VBR, CBR, and UBR Quality-of-Service (QoS) classes
- Fully integrated Fast Ethernet port on front panel
- Software selectable T3 or E3 line interface

RSC #63 @ www.embedded-computing.com/rsc

Interphase Corporation

2901 N. Dallas Parkway, Suite 200
Dallas, Texas 75093
Tel.: 214-654-5000 • Fax: 214-654-5500

INTERPHASE
Designed To Perform. Designed To Last.

4532 Intelligent PMC OC-3/STM-1 Communications Controller
(passive also available)

www.interphase.com

A gateway-on-a-card, the 4532 is an intelligent ATM over OC-3/STM-1 controller, enabling direct connectivity to SONET/SDH facilities, thus eliminating the need for additional line termination equipment. Featuring a software selectable 155-Mbits/sec SONET/OC-3 or SDH/STM-1 interface plus 10/100Base-T Ethernet interface, the 4532 supports ATM to Ethernet interworking. This functionality enables bridging of ATM and Ethernet networks on a single card instead of an entire system. Other features: ATM adaptation layers AAL0, 2, and 5; integrated CSU; and robust software development environment for VxWorks and Solaris. Custom software is also available. Purpose-designed for the most demanding ATM applications, including 2G/3G wireless (UMTS/W-CDMA, CDMA2000/1 x RTT, and 3 x RTT), broadband Internet access (DSLAMs, gateways, etc.), integrated voice/data over enterprise ATM backbones, and converged next-generation networks (softswitches, media gateways, etc.). New network processor blades are also available and are purpose-built for 3G wireless and converged NGN applications. The 4576 is also available as a passive OC-3/STM-1 solution that is price/performance maximized.

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For more information, visit www.interphase.com.

FEATURES

- Motorola MPC8260A (PowerQUICC II™) onboard 300 MHz processor
- Gateway-on-a-card capability for bridging ATM and Ethernet networks
- One software selectable SONET/SDH OC-3/STM-1 interface (front access)
- One Fast Ethernet interface (front panel)
- Supports up to 64,000 virtual connections
- Telecom clock management, master or slave synchronization modes
- Integrated CSU eliminates the need for additional line termination equipment and allows direct connectivity to SONET/SDH facilities.
- ATM protocol support for VBR, CBR, and UBR Quality-of-Service classes
- Robust software development tools for seamless integration with a common architecture to most Interphase products for ability to "mix-and-match" between various interfaces and form factors

RSC #64 @ www.embedded-computing.com/rsc

Interphase Corporation

2901 N. Dallas Parkway, Suite 200
Dallas, Texas 75093
Tel.: 214-654-5000 • Fax: 214-654-5500

INTERPHASE
Designed To Perform. Designed To Last.

4539 Intelligent PMC T1/E1/J1 Communications Controller
(CompactPCI, PCI, CPSB also available)

www.interphase.com

One card does it all – an unprecedented *gateway-on-a-card* technology on the Interphase T1/E1/J1 product family. Voice, data, ATM, frame relay, and signaling traffic can be intermixed in order to migrate to advanced networks without the replacement of legacy equipment. The following services can be supported, some simultaneously, on one card: ATM, SS7, PPP, HDLC, Ethernet, Frame Relay, X.25, ISDN, ATM to Ethernet interworking, SS7 to Ethernet interworking, frame relay and voice traffic over TDM, frame relay conversion to IP over Ethernet, signaling and IP over Ethernet, frame relay conversion to ATM, signaling termination of narrowband to broadband SS7 interworking, ATM to TDM interworking, and voice pass-through to DSPs. Other features include: Inverse Multiplexing for ATM (IMA) – Aggregates bandwidth of up to eight T1 lines; four to eight software-selectable T1/E1/J1 interfaces; 10/100Base-T Ethernet interface for remote LAN capability or interworking connectivity; integrated CSU eliminates the need for additional line termination equipment; MPC8264 processor at 300 MHz. Purpose-built for 2G/3G wireless, broadband network access, and converged next-generation networks (NGNs: softswitches, media gateways, etc.).

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For more information, visit www.interphase.com.

FEATURES

- MPC8264 (PowerQUICC II) 300 MHz onboard processor
- Four or eight software selectable T1/E1/J1 interfaces with options for front or rear access (8 ports on CompactPCI and CPSB products only).
- One Fast Ethernet interface for remote management or interworking
- Integrated CSU on T1 lines (eliminating the need for additional line termination equipment) with support for Facility Data Link
- Support for ATM AAL0, AAL2, and AAL5 Adaptation Layers
- Multiprotocol capable to support SS7, ATM, Frame Relay, X.25, ISDN, HDLC, and PPP, plus interworking of multiple protocols including ATM to Ethernet, SS7 to Ethernet, and Narrowband SS7 to Broadband SS7
- Inverse Multiplexing for ATM (IMA), with support for up to eight T1/E1/J1 lines for cost-effective bandwidth aggregation
- PICMG 2.15 PTMC compliance (on PMC card)
- PICMG 2.16 CPSB compliance (on 1635 product)

RSC #65 @ www.embedded-computing.com/rsc

Interphase Corporation

2901 N. Dallas Parkway, Suite 200
Dallas, Texas 75093
Tel.: 214-654-5000 • Fax: 214-654-5500

iNAV 9200 Multiprotocol Gateway Appliance
(or as a Blade)

www.interphase.com

Application-ready solution offers multimillion packet processing per second, predeveloped protocol stacks for ATM-Ethernet interworkings, and more. The Interphase iNAV 9200 series offers up to three times the protocol processing performance at a fraction of the price and equipment real estate of alternative gateway solutions for broadband access networks. iNAV 9200 is an advanced protocol bridging solution for DSLAM, cable head-end (CMTS), and fixed wireless (LMDS) access environments. In addition, it can function as a standalone multiservice switch, wireless gateway, or a media gateway, and can also be used to perform packet routing/classification, ATM switching, or ATM Segmentation and Reassembling (SARing). Initial iNAV 9200 units will perform ATM–to-Ethernet or Ethernet-to-ATM interworking using multiple OC-3/STM-1 and Fast/Gigabit Ethernet interfaces. Future versions will support multiple network protocols over T1/E1/J1, T3/E3, and OC-12/STM-4 interfaces. A blade format of this solution is also available, the Interphase iNAV 4000, operating as one function in a multi-slot, multipurpose system.

FEATURES

- Up to 5X improvement in price-to-performance ratio over router alternatives on the market today for bridging ATM and Ethernet networks
- Purpose-built for convergence, wireless, and broadband access applications
- Wintegra WinPath Packet Processor: Revolutionary design purpose-built for high-end access networking yielding multimillion packet processing per second
- ATM to Ethernet interworking function bridges ATM and Ethernet networks
- High degree of configurability via industry standard Command Line Interface (CLI) and SNMP-style management
- Facilitates IP routing and classification, ATM switching, and SARing, Packets over SONET, and Ethernet-to-ATM interworking
- L2 to L4 header processing with extensive QoS features
- Data and control path functions in a single, highly programmable platform for cost efficiency and flexibility

For more information, visit www.interphase.com.

RadiSys

5445 NE Dawson Creek Drive
Hillsboro, OR 97124

SYS50

www.radisys.com

RadiSys SYS50, the industry's first fully integrated, CompactPCI PICMG 2.16 platform. The SYS50 is ideal for high availability applications such as signaling, media gateways, VoIP gateways, switching and routing functions, billing servers, and storage servers including HLR and VLR. The RadiSys SYS50 is the latest addition to the company's family of switched fabric blade products based on CompactPCI, CompactPCI 2.16, and ATCA form factors and broadens the company's range of modules for blade servers, SS7, dual OC-3c line cards, and NPU modules, among others.

The RadiSys SYS50 is an integrated platform consisting of a 9U chassis, layer 2 switches, CPU blades, media modules, and platform management capability all integrated with the operating system. RadiSys has pre-validated each building block to ensure platform level compatibility. This means customers no longer need to spend their precious development time performing validation testing of individual building blocks from multiple vendors, which can be time consuming. Instead, the RadiSys SYS50 provides customers a proven system platform that can be used as the foundation for their production configuration, shaving months off their development time.

FEATURES

- PICMG 2.16-compliant 9U platform
- High availability design
- Redundant 24-link port
- Fast Ethernet, Layer 2 switches with built-in platform management software
- Intel 1.2 GHz Pentium® III Processor-M
- 512 Mbytes SDRAM with ECC
- Ultra-2 SCSI controller (via PMC and PIM)
- IDE: includes a 20-Gbyte IDE hard disk drive and a 32x CD-ROM drive

For more information, visit www.radisys.com.

Zephyr Engineering, Inc.

1620 West Fountainhead Pkwy., Suite 320
Tempe, AZ 85282-1876
Tel.: 480-736-8714 • Fax: 480-732-8322

ZPC.1900 Security Processor Development Platform

www.ZPCI.com

The ZPC.1900 Security Processor Development Platform from Zephyr Engineering, Inc. is a high-performance platform suitable for software development of security applications, and is the ideal development platform for MPC180, MPC184, MPC185, or MPC190 security processors. The ZPC.1900 Security Processor Development Platform has onboard MPC180 and MPC185 security processors and offers a complete single board solution. It also supports a 32-bit 33/66-MHz PMC card, so you can add either a ZPCI.3900 MPC190 security processor module or a ZPCI.3901 MPC184 security processor module.

The standard ATX form factor gives you system flexibility and allows mounting in a variety of off-the-shelf cases from desktop to rugge-dized rack-mount. There are plenty of onboard resources with 64 Mbytes of 64-bit SDRAM DIMM (expandable to 128 Mbytes), 2 Mbytes of Flash (expandable to 18 Mbytes), two Ethernet ports (10Base-T and 100Base-T), two RS-232 ports, JTAG COP connector for CPU emula-tor, and Mictor logic analyzer connectors. You have all the resources you need to develop your applications. The ZPC.1900 is your solution to long hardware lead times and is perfect for software developers. Set up your software environment virtually overnight and start development immediately.

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For more information, e-mail info@ZPCI.com.

FEATURES

- MPC8265 CPU with onboard MPC180 and MPC185 security processors
- 32-bit, 33/66-MHz PMC slot for MPC184 and MPC190 security processor modules
- Onboard 2 Mbytes Flash ROM with SIMM socket for expansion to 18 Mbytes
- DIMM socket for up to 128 Mbytes SDRAM
- Separate 8-Kbyte EEPROM for boot configura-tion
- One each 10Base-T and 100Base-T Ethernet ports
- JTAG COP CPU emulator connector
- Two RS-232C serial ports
- Three 96-pin DIN connectors for user expansion
- Mictor connectors for logic analyzer connection
- Standard motherboard footprint fits standard ATX chassis

RSC #68 @ www.embedded-computing.com/rsc

SBS Technologies, Inc.

2400 Louisiana Blvd.
Albuquerque, NM 87110

IB4X-PMC 2

www.sbs.com

SBS' dual-port, 10-Gbit/sec, PMC InfiniBand Host Channel Adapter (HCA) is engineered to drive the full performance of high-speed InfiniBand fabrics. Designed to provide the high throughput and low CPU utilization required for a 10-Gbit/sec database or High Performance Computing Clustering (HPCC), the HCA is configured with 256 Mbytes of DDR memory. The InfiniBand architecture defines and supports many applications, most with Remote Direct Memory Access (RDMA) capabilities. RDMA, combined with the inherent characteristics of InfiniBand, offers a high level of dexterity and enables high performance clustering, com-munication, and storage traffic to run over an InfiniBand fabric. Application support includes: Sockets Direct Protocol (SDP) for running over existing TCP applications without modifica-tion; Internet Protocol over InfiniBand (IpolB) to run IP over InfiniBand links; SCSI Remote Protocol (SRP) for storage area networking (SAN). Embedded application support includes: video streaming, aerospace, military, and elec-tronic controls. The IB4X-PMC-2 is based on Mellanox's InfiniHost™ silicon featuring an HCA core capable of full-wire-speed trans-missions over InfiniBand links. With a full hardware implementation of the InfiniBand architecture and hardware transport, the core fully supports RDMA transfers to reduce CPU overhead and to free the host processors for application use.

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Visit www.sbs.com for more information.

FEATURES

- Second-generation, 10-Gbit/sec, InfiniBand 4x HCA PMC IBTA v1.0a compatible design
- Supports up to 16 million queue pairs
- InfiniRISC™ embedded RISC processor
- HCA core capable of full-wire-speed transmis-sions over InfiniBand links
- Low latency transport
- 256 Mbytes DDR memory
- Multicast, atomic, and large message support
- Support for eight data VIs, plus the VL15 man-agement lane
- Sophisticated Quality-of-Service (QoS) features

RSC #69 @ www.embedded-computing.com/rsc

Advantech Embedded Computing

15375 Barranca Parkway, Suite A-106
Irvine, CA 92618
Toll Free: 1-800-866-6008

ADVANTECH Embedded Computing

OFPC-215

www.advantech.com/acg

Advantech's OFPC-215 Series Open Frame Panel Computer is the newest model of our reengineered Open Frame PC line designed to provide customers with maximum flexibility, performance, and integration ease. The OFPC-215 Series includes a touch-panel monitor with a computer system box joined together, perfect for integration into large, more complex systems. Because of the OFPC-215's modular design, customers can choose the right SBC/LCD panel configuration that suits their application needs best, plus use numerous third-party components. The modular design allows for easy upgrades and the flexibility to be easily adapted to different housings as well. Scalable from Pentium III CPUs up to 1.26 GHz for increased multimedia support to a VIA low power processor for reduced cost and lower power usage, the OFPC-215 simplifies cabling issues, I/O configuration, and chassis design. Great flexibility and scalable – Advantech Open Frame computers are designed to fit anywhere developers have space or environment constraints. Flexible and interchangeable choices are key to meeting niche application needs. The OFPC-215 is based on our industrial-proven box PC series that offers a choice of integrated SBCs that can go into housings and can easily be mounted on or into equipment. Our LCD touch monitors have been used in the harshest environments, including HMI, kiosks, and other applications. Their steel, open frame design can integrate customers' specific IDs (faceplates) for image and branding concerns. The system is prime for expansion, with ordering options such as Giga-LAN, VESA mounting, and CD-ROM/RW/Combo available. The unit accepts all major OS configurations, with available embedded OS and driver support.

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For more information, visit www.advantech.com/acg.

FEATURES

- 15" high brightness TFT LCD with 1024 × 768 resolution
- Touch panels provide options, including SAW, capacitive, resistive, SAW for vandal proof, and strength
- Computer system boxes provide SBC options of P III, VIA low power processor, or Ezra
- Attachable and detachable LCD touch panels in different sizes and different levels of SBC systems
- On Screen Display (OSD) for screen tuning and quick display adjustment
- Strong standalone system with a versatile function set that includes support for 1x SDRAM up to 512 Mbytes
- 2" × 3.5" HDD bays
- PCI and PC/104 expansion
- 2 × USB ports, 1 × parallel port, 4 × serial ports, 1 × 100Base-T Ethernet
- PS/2 keyboard and mouse ports
- MIC-in, SPK-out, Line-in/out, DC-out (for LCD) and CD-audio in

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Datalight Inc.

21520 30th Dr SE, M/S110
Bothell, WA 98021

Datalight®

TS-5600 SBC

www.datalight.com

ROM-DOS is the essential operating system for x86 devices. Since its introduction in 1989, ROM-DOS is the essential operating system for x86 devices. From its long success in the embedded arena, ROM-DOS has expanded worldwide into desktops and servers. ROM-DOS handles today's large disk drives and long file names.

With ROM-DOS, the current standards of long filename support, permitting file names up to 255 characters, FAT32 support, and providing complete access to large disk drives, are directly available within the kernel, so no extra drivers need to be loaded. Long file names can be read, written, and deleted on large hard drives with ROM-DOS using standard DOS/Windows APIs. Minimize your risks. ROM-DOS is solid and fully supported. The interface to DOS and its internal functions are well documented. Instead of spending valuable development time researching function calls or learning new development suites, you can go straight to work using a stable, well understood OS, and save costs.

ROM-DOS gives you the power and freedom to manipulate ROM creatively. You can embed the OS, as well as applications. With Datalight's Superboot technology, you can create hidden partitions that can reside on any disk. Within a ROM-DOS Superboot partition you can contain system recovery software, so if software fails, you can restore the device from ROM and avoid the costs of failed product returns.

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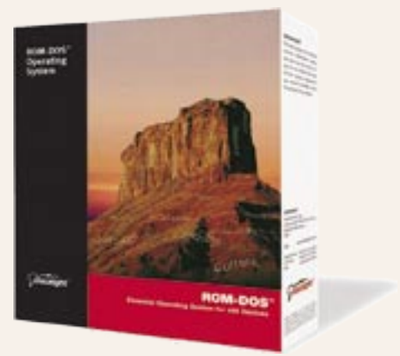
Visit www.datalight.com for more information.



FEATURES

- RXE – Relocatable Executables
- Build – Customizable Kernel
- Dynamic device driver
- SOCKETS™ – embedded TCP/IP stack
- FAT32 kernel support
- LFN kernel support
- Full technical support
- Datalight Reliance™
- Datalight FlashFX

RSC #71 @ www.embedded-computing.com/rsc

Grid Connect

Tel.: 630-245-1445 • Fax: 630-245-1717
E-mail: sales@gridconnect.com

CAN Interfaces: USB, PCI, Parallel, and Chips

www.gridconnect.com

Grid Connect supplies all types of CAN products for developers and plant engineers. The complete set of adapters for CAN 2.0B support baud rates up to 1 Mbit and a full featured set of software. The adapters for the PC include USB, Firewire, Parallel, PCI, ISA, PC/104, and custom. The rich set of software includes a FREE set of Windows or Linux drivers with a basic software API. A more advanced API is available for a small cost. Protocol aware tools and stacks are available for many protocols including: CANOpen, DeviceNet, J1939, and others. Diagnostic tools for CAN, CANOpen, and Detective are also available to help the end-user troubleshoot live network problems. The DSTni-LX and EX chips with two on-chip CAN interfaces provide the embedded OEM a single-chip solution with royalty FREE software. The DSTni chips provide high-speed CAN hardware and protocol software along with the other integrated peripherals: 10/100Base-T, serial ports, SPI, I2C, USB, and Profibus. Grid Connect (formerly Synergetic/Lantronix) has been a leader in the embedded and networking marketplace for more than 15 years. Grid Connect believes companies should provide network hardware (chips, controllers, and packaged systems) at reasonable prices and provide high quality software and services to their customers.

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For more information, e-mail sales@gridconnect.com.

FEATURES

- Hardware adapters for USB, Fireware, Parallel, PCI, PC/104, and ISA
- Free Windows 98/2000/NT device drivers
- Free software API to read/write/open/close
- Free Linux device driver
- Advanced software API available for complex software applications
- DeviceNet and CANOpen tools
- DSTni-LX and EX system-on-chip solutions for embedded OEMs
- Full CAN 2.0B compliance
- Custom hardware and software available

RSC #72 @ www.embedded-computing.com/rsc

Hartmann Elektronik GmbH

Motorstrasse 43 • D-70499
Stuttgart, Germany
Tel.: +49 711 13989 0 • Fax: +49 711 8661191

Bridge Boards

www.hartmann-elektronik.de

The Bridge boards by Hartmann Elektronik provide an interface between the PCI/CompactPCI bus and StarFabric. The bridge translates parallel PCI traffic into serial frame format for transmission across StarFabric. The fabric interface consists of two, 2.5-Gbit/sec full duplex links. These links comprise four aggregated 622-Mbit/sec LVDS differential pairs, which greatly simplify implementation. It's your choice: The two links can be bundled to create a 5-Gbit/sec full duplex unit. Or, if you prefer, a redundant connection can be implemented by using the links separately.

StarFabric – a net of PCI buses: The bridge boards extend your PCI bus and connect it to other PCI or CompactPCI systems – and at distances of up to 13 meters in each case. This configuration allows a single low-priced PC CPU to control more than 1000 Compact PCI system components – with data transfer rates of up to 880 Mbytes/sec. Greatest benefit to you: The bridge mode (transparent function) does not require additional software drivers that slow down your system.

The parallel data traffic is converted to a serial format by a StarFabric IC and transferred via cat5 cable pairs.

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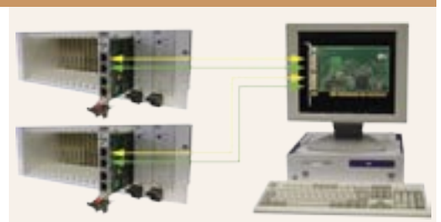
For more information, e-mail info@hartmann-elektronik.de.



FEATURES

- Separate application: concurrent data transfer to two remote systems
- Non-transparent mode: economical clustering of several CPUs, increased computing power, creation of redundant systems

RSC #73 @ www.embedded-computing.com/rsc

Lanner Electronics Inc.

925 Canada Court
City of Industry, CA 91748
Tel.: 626-581-1898 • Fax: 626-581-1897

EM-660A/B

www.lanner-usa.com

EM-660A/B is based on the VIA Eden low-power processor and the feature rich VIA VT8606/VT82C686B chipset. The VT8606 chip with integrated graphics supports a 36-bit LDC display panel and two channels of 18-bit LVDS. Other features include one SODIMM socket for up to 512 Mbytes of SDRAM system memory, one Realtek RTL8100B 10/100Base-T NIC, one PCI expansion slot, one CompactFlash type I/II socket, one PC/104 slot, and four COM ports.

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E-mail: sales@lanner-usa.com for more information.

FEATURES

- VIA Eden/Ezra low-power CPU onboard
- VIA chipset with integrated AGP 4X graphics
- 36-bit TFT and two channels LVDS support
- 10/100Base-T NIC and AC-97 audio
- Four COMs, one LPT, four USBs, one IrDA, and PC104/PCI

RSC #74 @ www.embedded-computing.com/rsc

MEN Micro

3740 North Josey Lane, Suite 203
Carrollton, TX 75007
Tel.: 972-939-2675

EM04N Embedded System Module

www.menmicro.com

The EM04N, an Embedded System Module (ESM), is a complete SBC. ESMs address the most common challenges of embedded applications: how to meet tailored application-specific I/O requirements while minimizing development time and design risk. Specialized I/O on an ESM can be implemented on a customized carrier board, keeping design costs low and making the final solution extremely cost-effective. ESMs consist of basic hardware including a processor, support chipset, memory, and common computer I/O. Most ESMs include an FPGA for implementing application-specific I/O. Board support packages (BSPs) are available for the most prevalent operating systems. A complete embedded system can be configured with a standalone ESM, with an ESM on an application-specific carrier card, or with an ESM and stacked PC/104-*Plus* I/O modules. The EM04N features the MPC8245 PowerPC (Kahlua II) microprocessor with clock speeds from 266 MHz to 400 MHz. The EM04N is ideal for low-cost, deeply embedded applications in harsh environments, such as machine control, man-machine interfaces, fieldbus bridges, or embedded Linux PCs.

The EM04N has a large onboard FPGA that can be used to implement a wide variety of I/O functionality, including graphics controllers, serial interfaces, CAN bus, or others.

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Visit www.menmicro.com for more information.

FEATURES

- PowerPC MPC8245/266 MHz (optional 400 MHz)
- Cyclone 250,000 gate FPGA
- Up to 512 Mbytes SDRAM
- SO-DIMM socket for SDRAM
- CompactFlash socket
- Graphics controller (with 16 Mbytes SDRAM) via FPGA Dual 100Base-T ports
- Two serial RS-232 communications ports
- Additional interfaces for CAN and IDE via FPGA
- Linux and VxWorks board support

RSC #75 @ www.embedded-computing.com/rsc

Mercury Computer Systems, Inc.

199 Riverneck Road
Chelmsford, MA 01824

ImpactRT 3100

ImpactRT 3100

www.mc.com

The First RapidIO Multi-computer – The ImpactRT 3100 multi-computer is the new flagship of Mercury's product line, scaling to 2.4 TeraOPS of processing and over 60 Gbytes of communication ban width in a single CompactPCI chassis. This quantum leap in system performance delivers a strong long-term growth path for developers of applications in medical imaging, semiconductor wafer inspection, defense electronics, or any industry where high compute density is required.

Power: Up to 600 GFLOPS/2.4 TeraOPS – The ImpactRT 3100 architecture balances computing, communications, and I/O, scaling system capabilities to meet a wide range of application-specific requirements. Harnessing PowerPC 7445 microprocessors to reach 600 GFLOPS or 2.4 TeraOPS, the ImpactRT 3100 multi-computer has the muscle to plow through the toughest computing tasks.

RapidIO bandwidth: 60 Gbytes/sec – Communication bottlenecks are eliminated by a RapidIO switch fabric. Each compute node and I/O node in the ImpactRT 3100 system has a direct connection to the RapidIO switch fabric, yielding an aggregate of 60 Gbytes/sec of simultaneous communication among the nodes. This tremendous bandwidth supports an immense amount of data streaming through the system so that the computational power of the ImpactRT 3100 gets maximum utilization.

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For more information, visit www.mc.com.

FEATURES

- The first RapidIO multi-computer
- Scales to 76 processors
- Up to 600 GFLOPS/2.4 TeraOPS
- 60 Gbytes/sec over the RapidIO switch fabric
- Up to 10 Gbytes/sec Fiber I/O
- Software compatible with RACE++ systems

RSC #76 @ www.embedded-computing.com/rsc

EMBEDDED INDUSTRY PRODUCT REVIEW

INDUSTRIAL

Micro/sys

3730 Park Place
Montrose, CA 91020

MICRO/SYS

SBC1586

www.embeddedsys.com

The SBC1586 is a Pentium PC/104 computer with CompactFlash. Based on the Low-Power Embedded Pentium processor with MMX technology, it packs plenty of memory and copious amounts of storage into a PC/104-sized board.

With 1 Mbyte of onboard Flash, accessible as a read/write disk, and up to 256 Mbytes of DRAM, many large programs can be run. However, if additional storage capacity is required, the CompactFlash connector allows hundreds of megabytes of removable program and data storage. External IDE drives can also be connected when necessary.

Four serial ports, 10/100Base-T Ethernet, a printer port, a USB port, three counter/timers, and a watchdog timer mean that the SBC1586 won't require any additional I/O for many applications. However, if additional capabilities are needed, PC/104 expansion allows a wide variety of I/O cards to be stacked on the SBC1586.

Micro/sys installs a ready-to-run firmware system at no cost. This firmware includes a complete industrial BIOS, board setup screens, and application download utilities, and can create a DOS-like execution environment immediately upon powerup. Borland or Microsoft C/C++ 16-bit .EXE files can be downloaded to the board upon receipt. Alternatively, the computer may be configured to boot 32-bit operating systems upon powerup. A development kit that includes cables, sample software, and full documentation is available.

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For more information visit www.embeddedsys.com.

FEATURES

- Compact PC/104 footprint
- Low-Power Pentium, 166 or 266MHz
- Up to 256 Mbytes SDRAM
- CompactFlash connector
- Four serial ports
- One USB port
- 10/100Base-T Ethernet
- Watchdog timer
- CPU and ambient temperature sensors
- Floppy and IDE drive interfaces
- Battery-backed real-time clock
- DOS, Windows 95/98/NT, Linux, Windows CE, NT Embedded, VxWorks

RSC #77 @ www.embedded-computing.com/rsc

Microbus Inc.

10849 Kinghurst, Ste. 105 • Houston, TX 77099
Tel.: 1-800-688-4405 • Fax: 281-568-4604
E-mail: sales@microbus-usa.com

WIB200 Series

www.microbus.com

WIB200 is a rugged, full-featured Wireless LAN product family in the PC/104-*Plus* form factor. The WIB200 modules plug onto your PC/104-*Plus* CPU modules and upgrade your embedded system into a wireless network device. The WIB200 modules are now available for all the 802.11x modes: 11b, 11a, 11g, and 11a/b/g. These modules include a complete set of drivers and networking tools to support operating systems including Windows ME, 98SE, 2000, XP, and Linux.

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For more information, visit www.microbus.com.

FEATURES

- PC/104-*Plus* form factor
- Rugged design
- Single or dual antenna
- 802.11b, 2.4 GHz, 11 Mbits/sec
- 802.11a, 5 GHz, 54 Mbits/sec
- 802.11g 2.4 GHz, 54 Mbits/sec
- 802.11a/b/g multiband

RSC #78 @ www.embedded-computing.com/rsc

SBS Technologies, Inc.

2400 Louisiana Blvd.
Albuquerque, NM 87110

PC7 Rugged

www.sbs.com

A rugged all-in-one computer with integrated power supply installed in a very compact EMI-protected metal housing – dust and water proof per IP67. The PC7 Rugged is designed to meet the needs of embedded applications such as machine control, communication, data processing, data acquisition, etc. It addresses industrial automation, measurement, military, and similar markets with the protection needed to conform to class IP67. Supported operating systems are Windows 2000/ NT/ XP, QNX, VxWorks, Linux, and others. The all-in-one concept with flexible processor and RAM configurations and an impressive array of peripherals including video interface, Ethernet, HD, and FlashDrive, combined with a custom specific assembly service provides optimized price/performance for all kinds of OEM applications. Special features include four serial channels with flexible opto-isolated RS-232 or RS-422 interfacing, a CANbus device for low-cost fieldbus I/O, and five opto-isolated I/O lines. Three PC/104-*Plus* slots enable custom specific extensions such as Interbus-S, Profibus, Device-Net, and others. Rugged needs are addressed with an extended temperature range of up to –40°C to +50°C, and with increased shock and vibration immunity.

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Visit www.sbs.com for more information.

FEATURES

- Custom specific, low-cost assembly versions available
- 566-MHz Celeron; 700-MHz Pentium III
- CE compliant
- EMI protection, Flash drive up to 512 Mbytes or local 2.5" hard disk
- Conduction cooling
- Optional –40°/+50°C
- Fast Ethernet
- CANbus for low-cost I/O
- 10-30VDC power supply
- Three PMC/104+ extension slots
- Up to 256 Mbytes SDRAM with ECC
- Opto-isolated I/O

RSC #79 @ www.embedded-computing.com/rsc

SCIDYNE
649 School Street
Pembroke, MA 02359-3649
Tel.: 781-293-3059 • Fax: 781-293-4034

ADIO-104 Analog and Digital I/O Module

www.scidyne.com

Analog and digital I/O module designed to satisfy mainstream and cost-sensitive applications. The ADIO-104 will be the only peripheral board required in many instances. The sixteen single-ended, 12-bit analog inputs are independently programmable to operate in one of four ranges: ±5V, ±10V, +5V or +10V. This feature effectively increases the dynamic range to 14-bits when using range-switching software techniques. The analog-to-digital converter operates at up to 50 Ksamples/sec and allows the separate acquisition and conversion intervals to be controlled by the host software or automatically timed by the ADIO-104 hardware. A special feature allows simultaneous (Phase-Coherent) acquisition on identically configured analog input pairs. Eight 12-bit analog outputs are provided and share a common jumper selectable output range and can be updated simultaneously using a single software command, a necessity in phase-critical applications such as X-Y positioning. Depending on the model purchased, all analog outputs are automatically set to zero-scale (RZ) or mid-scale (RM) during a hardware reset. Three 8-bit digital I/O ports are provided. PORT-A is bidirectional and can be software programmed for input or output operation on a 4-bit nibble basis. PORT-B has six bidirectional channels and two dedicated input channels. Pull-up resistors on the four lower channels simplify connections to external switches, contact closures, and open-collector devices. PORT-C is an output-only port.

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For more information, visit www.scidyne.com.

FEATURES

- Analog I/O and digital I/O in an inexpensive PC/104 module
- Sixteen 12-bit, multi-range analog inputs (±10V, ±5V, +5V, +10V)
- Over 50 Ksamples/sec analog input throughput, self-timed or user-controlled acquisition
- Eight 12-bit multi-range analog outputs (+5V, +10V, –5V, –10V, ±5V, ±10V)
- 24 digital I/O channels, four of which are 50VDC open-drain outputs
- One 8-bit binary pulse accumulator (counter)
- Interrupt fully supports sharing and access to all PC/104 bus IRQs
- Single +5V power requirement
- PORT-C four upper channels feature 50V165ma open-drain MOSFETs
- Standard J1/P1 stack-through connector
- Optional J2/P2 connector provides 16-bit stack-through compatibility

RSC #80 @ www.embedded-computing.com/rsc

EMBEDDED INDUSTRY PRODUCT REVIEW

INDUSTRIAL

SCIDYNE
649 School Street
Pembroke, MA 02359-3649
Tel.: 781-293-3059 • Fax: 781-293-4034

DIO96-104 High-Density Digital I/O Module 100-7618

www.scidyne.com

The DIO96-104 provides 96 TTL/CMOS compatible digital I/O channels arranged as four 24-bit groups. Each group is divided into three 8-bit ports and is controlled by a separate 82C55A peripheral interface chip. This industry standard device offers very flexible configurations, including software programmable port directions and strobed I/O handshaking. The I/O circuitry has been designed without passive pull-up or pull-down resistors allowing the user's application to individually dictate how each channel will be handled during reset and input modes. External devices connect to the DIO96-104 through four identical 26-pin IDC flat-ribbon headers, which include access to the host's +5VDC supply for powering external circuitry. A standard J1/P1 stack-through connector allows the DIO96-104 to reside anywhere within an 8-bit PC/104 stack. Adding an optional J2/P2 connector provides 16-bit stack-through compatibility.

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For more information, visit www.scidyne.com.

FEATURES

- 96 digital I/O channels
- Uses industry standard 82C55A chips
- Supports input, output, and strobed I/O operations
- Low-power CMOS design
- Single +5V power requirement

RSC #81 @ www.embedded-computing.com/rsc

Technobox

PMB 300 • 4201 Church Road
Mt. Laurel, NJ 08054

3761

www.technobox.com

The 3761 is an Ultra 160 SE/LVD SCSI controller. The ULTRA160 SCSI PMC provides an interface connection between a host board PCI bus and a SCSI device. Designed around an LSI Logic 53C1000 controller, the 3761 supports operation with either single-ended or low-voltage differential signaling. The 53C1000R also features an intelligent processing engine that reduces processor overhead in handling SCSI interface operations. Signaling mode is automatically set. Furthermore, the board will automatically accommodate 32 or 64-bit bus width, 3.3V or 5V signaling, and either a 33 or 66-MHz clock. The SCSI bus is available out the front panel through a 68-pin VHDCI connector per ANSI X3.131 specification. An active termination network for each SCSI signal line terminates the SCSI bus. Termination can be toggled on or off by setting a DIP switch. Onboard LEDs indicate operational status.

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For more information, visit www.technobox.com.

FEATURES

- Provides a single Ultra160 SE/LVD interface
- LSI 53C1000R controller
- Front panel connectivity via 68-pin VHDCI connector with user-selectable active termination
- Automatic setting of signaling mode, bus width, and clock
- Front-panel status LEDs
- Flash-resident boot code

RSC #82 @ www.embedded-computing.com/rsc

Technoland

1050 Stewart Drive
Sunnyvale, CA 94085

TL-EmbSBC ET710

www.technoland.com

Technoland introduces a cutting-edge ETX (Embedded Technology Extended) CPU module, the TL-EmbSBC ET710. This module shortens product development time and offers flexible time-to-market solutions for OEM/ODM clients. The TL-EmbSBC ET710 is an embedded plug-on module. It can be placed on a customized baseboard according to the customer's specific needs. Since the baseboard can be designed separately, it can dramatically reduce custom product development time.

The TL-EmbSBC ET710 is an extremely compact CPU module based on the Intel 815EB chipset. The board also has four board-to-board, high-density interface connectors for I/O signals that plug onto baseboards specific to customers' applications. Additional onboard standard interfaces include two IDEs, two serial ports, one parallel port, four USB ports, and one IrDA interface. Other advanced features for the TL-EmbSBC ET710 include PCI-to-ISA bridge support (three ISA compatible slots).

The ETX CPU fits the needs of industrial PC-based applications and can simply plug onto any form factors, including ATX, PICMG, CompactPCI, ISA, PCI, PISA, and VME, with no hassle. The interchangeability and scalability of both the TL-EmbSBC ET710 and the baseboard provide the fastest time-to-market solutions for embedded applications.

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Visit www.technoland.com for more information.

FEATURES

- Supports Intel Mobile Pentium III or ULV Celeron
- 133MHz FSB, 933MHz CPU clock
- Requires no CPU fan
- Intel 815EB chipset, ATI M6 VGA controller
- 16 Mbytes VGA memory, CRT/LCD support
- Intel 82801 10/100 LAN with Intel 82562E PHY
- One SO-DIMM socket for up to 512 Mbytes SDRAM
- 2 COM ports, 4 USB, watchdog timer, PCI-to-ISA bridge
- Small form factor: 95mm x 114mm (3.74" x 4.5")

RSC #83 @ www.embedded-computing.com/rsc

Technologic Systems, Inc.

16610 E. Laser Dr., #10
Fountain Hills, AZ 85268

TS-5600 SBC

www.embeddedx86.com

New PC-compatible SBC features PCMCIA slot, Fast Ethernet, IDE CompactFlash, 12-bit A/D, 12-bit DAC, digital I/O, and more. The new TS-5600 is a PC-compatible SBC based on the 133-MHz AMD 5x86 with 32 Mbytes of onboard high-speed SDRAM (64 Mbytes available). The embedded PC BIOS provides the standard PC BIOS calls and redirects the console to a COM port. The standard PCMCIA slot supports 802.11b WiFi cards, cellular modems, and a wide variety of card bus and PC cards including: modems, ATA hard drives, network cards, and various data acquisition cards. The onboard Fast Ethernet adapter is connected via PCI bus to provide connection to Local Area Networks and the Internet. The system will boot to an IDE device in the form of CompactFlash. Direct booting is supported for: Linux, DOS, QNX, Pharlap, SMX, etc. Technologic Systems' embedded distribution of Linux can provide complete network connectivity and includes kernel drivers for analog I/O, digital I/O, watchdog timer, etc. TS-Linux is open-source GNU/Linux using a 2.4.18 kernel and the standard GlibC. Many binaries will copy directly from a desktop system to TS-Linux and will run without modification. Analog options include a six-channel 12-bit A/D and a two-channel 12-bit DAC.

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Visit www.embeddedx86.com for more information.

FEATURES

- 133-MHz 586, 32 Mbytes RAM
- PC-compatible x86
- PCMCIA socket
- 10/100 Ethernet
- 12-bit A/D and DAC options
- Bootable IDE CompactFlash
- CMOS setup and RTC are PC standard, battery backup optional
- 23 digital I/O
- Alphanumeric LCD and matrix keypad interface
- Two RS-232 serial ports (RS-485 available)
- Single +5VDC supply
- PC/104 bus, dimensions: 4.3" x 5.6"

RSC #84 @ www.embedded-computing.com/rsc

VersaLogic Corp.

3888 Stewart Rd
Eugene, OR 97402
1-800-824-3163

Bobcat for industrial automation

www.VersaLogic.com

When selecting a PC board for your industrial application, be sure that it can withstand the harsh environment of the factory floor. Many computers don't have what it takes to stand up to the environmental fluctuations, shock, vibration, and contaminant exposure that industrial equipment may be subjected to. For real industrial applications, you need an embedded computer that is rock solid, well supported, and designed for rugged applications.

The Bobcat 586 PC/104-*Plus* SBC has earned a reputation for flawless operation in even the most extreme environments. The Bobcat utilizes a low-power 586 processor, accepts a DiskOnChip for up to 1 Gbyte local storage, includes four COM ports, a Fast Ethernet port, PC/104 and PC/104-*Plus* expansion, and 64 Mbytes of onboard RAM. Also, the Bobcat is available in an extended temperature (–40° to +85°C) version and can operate without a battery.

OEMs and system integrators especially like the field-upgradeable BIOS with reconfigurable defaults, remote network boot capability, and built-in reliability features like the Vcc-sensing reset circuit. There's a whole lot of functionality packed onto one PC/104-*Plus* board, combined with the advantage of VersaLogic support with every one we ship. (Platinum Vendor, VDC 2002-2003 industry reports.)

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Check out specs and pricing for the Bobcat and other VersaLogic products at www.VersaLogic.com/productinfo/.

FEATURES

- 133-MHz 486/586 class CPU
- 64 Mbytes system RAM
- Dual-speed fast Ethernet
- 32-pin DiskOnChip socket
- Battery-backed SRAM option
- Four COM ports
- PC/104 and PC/104-*Plus* expansion interface
- Watchdog timer
- Two general-purpose timer inputs
- Vcc sensing reset circuit
- Extended temperature option (100 MHz)
- Network boot capability (third-party boot code not included)

RSC #85 @ www.embedded-computing.com/rsc

Vibren Technologies

80 Central Street
Boxborough, MA 01719-1200

Reptron Modular Development Platform (MDP)

www.vibren.com

Vibren Technologies is a reseller of Reptron's Modular Development Platform (MDP) for embedded product solutions. The MDP system is a modular reference platform providing the software developer with a hardware target to complete application software development early in the product design cycle. The MDP includes a motherboard and pre-designed and tested plug-in modules including CPU module, LCD Panel Interface module, PCMCIA/CompactFlash module, I/O module, and Communication module. Vibren Technologies has developed a Windows CE .NET 4.2 board support package (BSP) for the MDP. Vibren's in-depth understanding of the platform allows for a complete software development solution including: BSPs for other embedded operating systems. Customization and enhancements to add new features and functions to match customer requirements. Custom application development and integration. Integration consulting to assist customers in determining how the board best fits into their architectural design.

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For more information, visit www.vibren.com.

FEATURES

- Motherboard; seven module slots, local bus interconnect
- SH7750R CPU with 16 or 32 Mbytes Flash, 64 Mbytes SDRAM
- Ethernet controller 10Base-T/100Base-TX USB 1.1 and four-channel serial port controllers
- PCMCIA and CompactFlash connectors
- Provides Wi-Fi and Bluetooth connections
- LCD controller with touchscreen and backlight controls
- Support for SVGA/64K colors or XGA/256 colors
- I/O module adds 36 user configurable I/O signals
- Future CPUs PXA255 XScale, ARM, SH7727/7760,
- Windows CE .NET 4.2 board support package
- System-level and application software development

RSC #86 @ www.embedded-computing.com/rsc

EMBEDDED INDUSTRY PRODUCT REVIEW

INDUSTRIAL

WinSystems, Inc.

715 Stadium Drive
Arlington, TX 76011 U.S.A.

EBC-C3

www.winsystems.com

The EBC-C3 is an EBX-compatible, Pentium-based SBC offering a wide operational temperature range from –40º to +85º celcius. This powerful CPU gives engineers a high-performance, cost-effective, and low-power x86 engine for computational-demanding, embedded applications.

Configured with a 733-MHz CPU, the EBC-C3 comes equipped with two 10/100 Ethernet controllers, advanced 4X AGP flat panel/CRT video support, four serial channels, 48 digital I/O lines, AC97 audio controller, and the standard AT peripheral feature set. It supports expansion with PC/104 and PC/104-*Plus* connectors or with 4 USB ports. The board measures 5.75" x 8.0".

The EBC-C3 is designed to run both 16-bit and 32-bit x86 instruction set software. It is compatible with Microsoft's Windows CE.NET and XPe systems along with the applications that run on them. It also supports Linux and other PC-compatible x86 operating systems such as QNX and VxWorks. Its PC software compatibility assures easy program development and checkout.

WinSystems has specialized in designing and manufacturing embedded computers for industrial applications for more than 22 years. The company has gained an excellent reputation for its innovative design and engineering skills and is recognized as a leading supplier of embedded PC board-level products.

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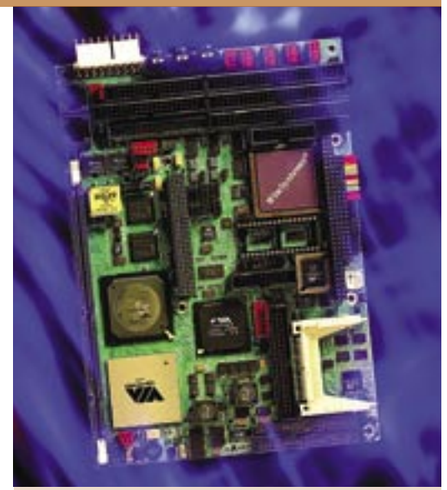
Visit www.winsystems.com more information.



FEATURES

- 733 MHz, low-power C3 processor
- x86-compatible, EBX-compliant SBC
- Dual 10/100 Ethernet and four USB controllers
- High resolution 4 x AGP video controller with CRT and LVDS flat panel support
- 48 Bidirectional TTL digital I/O lines
- Four RS-232 serial ports with FIFO, COM1, and COM2 with optional RS-422/485/J1708 support
- Two dual Ultra DMA/100 EIDE hard drive connectors
- Floppy disk controller supports one or two drives
- Bidirectional LPT port supports EPP/ECP
- 32 to 512 Mbytes of system SDRAM supported
- Socket for up to 1 Gbyte DiskOnChip or CompactFlash
- Operating temperature –40ºC to +85ºC

RSC #87 @ www.embedded-computing.com/rsc

Advantech Embedded Computing

15375 Barranca Parkway, Suite A-106
Irvine, CA 92618
Toll Free: 1-800-866-6008

ADVANTECH Embedded Computing

POC-123/153/173 Series

www.advantech.com/ehealthcare

Advantech's POC-123, POC-153 and POC-173 are medical-grade multimedia panel computers. These medical systems are UL2601-1/EN60601-1 approved, and the low-current leakage power supply enables them to act ideal and to secure point-of-care solutions for patients and hospital practitioners. The POC-123/153/173 series is specially designed to resist spills and water damage, and ensure dust resistance with their protected LCDs, sealed ports, and card slots. The quality, reliability, safety, and software support at the point-of-care is making it easier for hospital system integrators to incorporate POC-123/153/173 into their existing or new system configurations.

POC-123/153/173 series offers system integrators full-featured I/O and expansion slot (PCI/PCMCIA) capabilities. They integrate 12.1", 15" or 17", high brightness/high contrast LCDs (500:1 contrast ratio & 350 cd/m LCD), which are ideal for better image quality and PACS and DICOM applications such as intra-oral and endoscopy, CT, and ECG.

They are versatile point-of-care solutions with emphasis on dependability and safe, quiet operation. These panels feature an intuitive touch screen interface and are able to seamlessly integrate into any environment (supports 802.11b wireless).

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For more information, visit www.advantech.com/ehealthcare.

FEATURES

- UL2601-1/EN60601-1, CE and FCC Class B certified
- Point-of-care terminals for eHealthcare and medical applications
- 12.1", 15" or 17" LCD displays
- Spill and dust resistant
- 802.11b wireless antenna and touchscreen (optional)
- Supports VIA C3 Eden socket 370-based Pentium III/Celeron/VIA C3 CPU
- Supports up to 512 Mbytes SDRAM
- One 2.5" IDE HDD; 1.44 Mbytes
- Slim type CD ROM (Optional: CD RW/DVD ROM)
- Type II × 2 PCMCIA
- Fast Ethernet interface
- One PCI expansion slot

RSC #88 @ www.embedded-computing.com/rsc

Arcus Technology Inc.

4160-G Technology Dr.
Fremont, CA 94538

Arcus TECHNOLOGY

Proteus Series Motion Controller

www.arcus-technology.com

Arcus Technology introduces the Proteus Motion Controllers, innovative and cost effective stepper motion controllers for PC/104, PCI, and stand-alone platform with USB, Ethernet, and RS-232/485 communication interfaces.

The Proteus Motion Controllers come with full motion control features and capabilities: linear/circular interpolated motions, s-curve profiling, limits/home/alarm inputs, encoder feedback, text based multitasking motion programs, position latch inputs, synchronous outputs, digital servo interface, up to 72 digital inputs/outputs, analog inputs for general-purpose or joystick use, and much more.

Windows based program is provided to quickly setup, program, debug, and monitor the controllers. Communication drivers and sample codes in VB, VC++, and LabVIEW are provided for custom user-interface development. The stand-alone Proteus Motion Controllers also come with Proteus-PDA, a Palm OS interface program, and Proteus-WEB, a web-server capable controller that enables you to use Internet browser to monitor and control the Proteus Motion Controllers.

In addition to the Proteus Motion Controllers, Arcus Technology provides complete motion control solutions from integrated motor/driver package to custom-built OEM motion package.

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Visit www.arcus-technology.com for more information or contact our distributor, NetMotion by email: sales@netmotion.com or by phone: 800-790-7837.

FEATURES

- Four-axis stepper motion control
- Linear and circular interpolation
- Limits/home/alarm inputs
- Encoder feedback
- Digital inputs up to 72 points
- Analog inputs two channels
- Multitasking
- PC-104, PCI, standalone
- USB, Ethernet, RS-232/485

RSC #89 @ www.embedded-computing.com/rsc

VersaLogic Corp.

3888 Stewart Rd
Eugene, OR 97402
1-800-824-3163

PC/104 and EBX for medical electronic devices

www.VersaLogic.com

VersaLogic Corp. delivers top quality boards for use in medical and other high-tech industries. VersaLogic's embedded computers have many advantages over desktop PCs including long-term availability, rugged construction, high reliability, and compact size. Quality design features include latching I/O connectors, watchdog timers, voltage sensing reset circuits, programmable CPU temperature sensors, and more. Our high Mean Time Between Failure (MTBF) ratings translate into excellent field performance, eliminating costly field service calls and minimizing downtime.

You'll find VersaLogic products in diverse medical applications such as pacemaker calibration tools, endoscopic surgery devices, autoclaves, and phaco-emulsification equipment. A five-year product availability guarantee ensures that VersaLogic will keep your project online and supported for the long term.

Products that fit your application:

- EBX-compliant SBCs from Celeron to Pentium III
- PC/104-*Plus* processor modules from 586 to Pentium III
- PC/104 and PC/104-*Plus* expansion modules - Ethernet, video, I/O, and others.

VersaLogic Corp. prides itself on delivering the best service in the industry with its knowledgeable customer service and technical support staff. VersaLogic's support system generates the highest-rated customer satisfaction in the business, recognized by industry analysts Venture Development Corporation, with Platinum Vendor rankings in their 2002 and 2003 industry reports.

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For more information visit www.VersaLogic.com/medical/.

FEATURES

- PC/104, PC/104-*Plus,* and EBX form factors
- Low power and extended temperature boards
- Processors from 586 to Pentium III High Mean Time Between Failure (MTBF) rates
- ATi video chip, 4 Mbytes VRAM, 2D/3D support
- Expansion modules for add-on functionality
- Customization available
- Product longevity guarantee
- Expert technical support
- Lot tracking and revision locks
- Formal product change notifications
- Award-winning customer service

RSC #90 @ www.embedded-computing.com/rsc

Adtron Corporation

3710 E. University Dr., Suite 5
Phoenix, AZ 85034

I25FB

www.adtron.com

Shock, vibration, high altitude, extreme temperature, humidity, and dust particles destroy hard disk and tape drives. Adtron Flash disks, such as Adtron's 2.5" and 3.5" offerings, stand up to the demands of hostile defense environments while providing exceptional performance. Adtron accelerated life testing (based on MIL-HDBK-217F standards) at a 100 percent duty cycle demonstrates an extended life equivalent of 56 years and continuing without failure. Sophisticated defect management such as error detection and correction, sector sparing (similar to disk drives), and wear leveling extend the life of a Flash disk beyond that of magnetic media.

The I25FB and its sister IDE products incorporate Adtron's proprietary media controller, the foundation for "cacheless" technology and accelerated performance. Our new ATA controller permits enhanced emulation features, such as those required for tape functions. Adtron technology, coupled with industry standard interfaces (IDE and ATA) and Flash media, delivers unparalleled flexibility in tailoring data storage solutions to your application's unique needs. To see the complete line of Adtron SCSI and IDE Flash drives, visit our Web site at www.adtron.com or contact us at 602-735-0300.

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Visit www.adtron.com for more information.

FEATURES

- Capacities ranging from 64 Mbytes to 64 Gbytes of solid state Flash
- Transfer rates up to 33 Mbytes per second
- 2.5" and 3.5" form factors
- Interfaces include PIO, Multiword DMA, and UDMA
- Tested to MIL-STD-810F specifications
- Secure erase capabilities compliant with NISPOM DoD 5220.22-M, NSA/CSS, 130-2, AFSSI-5020, AR 380-19, and NAVSO P-5239-26
- Field upgradeable firmware prevents future obsolescence
- SCSI models also available

RSC #91 @ www.embedded-computing.com/rsc

Advantech Embedded Computing

15375 Barranca Parkway, Suite A-106
Irvine, CA 92618
Toll Free: 1-800-866-6008

ADVANTECH Embedded Computing

PCM-9580

www.advantech.com/epc

Advantech's PCM-9580 is a powerful 5.25" SBC aimed at fulfilling the needs of embedded applications requiring the highest multimedia and data processing performance. Utilizing an Intel Pentium 4 processor and Intel 845GV chipset, the PCM-9580 gives embedded developers the power to drive the most dynamic applications, perfect for high-end POS, gaming, and kiosk applications where performance is key. The PCM-9580 not only gives developers the Intel reputation and brand in their application, but also the assurance of a long product life cycle and strict revision control.

Providing support for Intel Socket 478 Celeron/ Pentium 4 processors up to 3.06 GHz and higher with FSB of 533 MHz/400 MHz and 256/512 Kbytes L2 cache, the Intel 845GV chipset delivers increased system responsiveness and performance by providing maximum bandwidth for I/O-intensive applications. Two 184-pin DIMM sockets support SDRAM DDR 200/266 for up to 2 Gbytes total memory, giving customers scalable performance options. The 845GV delivers ultimate graphics support with integrated Intel Extreme Graphics, delivering sharp 2D and 3D graphics, fast rendering, and with incredible detail. The 845GV architecture works perfectly with the Pentium 4 processor, enabling balanced memory usage between graphics and the system for optimal performance. With the 845GV and the onboard Chrontel CH7017 chip, the PCM-9580 provides a two-channel (2 x 24-bit) LVDS interface that supports 18/24/36/48 LVDS panels as well as TV-out (NTSC/PAL, S-video, and composite video).

FEATURES

- Socket 478 up to 3.06 GHz Intel Pentium 4
- Supports Gigabit Ethernet (PCM-9580FG)
- Supports embedded USB, 4 USB 2.0 ports
- Supports two-channel, 48-bit LVDS interface
- Optional audio interface

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For more information, visit www.advantech.com/epc.

RSC #92 @ www.embedded-computing.com/rsc

CG Mupac, Inc.

10 Mupac Dr.
Brockton, MA 02301
Tel.: 508-588-6110

CG MUPAC
A Carlo Gavazzi Group Company

714T Series 3/4 Size ATR Chassis

www.cgmupac.com

CG Mupac's 714T Series 3/4 Size ATR Chassis provides the highest available power supply wattage through its innovative heat spreader design to target your high performance military and transportation applications.

This 3/4 Size ATR chassis is designed to meet the requirements of the ARINC 404A/MIL-STD-91403. During the design process of this chassis, thermal simulation was employed to optimize the size and location of the heat spreaders, which are responsible for conducting heat away from the chassis' power supply and board area. To bring these simulated results into the real world, this all-aluminum chassis was dip brazed, which completely seals the enclosure and helps to quickly conduct heat away from the boards and power supply. Wedge lock guides not only secure the boards into the rack but also provide a thermally conductive path for removing heat generated by each board.

Up to 135 watts can be expected from the power supply while the chassis is in a 50°C ambient environment. The power supply plugs directly into the backplane to eliminate the need for power cabling to the backplane.

The internal rack infrastructure has been designed to support the popular DIN mechanical specification, which allows the 3/4 Size ATR Chassis to be fitted with VME, VME64X, and CompactPCI backplanes.

FEATURES

- 3/4-size, conduction-cooled ATR (Air Transport Rack) chassis
- Designed to meet the requirements of the ARINC 404A/MIL-STD-91403
- Accommodates VME, VME64X, and CompactPCI open architectures
- Unique backplane I/O breakout area and direct plug-in power supply provides a more rugged design by reducing the number of cables
- Innovative power supply heat sink allows for highest available wattage in this size and class of ATR chassis
- Custom backplane configurations are also available

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Visit www.cgmupac.com for more information.

RSC #93 @ www.embedded-computing.com/rsc

Condor Engineering, Inc.

101 W. Anapamu Street
Santa Barbara, CA 93101
Tel.: 805-965-8000 • Fax: 805-963-9630

Q-1553 Product Line

www.condoreng.com

Condor Engineering's new Q-1553 product family offers the highest level of performance and flexibility for MIL-STD-1553 Notice II applications. Available in PCI, PMC, VME, cPCI, PC/104 and PC/104-*Plus* formats, Condor's Q-1553 products provide up to four dual-redundant 1553 channels on a single board. All boards are available in a single-function and multi-function versions. Other standard features include 45-bit message time-tagging, triggers, error injection/detection, automatic/manual RT Status Bit, Mode Code responses, advanced BC functionality, IRIG B signal Receiver/Generator with GPS synchronization and on-board Test Bus and much more.

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For more information, e-mail sales@condoreng.com.

FEATURES

- 1Mbyte RAM per channel
- Abstract-level API for Windows XP, 2000, Me, NT, 98, 95, Linux, Solaris, LynxOS and VxWorks
- 1760 support
- Extensive I/O triggers and discretes
- Optional *BusTools*/1553 GUI analyzer

RSC #94 @ www.embedded-computing.com/rsc

Data Device Corporation

105 Wilbur Place
Bohemia, NY 11716

FC-75000 (Fibre Channel)

www.ddc-web.com

The FC-75000 FibreAccess™ series are dual redundant Fibre Channel Network Interface Controller (NIC) PMC cards optimized for use in military/aerospace applications. The FibreAccess NICs operate at either 1-Gbit/sec or 2-Gbit/sec data rates in point-to-point, arbitrated loop, or switched fabric topologies. Fibre Access cards are available with either electrical or optical interfaces on a conduction-cooled PMC form factor. Based on DDC's own Fibre Channel technology, FibreAccess's architecture is optimized to meet the highly deterministic performance, high reliability, and demanding environmental requirements of embedded, real-time, military applications. Its flexible FPGA-based architecture can be tailored to meet a wide range of specific system requirements. Moreover, FibreAccess is not subject to rapidly changing commercial market forces that can result in shortened life cycles.

DDC's FibreAccess technology has been designed to meet the multi-decade life cycle demands of military/aerospace programs, continuing DDC's demonstrated commitment as a long-term military COTS supplier of digital interface devices. FibreAccess NICs support Class 2 acknowledged and Class 3 unacknowledged Fibre Channel service. The cards provide leading edge performance, which includes capability to enable sustained data rates of more than 300 Mbytes/sec when operating at a 2-Gbit/sec data rate. DDC's FibreAccess NIC is suitable for a wide variety of applications for embedded avionics and vetronics systems. These include sensor interfacing, multiprocessor and DSP arrays, radar systems, display systems, serial backplanes, and storage.

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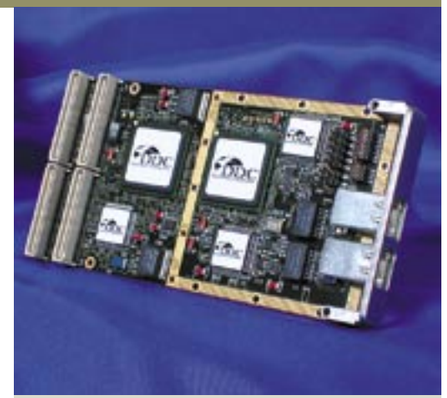
For more information, visit www.ddc-web.com.



FEATURES

- DDC-developed technology to support long life cycles
- Redundancy: Dual independent ports and autonomous failover
- Conduction-cooled PCI Mezzanine Card (PMC) providing extended temperature
- 1-Gbit/sec or 2-Gbit/sec operation
- Support for Class 2 and 3 service including broadcast and multicast
- 320 Mbytes/sec throughput with memory-to-memory latency under 100S
- Choice of transformer isolated electrical or fiber optic interface
- ASM, FC-AE-1553, TCP/IP, and UDP/IP support

RSC #95 @ www.embedded-computing.com/rsc

Delphi Engineering Group

485 East 17th St. Suite 400
Costa Mesa, CA 92627

1GHz PMC ADC Digitizer

www.delphieng.com

Delphi's 1GHz PMC ADC Digitizer is a PCI Mezzanine Card (PMC) analog-to-digital converter board with onboard digital filtering. It uses an 8-bit sampling A/D converter, sampling at a rate of up to 1 GHz. It is designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 1 GSPS. Buffering of the digitized data samples is provided onboard, as well as in phase and quadrature data processing. The onboard digital filter coefficients are downloaded from the host processor. The processed sample data is transferred to the processor card through the PCI bus for further host processing. This is an excellent acquisition module for RADAR and LIDAR applications hosted on quad-PowerPC processor boards.

The board's Xilinx Virtex II family of FPGAs implements processing, buffering, timing, and the PCI interface. FPGA design can be customized for specific applications, such as data preprocessing. It utilizes DSP functions, for example, FIR, IQ demodulation, and FFT. Processed sample data is transferred to the host system through the PCI bus. Data collection timing and duration are fully programmable through the PCI bus. PCI interfacing is implemented in an onboard FPGA. An analog single-ended input signal of 500mV peak to peak is accepted through an SMA female type connector on the front edge of the module. An analog single-ended clock input of +4dBm is provided through an SMA female type connector on the front edge of the module. The signal input is looped through to an output.

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For more information, visit www.delphieng.com.

FEATURES

- Analog input: Typical -3dB bandwidth of 1.0 GHz
- 1-GHz sampling rate
- Low Bit Error Rate (10-13) @ 1 GSPS
- Signal-to-noise ratio minimum 44dB
- Trigger jitter of 1/2 clock cycle
- Sample interval programmable from 5 to 8191 samples with 5nsecs resolution
- 64-bit, 66-MHz PCI 2.2 compliant bus

RSC #96 @ www.embedded-computing.com/rsc

Diversified Technology, Inc.

476 Highland Colony Parkway
Ridgeland, MS 39157

eTX-Lx05 Embedded Computer Module

www.dtims.com

The eTX-Lx05 embedded computer module, part of DTI's embedded product offering, features either an Intel Pentium III or Celeron low-power processor, the Intel 815E chipset, and up to 512 Mbytes PC100/133 SDRAM on a single 144-pin SODIMM socket. The integrated 2D/3D AGP4X video controller is enhanced with an 8-Mbyte display cache simultaneous LVDS, digital flat panel, and CRT output; the integrated AC'97 2.1 controller and CODEC provide excellent audio quality. The 10Base-T/100Base-TX Ethernet and Ultra ATA/100 EIDE controllers support fast data/file transfer. Four Universal Serial Bus (USB), two serial, and one shared, selectable parallel/floppy port round out the basic board.

The eTX-Lx05 AMI BIOS, in field upgradeable Flash, supports software Ethernet option ROM enable/disable, video override, serial/parallel port re-mapping/disable, keyboard disable, and console redirection. Other features include hardware monitor (input voltages, temperature), programmable two-stage watchdog timer, battery-backed real-time clock, power fail circuit, SMBIOS v2.3.1 and S.M.A.R.T. support.

DTI's eTX-Lx05 addresses embedded requirements for the medical, COTS military/defense, automotive, transportation, gaming, test and measurement, and Internet markets. The board combined with the FlexATA-compliant I/O baseboard supports time-to-market sensitive applications. The small thin form factor and the scalable performance configurations support both the PCI and ISA bus architectures.

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For more information, visit www.dtims.com.

FEATURES

- Single Intel low-power Pentium III or ULV Celeron processor to 933 MHz
- Intel 815E chipset with 100/133 MHz front-side bus
- Up to 512 Mbytes SDRAM/PC100/133, non-ECC memory
- AGP CRT, LCD, and TV-out video controller with 8 Mbytes SDRAM
- 10/100Base-Tx Ethernet
- Dual-channel Ultra ATA/100 EIDE
- AC'97 2.1 audio (OUT, IN, MIC)
- 4 × USB, 2 × serial, and 1 × parallel ports
- Supports four 32-bit/33-MHz PCI buses
- Hardware monitor, RTC, and two-stage watchdog timer
- ETX Specification 2.6 compliant
- 4.49" × 3.94" × 0.47"

RSC #97 @ www.embedded-computing.com/rsc

Dy 4 Systems

333 Palladium Drive
Kanata, Ontario K2V1A6 • Canada

SCP/DCP-122

www.dy4.com

Designed for space-constrained applications, the 122 offers the greatest processing power of any ruggedized 3U CompactPCI SBC on the market today. Based on the IBM 750FX processor, it runs at a clock speed of 800 MHz while executing an impressive 1856 Dhrystone Millions of Instructions Per Second (DMIPS). No other rugged COTS 3U CompactPCI SBC can match the raw processing power of the SCP/DCP-122.

The challenge of high density computing is to pack the greatest functionality into the smallest standard form factor possible while retaining as much flexibility as possible. In conjunction with its processing power, the SCP/DCP-122 meets this challenge by offering a full-speed onboard PMC site that allows developers to integrate Dy 4 or third-party PMCs directly onto the 122. A rich complement of I/O is also available on the 122 including Ethernet/Fast Ethernet, up to three serial channels (1 × RS-232, 2 × RS-422/485), up to 16-bit discrete digital I/O, and a Universal Serial Bus (USB) port.

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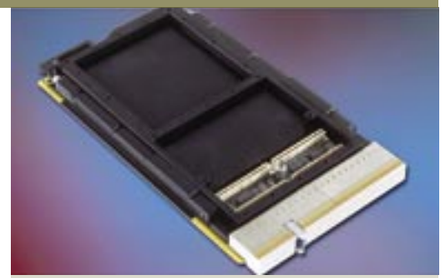
For more information, visit www.dy4.com.



FEATURES

- Based on the IBM PowerPC 750FX processor:
  - 800+ MHz
  - 100-MHz CPU bus speed
  - 512 Kbytes of Internal L2 cache running at core processor speed
- CompactPCI bus:
  - System controller and peripheral controller
  - Supports 3.3V or 5V signalling
  - 33 or 66-MHz operation
- 64-bit, 33/66-MHz PMC Expansion Site
- Memory
  - 128 Mbytes or 256 Mbytes of SDRAM with ECC at 100 MHz
  - 64 Mbytes non-volatile Flash
  - Flash for Permanent Alternate Boot Site (PABS)
  - 32 Kbytes non-volatile RAM
- I/O
  - 1 x 10/100Base-T Ethernet port
  - 1 x RS-232 serial port
  - 2 x HDLC/SDLC-capable EIA 422/485 serial channels (2 asynchronous or 1 synchronous)
  - 1 x USB
  - 8 x general-purpose DMA controllers
  - Up to 16 bits discrete I/O
- Comprehensive foundation firmware
- VxWorks and INTEGRITY support
- Available in commercial and rugged air-cooled, and rugged extended temperature conduction-cooled versions

Dy 4 Systems

333 Palladium Drive
Kanata, Ontario K2V1A6 • Canada

SVME/DMV-182 Dual PowerPC

www.dy4.com

Using dual, 1.3-GHz Motorola MPC7457 PowerPC processors with Altivec technology and 1 Gbyte of state-of-the-art DDR SDRAM, the 182 represents the new functionality and performance benchmark for rugged SBCs. With two 64-bit PMC sites, one which supports 133 MHz PCI-X and an unparalleled complement of I/O capability such as dual Ethernet, six serial ports, and two USB ports, the 182 will satisfy the most demanding requirements of embedded computing applications.

Available in the full Dy 4 range of environmental build grades, the 182 is targeted to the sophisticated data processing needs of tactical aircraft, armored vehicles, and many harsh environment naval systems. A future enhancement of the 182 will be the provision of a unique user-programmable feature that provides the user with the capability to tailor or develop customized hardware implementations on the base card. This feature will be available as an optional FPGA-based IPM.

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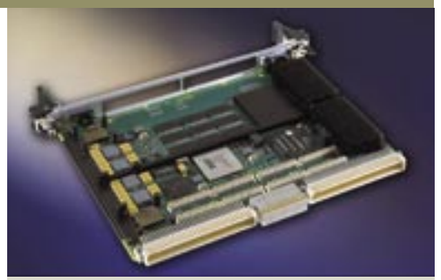
For more information, visit www.dy4.com.



FEATURES

- Single or dual 1.3-GHz 7457 PowerPC processors, each with:
  - 64 Kbytes L1 cache
  - 256 Kbytes internal L2 cache
- 2 Mbytes external L3 cache per processor
- 512 Mbytes or 1 Gbyte of DDR SDRAM with ECC
- 64 or 128 Mbytes of contiguous direct-mapped Flash memory
  - Hardware write protection provided
  - Permanent Alternate Boot System (PABS) provides back-up boot capability
- 32 Kbytes AutoStore nvSRAM
- One 10/100/1000Base-T Gigabit Ethernet port
- One 10/100Base-T Ethernet port
- Two 64-bit, 66-MHz PMC sites on independent PCI buses
  - One 133-MHz PCI-X capable, one 66-MHz capable
  - Optimized cooling of conduction-cooled PMCs
- Controlled impedance I/O routing for Fibre Channel, digital video, and other high-speed interfaces
- VxWorks, INTEGRITY & TimeSys Linux Support

GE Fanuc

12090 South Memorial Parkway
Huntsville, AL 35803

Embedded Systems

PowerPC VME SBC (VMIVME-7050)

www.gefanuc.com

The VMIVME-7050 is the flagship of GE Fanuc's PowerPC-based SBCs. Highly integrated and versatile, the single slot SBC provides increased performance at an energy efficient level for demanding embedded computing requirements.

Utilizing the IBM 750FX/GX PowerPC processor with 512 Kbytes of on-chip L2 cache and processor speeds up to 1.0 GHz, the VMIVME-7050 delivers extreme high performance. The VMIVME-7050 features two serial ports (up to 10 Mbytes/sec per channel), supports dual Gigabit Ethernet LANS, and provides up to 64.5 Mbytes of Flash. Onboard memory is provided by up to 2 Gbytes of DDR SDRAM with ECC running at 133 MHz, and PC2100 without losing any PMC expansion capabilities. The powerful IBM processor is mated with the industry's most powerful system controller (Marvell Discovery II) to yield one of the most impressive designs on the market.

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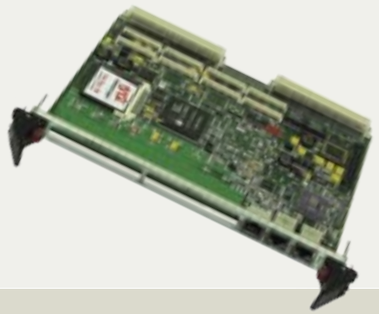
For more information, visit www.gefanuc.com/embedded.



FEATURES

- IBM 750FX/GX PowerPC processor (733 MHz to 1.0 GHz)
- Marvell MV64360 system controller with 2 Mbytes integrated SRAM
- Dual 64-bit PCI-X on PMC expansion sites (backward compatible) with support for double-wide PMC card
- Up to 2 Gbytes of DDR SDRAM with ECC
- 512 Kbytes of on-chip L2 cache
- 64.5 Mbytes total bootable Flash (64 Mbytes soldered down, 512 Kbytes in PLCC32 socket)
- Ultra-DMA IDE controller to CompactFlash Socket (Type 1)
- 32K NVRAM
- Two high performance 16550-compatible serial ports
- Dual 10/100/1000Base-T Ethernet
- Full 64-pin PMC I/O support for both PMC sites through VMEbus P0 & P2
- Operating system support available for VxWorks and Linux

RSC #100 @ www.embedded-computing.com/rsc

General Standards Corporation

3208 Whitesburg Drive SW
Huntsville, AL 35802
Tel.: 1-800-653-9970 • Fax: 256-880-8788

General Standards Corporation
High Performance Bus Interface Solutions

PMC-12AISS804

www.generalstandards.com

The 12-bit PMC-12AISS8AO4 analog I/O board samples and digitizes eight input channels simultaneously at rates up to 2.0 Msamples/sec for each channel. The resulting 12-bit sampled data is available to the PCI bus through a 64-Ksample FIFO buffer. All data is channel-tagged. The analog inputs can be sampled in groups of one through eight channels, and the sample clock can be generated either from an internal rate generator, through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are software-selectable as ±10V, ±1V or ±100mV. The inputs can be divided into two channel groups, each of which can be assigned an input range and clocking rate independently of the other. Four analog output channels provide software-selected output ranges of ±2.5V, ±5V, or ±10V and are accessed directly through dedicated control registers. A 16-bit bidirectional digital port can be configured as two independent byte-wide ports.

An on-demand auto-calibration feature determines offset and gain correction values for each input and output channel, and the corrections are applied subsequently during normal operation. A self-test switching network routes output channels or calibration reference signals to the analog inputs and permits board integrity to be verified by the host. This board is available on all form factors, including PCI, CPCI, VME, and PC/104-*Plus*. See our Web site for more details.

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E-mail: sales@generalstandards.com for more information.

FEATURES

- Eight differential analog inputs with dedicated 12-bit, 2.0 Msamples/sec ADC per channel
- True simultaneous sampling of all inputs; minimum data skew
- Sampling rates to 2.0 Msamples/sec per channel (16 Msamples/sec aggregate rate)
- DMA engine supports both block-mode and demand-mode analog data transfers
- Four analog output channels with direct register access
- Sampling controlled by internal rate generator, by software trigger, or externally
- On-demand internal auto-calibration
- Hardware sync I/O for multi-board operation
- Integral dual-conversion precision analog power supplies
- Completely software-configurable; no field jumpers
- Conforms to PCI Local Bus Specification, Revision 2.3, with universal signaling
- Single-width PMC form factor, with integral EMI shield

RSC #101 @ www.embedded-computing.com/rsc

General Standards Corporation

3208 Whitesburg Drive SW
Huntsville, AL 35802
Tel.: 1-800-653-9970 • Fax: 256-880-8788

General Standards Corporation
High Performance Bus Interface Solutions

PMC-16HSDI

www.generalstandards.com

The six-channel PMC-16HSDI analog input board provides high-density precision 16-bit analog input resources in a single-width PMC form factor. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements to the analysis of complex audio signals and waveforms. Each of the six sigma-delta analog input channels can be controlled by either of two independent sample clocks, and multiple channels can be harmonically locked together. Internal auto calibration networks permit periodic calibration to be performed without removing the board from the system.

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus. Each of the six input channels contains an input buffer, an adaptive digital-image filter, and a dedicated sigma-delta A/D converter. The inputs can be configured for either differential or single-ended operation, or an internal voltage reference can be applied to all channels to support self-test operations and auto calibration. Gain and offset trimming of the input channels is performed by calibration DACs that are loaded with channel correction values during auto calibration. The use of calibration DACs eliminates the missing codes that occur when analog input channels are calibrated exclusively in the digital domain. Multiple channels can be synchronized to perform synchronous sampling, either by a software command, or by external hardware sync and clock input signals. This board is available on all form factors, including PCI, CPCI, VME, and PC/104-*Plus*. See our Web site for more details.

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E-mail: sales@generalstandards.com for more information.

FEATURES

- Sima delta conversion; no external antialiasing filters required
- High effective sampling rate; 16-32 times the effective rate of successive approximation
- Converters operate at the same conversion rate
- Integral antialiasing input filters reject out-of-band interference components
- Software-selectable ranges: ±1.25V, ±2.5V, ±5V or ±10V
- Six, 16-bit analog input channels; dedicated sigma-delta converter per channel
- Sample rates adjustable up to 1,100 Ksamples/sec per channel
- Two independent sample-rate generators; adjustable with 0.2 percent resolution
- Low noise; typically less than 0.4mVRMS RTI
- 64 Ksamples FIFO buffer. All data is channel-tagged
- VxWorks and WinNT drivers are available

MCC Systems, Inc.

113 McHenry Rd, #239
Buffalo Grove, IL 60089

Consulting

www.mccengineering.com

MCC Systems, Inc. is in a unique position to provide its customers with a variety of consulting and engineering services from on-site debugging to full systems engineering. Areas of expertise include:

Linux development
Linux BSP development
Software Development Kits (SDKs)
Linux device drivers
Linux training
Linux support
Bid and proposal writing
Project management
Systems engineering
Custom software development
Systems integration
VxWorks® BSP development
Tornado® integration
VxWorks device drivers
Windows® development with C# and C++
.NET® development
Visual C++® development

Microprocessor expertise includes: PPC8260, PPC860, PPC405, x86, MIPS, ARM, i960, Hitachi SH, 68K, and Coldfire.

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For more information, visit www.mccengineering.com.

FEATURES

- TimeSys Linux
- ELDK Linux
- MontaVista Linux.
- Eclipse-based Java
- Eclipse-based C and C++
- INTEGRITY
- VxWorks & Tornado
- Board support /SDK
- Device drivers
- Proven track record
- C#, Java, ADA
- More than 30 years experience

MCC Systems, Inc.

113 McHenry Rd, #239
Buffalo Grove, IL 60089

Training

www.mccengineering.com

Today's embedded systems developer needs every advantage they can get in producing world-class software and systems on schedule and within tight budget constraints. Appropriate training is the key to improved time-to-productivity and more able personnel. MCC Systems provides the broadest selection of embedded systems courseware in the industry, delivered by some of the best instructors in the industry. Course list includes:

Linux Development
- Developing for Embedded Linux
- Developing Linux Device Drivers
- Developing Linux BSPs and SDKs
- Transitioning VxWorks Applications
- Transitioning OSE Applications

Green Hills Development
- Using the MULTI IDE
- Introduction to the INTEGRITY OS
- INTEGRITY and the MULTI IDE
- INTEGRITY BSP Development

Embedded Systems
- Real-Time Operating Systems
- Graphics for Embedded Systems
- Usability for Embedded Systems
- Robust Software for Embedded Systems

VxWorks Development
- VxWorks 5.x and Tornado 2.x
- VxWorks BSP Development

Software Design Technologies
- UML for Embedded Development
- Real-Time Software Design with UML
- Structured Systems Design Techniques
- Fundamentals of Software Development

Programming Languages
- C, C++, EC++, C# .NET, Java, Ada

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For more information, visit www.mccengineering.com.

FEATURES

- Embedded Linux
- Linux device drivers
- Linux board support transitioning
- INTEGRITY OS
- MULTI IDE
- VxWorks & Tornado
- Time-to-productivity
- Decrease support costs
- C, C++
- C#, Java
- ADA

EMBEDDED INDUSTRY PRODUCT REVIEW

MILITARY

MCC Systems, Inc.
113 McHenry Rd, #239
Buffalo Grove, IL 60089

TRT for LINUX

www.mccengineering.com

TRT for Linux offers a new and unique way of monitoring operational Linux systems. With TRT for Linux, the user can monitor multiple different Linux systems using the same Eclipse-based user interface with multiple points of access!

The interactive Linux Remote Shell (LRS) capability provides user-level access to running Linux target system via a TCP/IP link. The integrated scripting engine is perfect for creating test scripts while you develop your application code. The Linux System Monitor (LSM) capability provides 22 distinct points of system usage information. TRT also provides 11 points of per-process information via the Linux Process Monitor (LPM). Use these points of information to monitor your application process while it is running. Monitoring multiple processes is as simple as launching multiple LPMs.

Who can use this product? Application developers can use this product to monitor their Linux application processes from a remote location with minimal intrusion into the system. System test managers can use it to create system test procedures and documentation. System integrators can use this product to transition the product to manufacturing. In addition, system testers can use it to perform system test and maintenance of multiple systems. Finally, manufacturing engineers can use this product for final system test of multiple systems.

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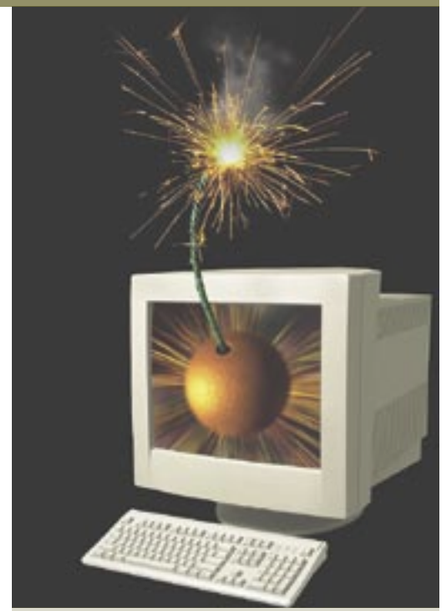
For more information, visit www.mccengineering.com.



FEATURES

- Monitor via LSM
- Resource usage
- Access multiple systems
- Simultaneous debug
- Multiple user access
- Advanced scripting
- Non-intrusive debug
- Linux remote shell
- Time-based logging
- Shell activity
- Linux process monitor
- Time-sensitive problems

SBS Technologies, Inc.

2400 Louisiana Blvd.
Albuquerque, NM 87110

AMC-cPCI-3000

www.sbs.com

The AMC-cPCI-3000 is an advanced 3U CompactPCI, ruggedized computing platform for flight management/mission computing, display processing, and information management applications. This flight qualified COTS computer system is suited for a variety of avionics, vetronics, navtronics, and space programs where time to market is critical.

This computer can meet the general-purpose, I/O, video, and graphics processing needs for a variety of military applications. It has been tested, qualified, and flown in some of the most extreme environmental conditions. Because of its reconfigurability and robust design, the AMC-cPCI-3000 computer offers customers a reliable, cost-effective, high-performance solution that meets mission critical reliability requirements.

This system was built on open systems architecture to allow for technology insertion. It leverages SBS' COTS products, conforms to open standards, and utilizes RTOS operating system software. The AMC-cPCI-3000 comes configured with an off-the-shelf power supply, a ruggedized 3U CompactPCI PowerPC-based RL4 or CM4 SBC running up to 500 MHz, and includes Fast Ethernet, four serial ports, parallel I/O, Build In Test (BIT), VxWorks, or Green Hills Integrity operating system support.

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For more information, visit www.sbs.com.

FEATURES

- Lightweight – less than 9 pounds (4.08 kg)
- Modified COTS RCOM03 conduction-cooled chassis
- 3u CompactPCI SBC
- 1553-PMC2-CC module
- High-speed serial module
- Digital I/O module
- CompactPCI transition module
- 3.5" (H) x 10.75" (W) x 12.8" (L)
- A ruggedized, 3U CompactPCI SBC

RSC #106 @ www.embedded-computing.com/rsc

SBS Technologies, Inc.

2400 Louisiana Blvd.
Albuquerque, NM 87110

FC22A-CCPMC-1C

www.sbs.com

The conduction cooled FC22A-CCPMC-1C has rugged features for enhanced immunity from harsh environmental conditions. The 1-Gbit/sec, 64-bit/66-MHz Fibre Channel PMC provides highly sustained throughput and the low latency required for demanding real-time and storage applications. This product includes optimized device drivers for Windows NT, Windows 2000/XP, VxWorks, Linux, and LynxOS. It supports one copper interface, offers rear I/O, and has a military style rugged connector for the Fibre Channel interface.

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For more information, visit www.sbs.com.

FEATURES

- 64-bit/66-MHz PMC
- 102.7 Mbytes/sec, half-duplex sustained
- Multiple initiator-capable copper interface support
- SCSI target, SCSI initiator
- RemoteDMA and IP protocol
- Conduction cooling
- Extended operating temperature
- AirBorn connector for Fibre Channel interface
- Rear I/O
- Unique high-bandwidth and low-latency firmware and software running on industry standard QLogic Fibre Channel 2200 controller chips

RSC #107 @ www.embedded-computing.com/rsc

SBS Technologies, Inc.

2400 Louisiana Blvd.
Albuquerque, NM 87110

VG5

www.sbs.com

SBS Technologies recently introduced the latest in its family of high-performance 6U VMEbus SBCs, the VG5. Configured with dual processors, the VG delivers the speed and bandwidth needed for performance-oriented applications such as real-time control, post video processing, and signal processing subsystems.

The VG5 comes with a choice of one or two integrated 800-1300 MHz Motorola MPC7455/57 PowerPC processors featuring AltiVec technology. The design permits two computing platforms with independent operating systems to work in parallel within one slot. Each processor has its own memory and chipset so one processor node can accomplish number-crunching DSP tasks while the other works as a general-purpose CPU and facilitates I/O functions for the board. In summary, the VG5 can handle the workload of two boards.

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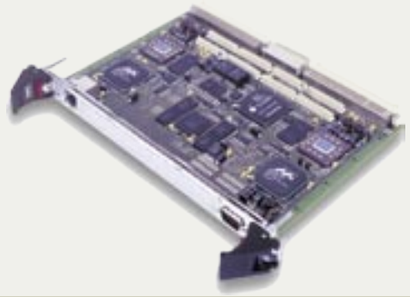
For more information, visit www.sbs.com.



FEATURES

- MPC7455/57 PowerPC™ processors with AltiVec™ technology and 2/4 Mbytes L3 cache
- Asymmetrical Multiprocessor Architecture (ASMP)
- Integrated Gigabit Ethernet and Fast Ethernet ports
- Two PMC slots
- Commercial and conduction cooled versions
- Support for the Ready Driver™ program assuring easy integration of additional SBS I/O modules
- The VG5 packs two complete processor subsystems on a single board
- Assures out-of-the-box interoperability
- Up to 1 Gbyte DDR SDRAM with ECC, and a Marvell MV64360 chipset
- Configurations support three independent onboard 64-bit PCI buses
- User-programmable FPGA for customized rear I/O
- Software support available for VxWorks, Greenhills, and LynxOS operating systems

RSC #108 @ www.embedded-computing.com/rsc

Targa Systems

2081 Merivale Road, #200
Ottawa, Ontario K2G1G9 • Canada

VME25 Flash Disk

www.targasystems.com

Targa's solid-state 6U VME Flash Disk has been designed specifically to replace hard disk drives in rugged aerospace and military environments. The 6U VME board is available in a single-slot board (up to 30 Gbytes) and in a dual slot configuration, with capacities up to 90 Gbytes. Both convection-cooled and conduction-cooled units are available. The VME25 Flash Disk design meets demanding military standards and is suitable for a wide range of airborne and ground applications. The VME25 is available in Fast and Ultra SCSI, as well as ATA and I/O memory-mapped interfaces. A version is also available in the CompactPCI 3U and 6U form factors.

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For more information, visit www.targasystems.com.

FEATURES

- No moving parts
- Conduction-cooled
- Convection-cooled
- Capacities up to 90 Gbytes
- MTBF 500,000 hours
- Fast access times
- Low power consumption
- Write protect
- High-speed erase
- All solid state

RSC #109 @ www.embedded-computing.com/rsc

Thales Computers

3100 Spring Forest Road
Raleigh, NC 27616

PowerEngine7 SBCs

www.thalescomputers.com

Thales Computers' PowerEngine7 delivers higher performance and lower power consumption than any other board on the market. Employing the PowerPC 750FX processor results in 50 percent more performance with 25 percent less power consumption than competing boards, making it ideal for demanding military and severe environment applications. The PowerEngine7 features single or dual PowerPC 750FX processors, operating at 733 MHz, providing extremely high performance at more than 1600 Dhrystone 2.1 MIPS, while drawing a very low 14 watts of power for the entire board. The new SBC includes up to 512 Mbytes of SDRAM and up to 128 Mbytes of Flash memory. A 133 MHz Avignon host bridge system controller is optimized for use with the PowerPC processor. The ALMA2e PCI/VME bus bridge provides for 2eSST transfers. Other features include twin PMC slots (one PCI 64 @ 66 MHz, one PCI 32 @ 33 MHz), two 10/100 Base-T Ethernet interfaces, as well as four asynchronous and two synchronous/asynchronous serial lines. A bridgeless PMC-Carrier is available to expand the PCI 64-bit bus on the P0 and increase the number of slots to as many as four. Available in convection- and conduction-cooled models.

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For more information, visit www.thalescomputers.com.

FEATURES

- Single or dual PowerPC 750FX processors, operating at 733 MHz, up to GHZ
- 50 percent more performance with 25 percent less power consumption
- Up to 512 Mbytes of SDRAM
- Up to 128 Mbytes of Flash memory
- 133 MHz Avignon host bridge system controller
- ALMA2e PCI/VMEbus bridge for 2eSST transfers
- Twin PMC slots
- Two 10/100 Base-T Ethernet interfaces
- Four asynchronous and two synchronous/ asynchronous serial lines
- Convection- and conduction-cooled versions

RSC #110 @ www.embedded-computing.com/rsc

Themis Computer

3185 Laurelview Court
Fremont, CA 94538
Tel.: 510-252-0870 • Fax: 510-490-5529

USPIIe-USB™

www.themis.com

Themis Computer's new USPIIe-USB is a family of high-performance VMEbus computer boards based on Sun® Microsystems' most advanced 64-bit embedded SPARC superscalar processors. The USPIIe-USB provides users with a 650-MHz UltraSPARC™ RISC processing performance and Solaris 8 and Solaris 9 compatibility.

The USPIIe-USB is available in one-slot, two-slot, and three-slot configurations. The affordable USPIIe-USB/1 single-slot model features a compact 6U form factor, low power dissipation, and flexibility for embedded computing applications. The USPIIe-USB/2P2 model facilitates I/O expansion in a two-VME slot configuration. The USPIIe-USB/2P3 is a doublewide configuration providing users three additional PMC slots without the expansion features of the USPIIe-USB/2P2 configuration. The USPIIe-USB provides excellent graphics support with Themis' optional TGA3D+ graphics adapter.

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For more information, contact info@themis.com.

FEATURES

- 6U VME64 engine with 64-bit 650-MHz UltraSPARC IIi processor
- 512 Kbytes of L2 cache memory
- High performance Tundra 64x Tundra VME64 interface
- 128 Mbytes to 4 Gbytes SDRAM memory
- Three USB 1.0 ports (two on front panel, one at rear of board)
- Up to four PMC (3.3/5V) expansion slots: one on baseboard, up to three additional PMC slots on optional I/O expansion boards
- Up to two Fast Ethernet ports, one on baseboard, one on optional USPIIe-USB/2P2
- Two 80-Mbytes/sec Ultra2 LVD SCSI ports
- Injectors – both VME64 and traditional VME injectors are available
- Optional TGA3D+ provides 3-D graphics support – up to 8.5 million triangles per second and up to 160 million textured pixels per second tri-linear fill rate
- 64-bit Solaris™ 8 and Solaris 9 OS support

RSC #111 @ www.embedded-computing.com/rsc

Themis Computer

3185 Laurelview Court
Fremont, CA 94538
Tel.: 510-252-0870 • Fax: 510-490-5529

USPIIIi™

www.themis.com

The USPIIIi from Themis Computer is a new high-performance family of single- and dual-processor SPARC®-based VMEbus computers for military, telecommunications, and embedded processing applications. Featuring a new system architecture with 1.28 GHz UltraSPARC IIIi processors, dual 160-Mbyte/sec ultra-SCSI ports, and dual fibre-channel ports, the USPIIIi is designed to provide users the industry's best data bandwidth, two-way scalability, and server class I/O.

The USPIIIi is a next generation computer ideal for demanding new applications or as an upgraded replacement of earlier USP-2 SMP VME products. The USPIIIi leverages Themis' USPIIe-USB™ product family, and can be configured with either one or two UltraSPARC IIIi CPUs. The single-processor configuration consists of an I/O board and a CPU board assembly occupying two VME slots. A dual-processor configuration occupies three VME slots. Each USPIIIi CPU has a local SMP readable 4-Gbyte memory, both processors of a dual-processor configuration that can access up to 8 Gbytes of memory.

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For more information, contact info@themis.com.

FEATURES

- 1.28 GHz UltraSPARC with 1Mbyte L2 cache
- 4-Gbyte, 266 DDR SDRAM memory per CPU, 8 Gbytes total
- Memory bandwidth – 4.2 Gbytes/sec (peak), 3.3 Gbytes/sec (sustained)
- Dual Ultra 160 LVD SCSI ports
- Optional TGA3D+ graphics – incorporates Sun XVR-500 graphics technologies
- Gigabit Ethernet port
- One 64-bit/66-MHz PMC slot
- Up to three PMC expansion slots (up to five slots with optional TGA3D+ graphics)
- Dual FC-AL ports
- Universe II 64x VME interface
- Solaris™ operating environment support for superior scalability
- Rugged design for reliability in harsh operating environments – up to 30 Gbytes shock

RSC #112 @ www.embedded-computing.com/rsc

VersaLogic Corp.

3888 Stewart Rd
Eugene, OR 97402
1-800-824-3163

Jaguar PC/104-*Plus* for homeland security

www.VersaLogic.com

Why do military contractors buy their COTS computers from VersaLogic? The design engineers at a number of major defense contractors have been impressed with VersaLogic's outstanding technical support, off-the-shelf availability, high reliability, and long-term availability. Fast and accurate responses to questions allowed them to complete their project in less time. Design reliability ensures reduced field failure and cost savings. Long-term availability means less frequent product redesign.

The Jaguar PC/104-*Plus* CPU module from VersaLogic is a favorite of defense contractors and systems integrators because of its small size and powerful processing capabilities. They also like the fact that it is available in low-power fanless and extended temperature versions (–40ºC to +85ºC degrees). The long list of features includes an 850 MHz Pentium III processor, Fast Ethernet, AGP video and flat panel support, TVS devices for ESD control, and PC/104 and PC/104-*Plus* expandability that make this board a winner for almost any mission-critical embedded system.

VersaLogic's product line includes a full range of PC/104, PC/104-*Plus,* EBX, and STD32 SBCs with processors and features for any size application. What's more, the support you'll get with your VersaLogic embedded computer rates among the best in the industry. In the last two years, according to the VDC embedded industry reports, VersaLogic has received five platinum vendor awards for customer service.

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For more information visit www.VersaLogic.com/COTSproducts/.

FEATURES

- Pentium III/Celeron processors from 350 to 850 MHz
- Extended temperature and low-power fanless options
- Fast Ethernet
- Up to 256 Mbytes RAM
- AGP video/flat panel support
- TVS devices for ESD protection
- Two high-density latching I/O connectors
- CD-ROM boot capability
- CPU temperature sensor
- High reliability design and construction
- Field upgradable BIOS with OEM enhancements
- Customizing available

RSC #113 @ www.embedded-computing.com/rsc

Advantech Embedded Computing

15375 Barranca Parkway, Suite A-106
Ivine, CA 92618
Toll Free: 1-800-866-6008

ADVANTECH Embedded Computing

PCM-3370

www.advantech.com/epc

Advantech's newly released PCM-3370 is a powerful PC/104-*Plus* SBC that brings a new performance standard to the PC/104-*Plus* SBC form factor community. With an onboard Intel ULV Celeron 400/650 fanless CPU or LV Pentium III 800/933 processor (optional), along with a VIA VT8606/TwisterT + VT82C686B system chipset, the PCM-3370 is one of the most capable size/power CPU boards on the market. With onboard PC/104 and PC/104-*Plus* I/O expansion, features can be quickly added using off-the-shelf modules, giving developers a fanless, high performing, and scalable platform with good graphics performance that can fit into the tightest spaces. The PCM-3370 is perfect for applications, such as medical DVRs, transportation, and industrial automation, where uncompromised SBC performance in a limited space, high reliability, and long product availability are needed.

The PCM-3370 provides as many features as CPU boards several times its size. The PCM-3370's internal 4x AGP VIA VT8606T chipset ensures excellent graphics performance and provides VGA/LCD support up to 1024 × 768. SDRAM memory up to 512 Mbytes is supported as is one CompactFlash (Type I) card. Two USB 1.1 compliant ports are available as is one LPT and two COM ports (RS-232 and RS-232/422/485). Watchdog timer support and Fast Ethernet is provided as well. Numerous standard PCI and ISA add-on cards are available utilizing the PC/104 and PC/104-*Plus* sockets. This helps speed development time and reduces costs.

For more information, visit www.advantech.com/epc.

FEATURES

- Intel Celeron 400/650 ULV fanless, Pentium III 800/933 LV (optional)
- Chipset: VIA VT8606/TwisterT and VT82C686B
- VGA/LCD controller with optimized Shared Memory Architecture (SMA)
- 4x AGP VGA/LCD & LCD controller up to 1024 x 768
- Supports +5V and +12V power
- Fast Ethernet PCI interface, supports wake-on-LAN
- COM2 (5V) supports power line connected on pin 9
- PC/104 and PC/104-*Plus* expansion connector
- Socket for CompactFlash Card (CFC) Type I supported
- 1.6-second interval watchdog timer
- 1 SODIMM socket supports up to 512 Mbytes SDRAM

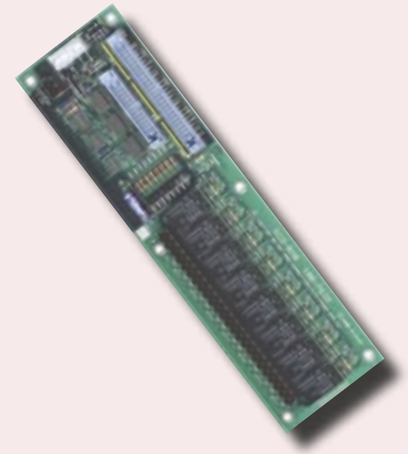
SCIDYNE

649 School Street
Pembroke, MA 02359-3649
Tel.: 781-293-3059 • Fax: 781-293-4034

SCIDYNE®

XIO-RO8 External I/O Eight-Channel Relay Output Board

www.scidyne.com



The XIO-RO8 accepts up to three 8-bit TTL/CMOS digital ports and uses one of the ports to control eight isolated SPDT (Form C) relay outputs. Dual IDC input headers directly support the two most common pinout arrangements for digital I/O ports. Other pinouts can be accommodated with custom cable assemblies. Input resistors serve to keep the XIO-RO8 outputs in a known state in the event the host loses power or becomes disconnected. The remaining two non-selected ports are unaffected and can be used with other circuitry, including additional XIO-RO8 boards. Each bit of the selected port controls a corresponding relay output. Depending on whether the XIO-RO8 is configured for "non-inverted" or "inverted" operation, a relay is activated by its control bit being logic "1" or logic "0" respectively. A status LED on each channel illuminates whenever its relay is energized. By taking advantage of the buffering circuitry and bussed interconnection nature, a special feature can be realized that allows multiple boards to be simultaneously driven by the same digital port. This effectively creates another relay "pole" for each XIO-RO8 added. Independent access to each relay's normally-closed, normally-open, and common contacts eases wiring constraints and permits flexible mixing of AC and DC signals.

For more information, visit www.scidyne.com.

FEATURES

- Converts a low-power 8-bit digital port to eight 10A/250V SPDT relay outputs
- Removable screw terminals accept 12-24 AWG field wiring
- LED status indicators show board's operation at a glance
- +5V-only power requirement can be supplied by host or externally
- Works with products from SCIDYNE and other manufacturers
- Conveniently mounts using 3" SNAPTRACK®, standoffs or on DIN rail
- DIP switch configuration

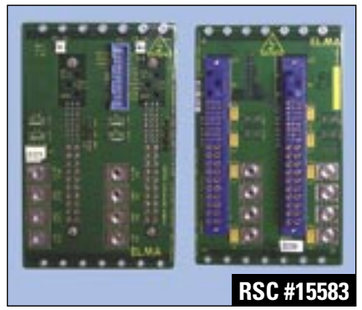
By Eli Shapiro

TABLE OF CONTENTS

BACKPLANE: ACCESSORIES

Bustronic Corporation

Web site: www.bustronic.com
Model: Power Interface Boards **RSC No:** 15583
A line of power interface boards (PIBs) • 3U version has two 47-pin connectors for hot-pluggable power supplies meeting the PICMG 2.11 specification • Power taps for +5V, 3.3V, and GND and fast-ons for +12V and -12V • Allows users to choose between standard power interfaces and pluggable modules on Bustronic backplanes • The PIB interfaces to the backplane via power bugs with 6/32 screws and includes mounting holes to be securely fixed to the chassis • Header for voltage sense and IPMB interface • Auxiliary disk/drive connector • Power switch header • Sense lines help the power supply better regulate the power at the load end • Current-share lines allow multiple power supplies to share current, either on one PIB or between multiple PIBs • Geographical addressing on the power supply connector is selectable



CHIPS & CORES: DSP

Analog Devices, Inc.

Web site: www.analog.com/dsp
Model: ADSP-TS201S **RSC No:** 15835
A TigerSHARC DSP processor • Static superscalar architecture that supports 1, 8, 16, and 32-bit fixed point processing • High-performance, 600-MHz, 1.67 nsecs instruction rate DSP core • 24 Mbits on-chip embedded DRAM internally organized in six banks with user-defined partitioning • 14-Channel, zero-overhead DMA controller • Enhanced communications instruction set for wireless infrastructure applications allows for the TigerSHARC to offer complete baseband processing • Four internal 128-bit wide internal buses providing a total memory bandwidth of 38.4 Gbytes/sec • Software radio approach allows for the adoption of a single platform for multiple wireless telecommunication standards • Single Instruction Multiple-Data (SIMD) operation supported by two computation blocks each with an ALU, multiplier, shifter, and 32-word register file • Assembly and C language programmability

Model: Blackfin Processors **RSC No:** 15836
A series of DSP processors • Performance to 600 MHz/1,200 MMACs enables multichannel audio plus VGA/D1 video processing in multimedia applications • Enhanced dynamic power management with on-chip voltage regulation allows operation to 0.7V, extending battery life in portable applications • Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications • Multiple low-cost, pin- and code-compatible derivatives enable software differentiation in cost sensitive consumer applications • Up to 148 Kbytes of on-chip SRAM • 32 Kbytes of on-chip, user definable ROM (ADSP-BF531 and ADSP-BF532 only) • Parallel peripheral interface supports ITU-R 656 video data formats • Two dual-channel, full-duplex synchronous serial ports support eight stereo I2S channels • 12 DMA channels support one- and two-dimensional data transfers • Memory controller provides glueless connection to multiple banks of external SDRAM, SRAM, Flash, or ROM • Three timer/counters support Pulse Width Modes (PWM) and event count modes • UART with support for IrDA • SPI compatible port • Real-time clock • Watchdog timer • PLL capable of 1x to 63x frequency multiplication • 160-lead (12mm x 12mm) Mini-BGA and 176-lead (24mm x 24mm) LQFP packages • Industrial temperature range

COMPONENT-LEVEL MODULES

Fairchild Semiconductor

Web site: www.fairchildsemi.com
Model: QFET **RSC No:** 15536
Planar MOSFETs for applications including power supplies, power factor correction, DC/DC converters, plasma display panels, lighting ballasts, and motion control • Offers reduced on-state loss by lowering on-resistance and reduced switching loss by lowering gate charge and output capacitance • Available in standard surface-mount and through-hole type packages

Linear Technology Corporation

Web site: www.linear-tech.com
Model: LTC2433-1 **RSC No:** 15556
A low-noise, low-cost, analog-to-digital converter • 16-bit resolution with input signals down to ±50mV • 1.25LSB (max) INL • 1.45µV noise • Less than 0.02LSB transition noise • 10-pin MSOP package • No status or configuration registers • On-chip oscillator • Automatic, transparent offset/full-scale calibration • Simultaneous 50-Hz/60-Hz notch frequency filter • 87dB rejection of line frequencies • VREF can span 0.1V to VCC • Low supply current: 100µA during conversion and 4µA during shutdown • 2.7V to 5.5V supply range

CONNECTOR: OTHER

Yamaichi Elect

Web site: www.yeu.com
Model: Mini SD Connectors **RSC No:** 15852
A line of connectors and adapters for Mini Secure Digital (SD) applications • Low profile design • Can be used in a wide variety of mobile phones and PDA handheld devices • Dual-point contact to prevent chattering in the event the host device is dropped • Card/connector keying to prevent incorrect insertion • SDIO ground tab grounds out ESD and EMI directly to the metal shell, resulting in higher contact reliability from Mini SD and SD card pads • Available for both top-mount and reverse type applications

DATA ACQUISITION

Interactive Circuits & Systems Ltd. (ICS)

Web site: www.ics-ltd.com
Model: ICS-710 **RSC No:** 15588
A 32-channel, CompactPCI data acquisition board • 32 differential input channels • Onboard programmable antialiasing filter and gain • 24-bit Sigma-Delta ADCs • Simultaneous sampling rates of up to 216 KHz/channel • Signal-to-noise ratio of more than 85 dB • FPDP II, 400-Mbyte/sec front-panel interface • 64-bit/66-MHz CompactPCI PICMG 2.0 R3.0 hot-swap interface • Up to 32 ICS-710 boards can be operated synchronously to ensure simultaneous sampling of more than 1024 channels

National Instruments

Web site: www.ni.com
Model: PXI-4220 **RSC No:** 15822
A PXI data acquisition board for high-speed strain measurements • Two strain gauge inputs at 200 Ksamples/sec, 16-bit resolution • Programmable excitation (0 V-10V) per channel • Programmable gain (1 to 1000) per channel • Programmable 4-pole Butterworth filter (10 Hz, 100 Hz, 1 KHz, 10 KHz) per channel • Quarter, half, and full-bridge completion • Differential simultaneous sampling inputs • Dual 9-pin D-Sub connectors (one per channel) • Two shunt calibration circuits per channel • Remote sensing • NI-DAQ driver simplifies configuration and measurements • Compatible operating systems: Windows 2000/NT/XP • Includes NI-DAQ 7 driver software

DATA COM: ATM

RadiSys Corporation

Web site: www.radisys.com
Model: ENP-3504 **RSC No:** 15844
A dual OC-3C/STM-1 ATM-to-IP RNC gateway line test and monitoring card • Intel 200-MHz IXP1240 network processor • UTOPIA-to-Packet bridge • Eight 10/100Base-T Ethernet ports on the IX bus with I/O on an RTM • Optional four 10/100Base-T Ethernet ports on the IX bus out the front • Dual OC-3c optical interface • Up to 128 Mbytes of SDRAM, up to 8 Mbytes SSRAM, and up to 8 Mbytes of Flash memory • Single-slot, 64-bit, 6U CompactPCI form factor • Hot standby capability • Capable of remote software updates • PICMG 2.16 compliant • PICMG 2.9 compliant • CompactPCI hot-swap compliant • RTM for carrier class rear I/O • Front I/O for all front access • Full onboard diagnostic suite • Boot menu selection for various operating systems, bearer-plane applications • AAL2: Voice and data (I.366.1 protocol) traffic routed on microengines • AAL5: (I.363.5) reassemble and transmission • IP layer 3 forwarding between four 10/100Base-T Ethernet and OC-3c ATM (RFC 1577) • Ethernet encapsulation of data • First release with Linux • VxWorks 5.5 board support package • Development tools • Supports the Intel IXA SDK 2.01

DEVELOPMENT PLATFORM

Analog Devices, Inc.

Web site: www.analog.com/dsp
Model: Blackfin for SoftFone **RSC No:** 15834
A complete hardware and software system that enables rapid development of EGPRS terminal devices, including cellular phones, PC card form-factor wireless data cards, multimedia smartphones, and wireless-enabled PDAs • High-performance Blackfin processor core • ARM control processor • Extended peripheral interfaces for multimedia applications • Othello EGPRS direct-conversion radio • EGPRS software package from TTPCom

Arcom Control Systems, Inc.

Web site: www.arcomcontrols.com
Model: VIPER Linux Development Kit **RSC No:** 15573
A ready-to-run embedded Linux development kit to support the VIPER, XScale-based PC/104 processor • Includes a pre-installed operating system image • Based on the 2.4 Linux kernel and includes read/write and read-only support for the onboard Flash memory using the compressed Journaling Flash File System (JFFS2) • Integrated support for the PXA255 graphics controller and drivers for many of the onboard peripherals • Power management support • Includes a standard installation of OpenSSH • Includes a 400-MHz VIPER SBC fitted with 64 Mbytes of DRAM, 16 Mbytes of Flash, VIPER ICE (Industrial Compact Enclosure), the VIPER-UPS (uninterruptable power supply), serial and Ethernet cable set, an optional Q-VGA color display and touchscreen, and a quickstart manual

ENCLOSURE + CARD RACK + POWER SUPPLY

Arcom Control Systems, Inc.

Web site: www.arcomcontrols.com
Model: OLYMPUS ICE **RSC No:** 15255
A rugged, industrial, compact enclosure for the EBX format Socket 370 OLYMPUS SBC • Fully tested and approved for CE/FCC EMC compliance and safety tested to EN60950 • Available as a fanless system using a large passive heatsink (40°C maximum operating temperature with an 866-MHz Pentium III) or with forced air cooling for more demanding environments (50°C maximum operating temperature) • Manufactured in lightweight aluminum • Designed for wall or panel-mounted installations • Includes all standard cable assemblies, a 60W universal AC input power supply, and sufficient space to accept two PC/104 I/O modules

FABRICS: PICMG 2.16 ETHERNET

ELMA Electronic, Inc.

Web site: www.elma.com
Model: cPSB Chassis Solutions **RSC No:** 15570
A line of 6-slot and 8-slot, PICMG 2.16 compliant, compact packet switching backplane (cPSB) chassis solutions • 8-slot versions have one or two fabric slots and the rest as node slots • Available with dual star topology for redundancy • Available with connections for the H.110 bus • The 6-slot version has one fabric slot and five node slots • All backplanes offer one slot that is convertible to a system slot via a CPU enable pin • The 4U horizontal chassis has a card rack and is EMC shielded to meet NEBS II/III, UL, CE, and FCC requirements • Side-to-side airflow optimized for card, device, and PSU requirements


RSC #15570

FPGA

Alpha Data

Web site: www.alpha-data.co.uk
Model: ADM-XRC-II/II Pro **RSC No:** 15745
A set of Xilinx Virtex-ii and Virtex-II Pro based FPGA processor PMCs • Support for the largest Xilinx devices from 2V1000 to 2V10000 and 2VP4 and 2VP50 • Up to six banks of 512K x 36-bit ZBT SRAM • 384 Mbytes of DDR SDRAM • 16 Mbytes of Flash • PCI bandwidth up to 528 Mbytes/sec • High-performance bus mastering PCI interface with twin DMA • Flexible front and rear panel I/O interface options, with bandwidth up to 5 Gbytes/sec • Support for Xilinx PAVE, System Generator, and ChipScope • Programmable clock generators • Drivers for Windows NT/2000/XP, VxWorks, and Linux; VxWorks BSP for Virtex-II Pro • Template designs included in Verilog/VHDL

I/O: ANALOG

Meilhaus Electronic GmbH

Web site: www.meilhaus.com
Model: ME-1600 **RSC No:** 15594
A 12-bit, CompactPCI, analog output board • Depending on model 4, 8, 12, or 16 analog outputs for voltage • A version is available with 16 analog outputs for voltage, eight of which can also be used as current outputs • Software programmable output ranges • Output range of the voltage channels is 0V to 10V or ±10V; the range for the current outputs is 0 or 4mA to 20mA • Current outputs are short-circuit-proof and readjusting • Depending on the board version and number of channels, there are one, two, three, or four 12-bit D/A converters • Driver support software for Windows 98/ME/NT/2000/XP, Linux, VxWorks, and QNX


RSC #15594

I/O: MULTIFUNCTION

Thales Computers

Web site: www.thalescomputers.com
Model: PMC-DAADIO **RSC No:** 11215
A multifunction I/O PMC • Analog inputs: Eight output and 16 single-ended or eight differential input channels • Analog outputs: Eight single-ended or four differential outputs • Digital I/O: 18 TTL I/O lines • DSP-to-PMC host interface with dual port RAM and a 32-bit, 33-MHz PCI • 64-bit counter input • 64-bit timer output with 40-bit resolution • Support for VxWorks • Air or conduction-cooled versions

IEEE 1394 (FIREWIRE)

Mindready Solutions, Inc.

Web site: www.mindready.com
Model: SedNet OHCI Board Family **RSC No:** 15612
A family of IEEE-1394 a and b OHCI boards • Fully compliant with the OHCI v1.0 specification • Available in popular PCI-based formats such as PCI, CompactPCI, PMC, and PC/104-*Plus* • Provides either IEEE-1394a (up to 400 Mbits/sec) or IEEE-1394b (up to 800 Mbits/sec) bus support • PCI host and external power feed option • Extensive protection through either galvanic isolation or with a transformer isolation option • Choice of electrical and optical interfaces, supporting various bit rates • Fully tested for compatibility with Mindreadyís SedNet 1394 stack and high-level protocol software suite • Able to power external devices via the 1394 cable • Full real-time synchronization between all attached devices

INTEGRATED DEVELOPMENT ENVIRONMENT

VenturCom, Inc.

Web site: www.vci.com
Model: Phar Lap ETS **RSC No:** 15999
A complete embedded development environment for Intel's 32-bit x86 processors • Features a Windows-friendly RTOS, the Real-Time ETS Kernel, built to meet the requirements of industrial-strength embedded applications • Supports deterministic, multi-threaded embedded applications, including reliable priority inversion avoidance • Fixed-priority and round-robin scheduling with variable time slices • Robust networking capabilities, including a built-in TCP/IP stack, WinSock 1.1 libraries, and Ethernet and serial network drivers • SNMP agent library, including SNMP MIB-II network information • Microsoft Win32 serial API library • Microsoft WinInet FTP client API library • Dynamic Link Libraries (DLLs) • MS-DOS-compatible file system with support for FAT12, FAT16, and FAT32 formats, as well as a wide variety of disk types including IDE (both CHS and LBA formats), floppy, PC Card ATA (both Flash and rotating media), M-Systems Flash and RAM disk • Real-Time GUI, including video, mouse, and keyboard drivers • Floating-point emulation library • Drivers for PC Card ATA disks, Ethernet adapters, serial ports, and modems • Support for the Microsoft C/C++ runtime libraries and a subset of the Win32 API • LinkLoc, a 32-bit linker/locator • Includes the Visual System Builder, a Windows program for configuring the Real-Time ETS Kernel and applications

MASS STORAGE: PLUG-IN UNIT

Asine Ltd.

Web site: www.asinegroup.com
Model: AscPCI620 **RSC No:** 15551
A 6U, SCSI, fast Flash disk CompactPCI board • Interfaces via LVD or single-ended SCSI bus utilizing SCSI-1/2 or SCSI-3 protocols • 0.5 Gbytes to 14 Gbytes of nonvolatile Flash memory • Less than 20µsecs access time • Sustained write rates at 30 Mbytes/sec and 20 Mbytes/sec • Fast erase; 10 seconds for entire media • Embedded EDC/ECC, based on 48-bit Reed Solomon algorithm • Built-in power-up self test • Manual and automatic self diagnostics • TrueFFS bad block mapping-out algorithms • Dynamic wear leveling • 3.5W max power dissipation • Available in three operating temperature ranges • Uses existing Windows and VxWorks SCSI drivers • MIL-STD-810F compliant

MEZZANINE: PMC

Interactive Circuits & Systems Ltd. (ICS)

Web site: www.ics-ltd.com
Model: ICS-572 **RSC No:** 15742
A 2-channel, 105-MHz ADC and 2-channel, 200-MHz DAC PMC module with up to an 8-million-gate onboard Xilinx FPGA • 64 Mbytes ofSDRAM • Over 16 Mbytes of SRAM • Pn4 user I/O connector • PCI 64-bit/66-MHz DMA interface

MEZZANINE: PrPMC

Prodrive B.V.

Web site: www.prodrive.nl
Model: P3G4508 **RSC No:** 15743
A low-cost G4 PowerPC PMC processor module • Motorola MPC741 processor at up to 500 MHz with MPX processor bus up to 133 MHz • Up to 2 Mbytes of L2 cache • Up to 256 Mbytes of SDRAM • Up to 32 Mbytes of Flash • 32/64-bit 33/66-MHz PCI 2.2 interface • Three full-duplex 10/100Base-T Ethernet interfaces • Two full-duplex RS-232 serial interfaces • JTAG interface • Supports Linux and VxWorks

RadiSys Corporation

Web site: www.radisys.com
Model: EXS-6424 **RSC No:** 15845
Processor PMC with two Intel XScale processors • Single or dual 533-MHz IXC1100 XScale processors, each with up to 256 Mbytes of 133-MHz SDRAM memory • 10/100Base-T Ethernet port with front panel connectivity and status LEDs • 10/100BaseT Ethernet port with PN4 connectivity • Status LED • Watchdog timer • 32-bit,33/66-MHz PCI bus interface • Automatic sense and configuration for monarch and non-monarch modes • Reset switch • Supports VxWorks operating system

MIL-STD-1553

Condor Engineering

Web site: www.condoreng.com
Model: CORE-1553 **RSC No:** 12140
A MIL-STD-1553 hardware/software IP design • Enables users to insert MIL-STD-1553 functionality into PLDs/FPGAs • Conforms to MIL-STD-1553B Notice II and can support 1553A and MACAIR devices • BC, RT, and BM functionality available • When connected to an external transceiver, provides all 1553 protocol decoding/encoding, message processing, time stamping, and message buffering

PROCESSOR: CELERON

Acrosser Technology Co., Ltd.

Web site: www.acrosser.com
Model: AR-B1661 **RSC No:** 15831
A 5.25" embedded PC • Onboard Intel Ultra Low Power BGA2 Celeron processor at 400-850 MHz • Intel 440MX chipset • One DIMM socket supports up to 256 Mbytes of SDRAM memory • Supports DiskOnChip • Two 10/100Base-T Ethernet interfaces • Onboard audio output • Supports VGA CRT/LCD, TV-out display, and dual view display • Compact size: 203mm x 146mm (8" x 5.75")

PROCESSOR: GEODE

Parvus Corporation

Web site: www.parvus.com
Model: SpacePC 4320 **RSC No:** 15599
A PC/104 SBC • Geode Processor • PC/104 form factor • PC/104 and PC/104-*Plus* expansion connectors • DiskOnChip and CompactFlash interfaces • Ethernet, IDE, RS-232, and LPT interfaces • Real-time clock and watchdog timer • Extended temperature range • Low power consumption • Supports ROM-DOS, QNX, Windows 9x/NT/CE, VxWorks, and Linux

NEW PRODUCTS NEW NEW NEW
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PROCESSOR: OTHER

Motorola Computer Group

Web site: www.motorola.com
Model: 56F8300 Controller Series **RSC No:** 15851
A 16-bit hybrid embedded controller • Up to 60 MIPS at 60 MHz execution frequency • DSP and MCU functionality in a unified, C-efficient architecture • JTAG/EOnCE for unobtrusive, real-time debugging • Four 36-bit accumulators • 16 and 32-bit bi-directional barrel shifter • Parallel instruction set with unique addressing modes • Hardware DO and REP loops available • Three internal address buses • Four internal data buses • Architectural support for 8, 16 and 32-bit single-cycle data fetches • MCU-style software stack support • Controller-style addressing modes and instructions • Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)

Renesas Technology America, Inc.

Web site: www.renesas.com
Model: R8C/Tiny **RSC No:** 15847
A line of 16-bit Flash microcontrollers • Powerful 16-bit R8C CPU core • High clock speeds deliver high throughput: Up to 20 MHz for R8C/11 MCUs, up to 16 MHz for R8C/10 devices • CPU runs M16C instruction set with 89 instructions, allowing reuse of code developed for other M16C MCUs for shorter system development cycles • 64 Kbytes of memory address space is sufficient for low-end systems • Choice of Flash sizes (8, 12, or 16 Kbytes) for cost-effective matching of memory size to application • Two X 2-Kbyte blocks of Flash memory (in addition to program Flash) can be used as virtual EEPROM (data Flash) • Fast write speed for convenience and performance (75 µsecs/byte) • Allows onboard, in-circuit programming for easy code downloads in production and system upgrades in the field via serial port • Single-voltage programming simplifies system design • Flash memory protect function provides higher reliability • 32-pin, 7mm x 7mm LQFP package

PROCESSOR: PENTIUM

Acrosser Technology Co., Ltd.

Web site: www.acrosser.com
Model: AR-B1790 **RSC No:** 15830
Pentium 4 Embedded ATX board • Supports Pentium 4 processors up to 2.8 GHz (400-MHz and 533-MHz front-side bus) • Supports CRT/2x LVDS/TV-out function • Onboard two-channel AC97 audio with 3W amplifier • Six USB 2.0 ports and four serial ports • Supports CompactFlash + Type II • Mini PCI interface • Onboard 10/100Base-T Ethernet function • Dimensions: 244mm x 244mm (9.6" x 9.6")

NEW PRODUCTS

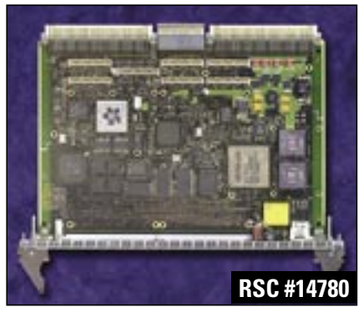
American Megatrends

Web site: www.ami.com
Model: Olympus III Series **RSC No:** 15828
An Intel 875P or Canterwood chipset-based motherboard • Single Pentium and Prescott/Northwood PGA 478 Socket • 533/800 MHz front-side bus • Five 32-bit/33-MHz PCI slots • One AGP 8x slot • Onboard video • Onboard LAN • Two USB 2.0 ports • Dual serial ATA connectors • Dual parallel IDE ATA-100 connectors • PS/2 mouse • Standard ATX form factor

PROCESSOR: Power PC

Thales Computers

Web site: www.thalescomputers.com
Model: PowerEngine7 Series **RSC No:** 14780
A series of PowerPC SBCs • Uses single or dual IBM 750FX processors operating at 733 MHz to 1 GHz • Draws only 14W of power for the entire board • Up to 512 Mbytes of SDRAM • Up to 128 Mbytes of Flash memory • Host bridge system controller operates at 133 MHz • Twin PMC slots: One PCI 64 at 66 MHz, and one PCI 32 at 33 MHz • Two 10/100Base-T Ethernet interfaces • Four asynchronous and two synchronous/asynchronous serial lines


RSC #14780

Model: VxG4a **RSC No:** 7911
A quad 400 MHz PowerPC 7400 (G4) computer board • Four asynchronous RS-232 serial channels • Up to 512 Mbytes of onboard global memory • 2 Mbytes of cache memory per processor • 512 Kbytes and 1 Mbyte of system Flash memory • Up to 32 Mbytes of user Flash • Optimized double bank memory management • Two PMC mezzanine sites • Crossbar by host-bridge • DMA Engines • Operating system support includes LynxOS and VxWorks

PROTOTYPING & DEBUGGING AIDS

Lynux Works, Inc.

Prototyping & Debugging Aids
Web site: www.lynuxworks.com
Model: SpyKer Pro v2.0 **RSC No:** 15840
A dynamically instrumented system trace analyzer • Auto-instrumented tracing; no lengthy application instrumentation cycles or kernel rebooting necessary • Fast, automated, and transparent collection of timing information • Accelerated development and debugging: Easy, anytime visibility into program execution • Accurate, actionable, performance-tuning information • SpyKer trace patch overhead is exceedingly low • Easy to-comprehend GUI with multiple, concurrent windows • The front end can reside locally or remotely from the system to be measured • Traces extensive list of system events: System calls, interrupts, context switches, processor exceptions, etc. • Dynamic tracing of user applications • SpyKer patches dynamically linked libraries • CPU time use, context switches, and processor exceptions are graphically depicted • Event histogram tool displays time spent in ISRs or between any two event points and allows for fast isolation of timing areas in question • Selective tracing allows selection of events to trace, minimizing impact on a target system

RADAR/SONAR

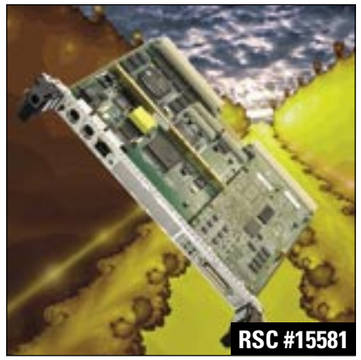
Interactive Circuits & Systems Ltd. (ICS)

Web site: www.ics-ltd.com
Model: ICS-725 **RSC No:** 15589
A 32-channel, 24-bit, 288-KHz/channel, Delta-Sigma DAC board • Requires no post-filtering • Provides differential outputs with high-current drives • Standard product comes with 4 Mbytes/sec of swing buffer memory (option to expand capacity to 16 Mbytes) • FPDP II interface • 64-bit/66-MHz CompactPCI PICMG 2.0 R3.0 hot-swap

interface • Operates in continuous, one shot, and loop mode

Primagraphics

Web site: www.primag.co.uk
Model: Radar Video Distribution Server **RSC No:** 15581
A radar video distribution server in PCI, CompactPCI, and VME form factors • Cost-effective solution for the distribution of radar video from a sensor to multiple display consoles • Uses standard COTS



Ethernet networks and proprietary digital compression technology to distribute video from a radar source to any number of display stations • Provides flexibility in the choice of where and when radar video is displayed • Interfaces with different radar types, including ACP/ARP, RADDS, ASDE-3, and specialized serial and parallel formats • Video from radar interfaces is digitized and compressed with Primagraphics' RACE radar codes • Available in a range of form factors and configurations, ranging from a 4U rack-mountable, industrial-grade, PCI-based enclosure to a single-slot VME or CompactPCI card

REFERENCE SYSTEM

Analog Devices, Inc.

Web site: www.analog.com/dsp
Model: Blackfin Car Telematics Platform **RSC No:** 15833
A reference design for a low-cost telematics solution • Navigation functions: GPS location management and dead reckoning • Speech processing functions: Speech recognition, text to speech, and noise and echo cancellation through single or multiple microphones • Audio processing functions: FM/MPX decoding, MP3 decoding, block decoding of CD drive/Flash card data, MP3 encoding, multiband stereo equalization, and fading, mixing, and volume control • Communication functions: Physical connectivity to mobile phone module for emergency services, Bluetooth connectivity to local mobile devices, and connectivity to optional host processor

ROUTERS/SWITCHES

GNP

Web site: www.gnp.com
Model: 3U cPSB 8+2 Ethernet Switch **RSC No:** 15563
A 3U, single-slot, CompactPCI Ethernet switch • Provides eight 10/100Base-T Fast Ethernet ports and two 10/100/1000Base-T Ethernet ports in a fully non-blocking switching configuration • CompactPCI packet switching backplane compliant • Two 3U cPSB 8+2 Ethernet switches provide redundant switching fabrics while occupying one 6U CompactPCI slot • Console-based management interface • VLAN and QoS support • Link aggregation and port mirroring support

NEW PRODUCTS

SOFTWARE: APPLICATION

Eternal Systems, Inc.

Web site: www.eternal-systems.com
Model: Eternal Duration **RSC No:** 15853
A high-availability software solution for applications that require the benchmark 5-nines (99.999 percent) or greater service availability • Stateful application failover ensures that the working data and processing state is preserved when an application switches over to a new machine or node • Automated check-pointing engine links in underneath the application and is configured to take periodic snapshots of the processing context and critical operating system state associated with the application • Set of facilities for heartbeats, virtual addressing, alarm processing, event notification, and policy configuration wraps around the core engine to ensure that applications continue to offer service under failure conditions • Applications can be protected by inserting as little as one line of code

VenturCom, Inc.

Web site: www.vci.com
Model: ReadyOn Solution **RSC No:** 16000
Software that allows instant on/off switching of a computer system • Resumes from hibernation state each time the device starts up • Takes a snapshot of the memory state of a device or system upon initialization in a hiberfil.sys file • Bypasses the hibernation reset flag and does not need to suspend and recreate the hibernation file each time • Can be turned off without a shutdown process • Write filter is applied across the boot partition to prevent changes • Supports Microsoft Windows XP Embedded/XP Professional/2003

SOFTWARE: DEVELOPMENT TOOL

Altium Limited

Web site: www.altium.com
Model: Tasking C166 Toolset **RSC No:** 15848
A fully integrated embedded development environment for the C166 microcontroller family from Infineon Technologies • Language sensitive editor • Highly optimized C++/EC++/C compilers • MISRA C enhanced code checking • CrossView Pro debugger • Kernel aware debugging • Extensive RTOS, ICE, and evaluation board support • DAvE 2 compatibility • Available for PC/Windows, PC/Linux, Sun/Solaris, and HP/UX

Green Hills Software, Inc.

Web site: www.ghs.com
Model: SuperTrace Probe **RSC No:** 15855
A hardware trace probe that allows high-speed software trace collection to processors with embedded trace ports • Combines a high-speed trace engine available with 1 Gbyte of trace memory • Provides both a means of controlling the processorís trace logic and a channel for capturing trace data while the processor is running • Includes all the run-control features of the original Green Hills Probe • Compatible with the PowerPC 405, PowerPC 440, ARM7 Embedded Trace Macrocell (ETM), ARM9 ETM (multi-core and single-core), and ARM10 ETM • Capable of expanding to handle ColdFire processor families as well as Nexus-compatible devices • Works with all ETM modes • One gigabyte trace buffer that can capture several hundred million processor cycles of execution and data trace works closely with Green Hills' MULTI integrated development environment • Trace data is uploaded from the SuperTrace Probe to MULTI's host system through a USB or 10/100Base-T connection • Triggers and trace conditions are configured and set from MULTI, allowing developers to correlate their trace settings to source code • Complicated trigger conditions can be graphically configured with state transition diagrams

Kozio, Inc.

Web site: www.kozio.com
Model: kDiagnostics **RSC No:** 15843
Diagnostic software for embedded designs using Intel XScale processors • Diagnostics include comprehensive functional and performance tests for the processor, memory, buses, peripherals, and other components • XScale processor tests include: Processor exception handling, interrupt tests, instruction and data cache control, MMU setup, core processor register access and coprocessor register access, memory controller tests, peripheral bus tests, timer configuration, DMA controller tests, and CPU reset • PCI/PCI-X tests include: PCI device discovery, including all downstream buses, primitives for generating PCI configuration type 0 and configuration type 1 cycles, performance measurement of data transfers across PCI bus, and PCI compliance tests • RAM tests: Data bus bit tests, address bus bit tests, memory cell tests (verifies that all bits in a memory device can be set and cleared), and random access tests

SOFTWARE: NETWORKING

VenturCom, Inc.

Web site: www.vci.com
Model: BXP for Education **RSC No:** 15996
A high-performance diskless boot and centralized desktop management solution for Windows • Diskless network boot with centralized management of student desktops • Centralized server facilitates desktop maintenance of software installations, system reconfiguration, and license management • Efficient reconfiguration of entire classrooms of desktop systems • Chubby Client desktops allow full access to rich multimedia and simulated learning applications without sacrificing performance • Multiple PC boot modes • Supports Microsoft Windows XP Embedded/XP Professional/2000/2003 • Hardware requirements: Standard PXE BIOS v1.0 or equivalent BootROM, client system that runs Windows 2000 (Server or Professional), XP (Home, Professional, or Embedded), or Windows 2003, any Network Interface Card (NIC) with drivers for Windows 2000, XP, or 2003, and a Windows 2000, XP, or 2003 host to run boot services and BXP services

Model: BXP Secure **RSC No:** 15998
A diskless boot and image management solution for Windows • Unique image management and deployment solution that fills security gap for desktop computing and delivers reduced total cost of ownership • Increases data security by eliminating local persistent storage and strict client and server authentication • Maximum encryption protection provided by 192-bit 3DES and IPsec encryption • Eliminates compromised data concerns due to hardware theft and reduces hardware costs with diskless computing devices • Adheres to NNSA security requirements of US Department of Energy and Department of Defense • Maintains high performance through complete local processing and application support • Supports Microsoft Windows XP Embedded/XP Professional/2000/2003 • Hardware requirements: Standard PXE BIOS v1.0 or equivalent BootROM, client system that runs Windows 2000 (Server or Professional), XP (Home, Professional, or Embedded), or Windows 2003, any Network Interface Card (NIC) with drivers for Windows 2000, XP, or 2003, and a Windows 2000, XP, or 2003 host to run boot services and BXP services

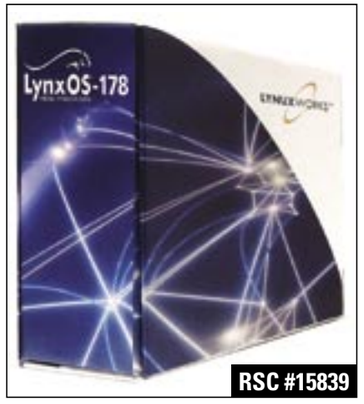
SOFTWARE: OPERATING SYSTEM

Green Hills Software, Inc.

Web site: www.ghs.com
Model: Integrity **RSC No:** 15347
A secure, royalty-free, real-time operating system intended for use in embedded systems that require maximum reliability • Fast, deterministic, real-time response • Protected address spaces • Guaranteed resource availability • Distributed multiprocessor support • Dynamic task download • Field upgrade and debug • POSIX API • Comprehensive communications protocols • Powerful development tools • Optimizing C/C++/EC++/Ada95 compilers • Execution profiling • Advanced debugging capabilities • Real-time event analyzer • Runtime error checking • Kernel object access control • Processor support includes: PowerPC, PowerQUICC III, MIPS, ARM, and XScale • Available with a variety of board-support packages • Available with extensive support for networking, embedded internet, and telecommunications protocols

LynuxWorks, Inc.

Web site: www.lynuxworks.com
Model: LynxOS-178 **RSC No:** 15839
A certifiable RTOS for safety-critical computing • DO-178B and EUROCAE/ED-12B certifiable, POSIX-conformant RTOS solution • COTS package • Designed to be tightly integrated with the LynxOS Certifiable Stack (LCS) • The LynxOS-178 product family includes: A suite of standards-based development tools, full customer support including DO-178B capable consulting services, and an artifacts package for the OS with DO-178B required documentation



NEW NEW NEW NEW PRODUCTS
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VenturCom, Inc.

Web site: www.vci.com
Model: RTX **RSC No:** 16001
Real-time extension software that allows Windows XP/XP Embedded/2000/NT/NT Embedded to function as a general-purpose operating system and a high-performance, high availability (99.999) operating system, at the same time on the same computer • Guaranteed task scheduling and performance • APIs for direct hardware access • Exception (bluescreen) handling • Windows XP, 2000, and NT API portability • Uniprocessor and multiprocessor support • Application and kernel-level debugging • Applications can start seconds into the boot cycle for extended control

SOFTWARE: PROTOCOL STACK

Green Hills Software, Inc.

Web site: www.ghs.com
Model: IPNET and IPLITE **RSC No:** 15854
Two dual-mode IPv4/v6 Internet Protocol stacks for the INTEGRITY RTOS • Provides backward compatibility with current IPv4 requirements while overcoming 32-bit address limitations and security shortcomings • IPNET provides complete IPv4 and IPv6 networking solutions, supporting multiple network interfaces, NAT, PPP, built-in routing table support, and built-in advanced IP Security (IPSec) • IPLITE provides a small and compact dual IPv4/v6 protocol stack configurable from 17 Kbytes of memory for embedded systems requiring a small footprint • IPSec is optionally available for IPLITE • Both stack offerings have additional network applications available, such as Telnet, FTP, TFTP, DNS, and DHCP, along with L2TP, LDAPc, NAT, PPPoE, RIPv2, SNTP, Web server, and SNMP • Additional security protocols, including Radius, Firewall, SSH, SSL, and IKE are also available • Both IPNET and IPLITE are fully compatible with existing Internet standards

LynuxWorks, Inc.

Web site: www.lynuxworks.com
Model: LCS **RSC No:** 15838
A standalone, certifiable TCP/IP stack for safety-critical systems • Certifiable to DO-178B level A • Standards-based code enhanced for determinism and safety-critical operation • COTS solution offers standalone stack operations on a Motorola 8260 processor to offload the sporadic nature of TCP/IP processing from host-based resources • Full IPv4 protocol stack • 100 percent modified condition decision coverage (MCDC) structural coverage for safety and security critical code verification • Supports security with pre-configuration of allowable IP addresses, ports and sockets allowed, and individual rate limits on a per-socket basis • Applications interface library with LynxOS-178B RTOS

SYSTEM INTEGRATION SERVICES

TeamF1, Inc.

Web site: www.teamf1.com
Model: Products/Services **RSC No:** 15837
Embedded software products and services enable customers to build differentiated, higher performance, smaller footprint embedded systems with lower development costs and faster time to revenue • Designed for hardware acceleration on embedded platforms like VxWorks, pSOS, QNX, and Embedded Linux, TeamF1's pre-ported products enable secure management of telecom/datacom and industrial equipment, and provide the infrastructure components needed for switching and wireless products in various market segments • Products include components for Security (firewall, SSH, SSL, IPSec), authentication (Kerberos, RADIUS), IP-networking (TCP/IP v4/v6, NAT, CBQ/WFQ), and layer 2 and wireless services (802.1x, LACP, STP)

SYSTEM MONITORING

Acrosser Technology Co., Ltd.

Web site: www.acrosser.com
Model: AR-B1662L4 **RSC No:** 15832
A fanless Internet security embedded PC • Supports fanless Eden processors at up to 667 MHz • Onboard four 10/100Base-T interfaces • Two WAN, one LAN, and one DMZ interface • One SO-DIMM socket supports up to 512 Mbytes of memory • Supports CompactFlash • Two COM ports and two USB ports • Mini PCI interface • Expansion PCI bus • Built-in LAN status LED indicators • Compact size: 203mm x 146mm (8" x 5.75")

TELECOM: T1

N.A.T. GmbH

Web site: www.nateurope.com
Model: NPMC-8266-OC3 **RSC No:** 15723
A high-performance telecommunications PMC module • Motorola MPC8266 processor at 166 to 300 MHz, with on-chip PCI bridge • 32 to 256 Mbytes of SDRAM • 16 or 32 Mbytes of Flash PROM • Four primary-rate E1/T1/J1 lines on standard RJ-45 connectors at front panel • PC3 SDH/STM1 optical fiber on standard connector at front panel • OKI CT812 H.110 on PMC P14 connector • Supports VxWorks and Linux

TURNKEY SYSTEM: TELECOM

RadiSys Corporation

Web site: www.radisys.com
Model: SYS50 **RSC No:** 15846
A PICMG 2.16 compliant 9U Platform • High availability design • Redundant 24-link port, Fast Ethernet, Layer 2 switches with built-in platform management software • Intelligent platform management: Fault notification and prediction, user configurable alarm thresholds, SNMP management interface to hardware platform, and remote resetting and power cycling • Intel 1.2 GHz Pentium III Processor-M • 512 Mbytes SDRAM with ECC • SVGA video controller (via PMC) • Ultra-2 SCSI controller (via PMC and PIM) • Choice of two media modules: IDE includes a 20-Gbyte IDE hard disk drive and a 32x CD-ROM drive; SCSI includes two 18-Gbyte hard disk drives • Hot swappable fan tray with fault indication and audible alarm • Hot swappable, load sharing DC or AC power supplies with N+1 capability • MontaVista Carrier Grade Linux 3.0 comes pre-installed; other operating systems are available upon request

WIRELESS

Atmel Corporation

Web site: www.atmel.com
Model: ATA5811/12 **RSC No:** 15842
An RF remote control ASK/FSK transceiver • Designed for automotive and other mobile Remote Keyless Entry (RKE) and Passive Entry Go (PEG) systems • Extremely low current consumption and small size • The ATA5811 is designed for 433-435 MHz and 868-870 MHz, whereas the ATA5812 operates at 314-316 MHz • Both transceivers are pin-identical and functionally identical • Current consumption is both in receive and in transmit mode as low as 10.5mA • Available in QFN48 (7mm x 7mm) packages

Model: SiGe2-Power **RSC No:** 15829
A bipolar semiconductor technology for RF applications with high frequency and high power requirements • Shrink version of Atmel's SiGe1-Power bipolar 0.8 micron process • Supports simultaneous use of two available transistor types with switching speeds of 35/45 GHz cut-off frequency, 90 GHz cut-off for power gain, and breakdown voltages of 6/4V • 3-layer metal system optimized for high current densities

Wavecom Inc.

Web site: www.wavecom.com
Model: WISMO **RSC No:** 14578
A ready-to-use solution for wireless communication • Contains all the digital, baseband, and radio frequency hardware and software required for a complete wireless solution • Based on an open platform • Modular User Software Environment (MUSE) platform provides: Access to the protocol stack, software development tools, and support • Features such as WAP, hands-free, voice recognition, and multimedia SMS are software-based.

CompactPCI Systems 2004

The Magazine for Developers of Industrial, Communication, and Embedded PCI Systems

ISSUE	EDITORIAL FEATURES: SPECIAL FEATURE	TECHNOLOGY FEATURE	APPLICATION FEATURE	PRODUCT GUIDE	PROMOTIONS	DEADLINES: Editorial: Abstract Due	Editorial: Article Due	Advertising: Ads Close	Advertising: Ads Due
JANUARY	Guide to selecting memory	Transitioning to Optical Network Architectures	Embedded Internet devices	Mission critical products • MIL-STD • Ruggedized	CompactPCI reference CD sponsorships available	Oct. 15	Nov. 15	Nov. 14	Nov. 28
SPRING	Spring CompactPCI/ATCA Catalog				ESC/Electronica distribution	Dec. 15	Jan. 15	Jan. 15	Jan. 30
MARCH	Designing with DSPs and FPGAs	High Availability • Failures • Fault tolerance • Testing	Applications that protect and serve • Military • Homeland security	SBCs & chips: • Intel • Motorola • MIPs • IBM • ARM	SBC poster	Dec. 15	Jan. 15	Jan. 15	Jan. 30
APRIL	Next generation telecom: • Applications for Carrier IP networks • Wireless applications and the Internet • Wi-Fi Technologies • Wireless testing • Blades and servers • Looking toward optics				Telecom pullout	Jan. 15	Feb. 13	Feb. 13	Feb. 27
MAY/JUNE	Consortium issue: • PICMG standards update • PCI Sig standards update • Interconnect update from: RapidIO Trade Association and StarFabric Trade Association				Sponsorship tabs available	Feb. 13	Mar. 15	Mar. 15	Mar. 29
JULY/ AUGUST	Security issues in next generation networks	The migration to Packet-Based and VoIP Networks	Transportation applications: • Vetronics • Avionics • Mass transit	PMCs, PrPMCS, PTMCs, PCI-X, PMCs, CCPMCs, and Carriers	Annual online survey ESC Boston product preview	April 15	May 14	May 14	May 28
SEPTEMBER	Packaging issue: • Hear from the technology innovators and business leaders driving this industry • Product selection guide covering displays to power sources summarized by application				Packaging poster	June 15	July 15	July 15	July 30
OCTOBER	You can use Ethernet, exploring the new generation of Ethernet and the alternatives	Multi-board architectures • Components • OS support • Interfaces • Redundancy	Have it your way: custom applications	ATCA Spotlight	ATCA reference CD sponsorships available	July 15	July 15	July 15	July 30
NOVEMBER	Embedded software: • Dev tools • RTOS • Networking protocols • Middleware • Prototyping tools • BSPs	Understanding hot swap	Working for the government: • Server clusters • Global communications	I/O Source Book: Analog, Digital, Multi-functional, Industrial	Software pullout	Aug. 13	Sept. 15	Sept. 16	Sept. 30
DECEMBER	Special Issue: 2005 Buyer's Guide The most comprehensive source of CompactPCI and ATCA product information				Sponsorship Tabs/ adlets/spotlight ads	Sept. 15	Oct. 15	Oct. 15	Oct. 29

Also included:
New Products, Specifications Corner, CompactPCI Perspective, PCI Express, StarFabric Watch, PICMG Europe, Market Studies, Book Reviews, Software Corner, Technology Update, Homeland Security, Specifications Corner

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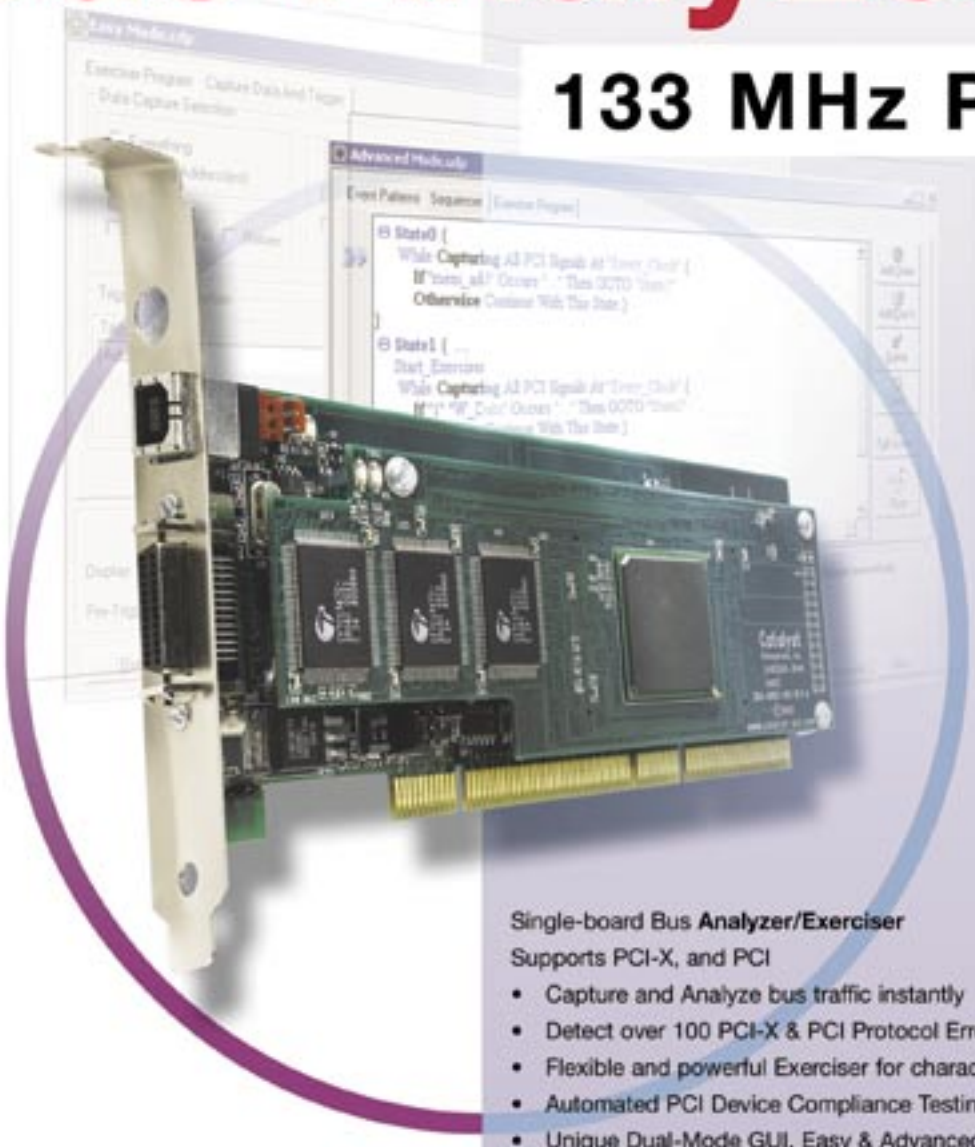
TA800

Bus Analyzers

133 MHz PCI-X



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