



Embedded COMPUTING DESIGN

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WINTER 2004

Vol. 2 No. 5

SPECIAL FEATURE:

Six-pin SOT-23 microcontroller promotes non-traditional usage

ALSO:

High-Availability
system design

Built-in Test for
mission-critical systems

TECHNOLOGY FEATURE:

Linux cluster considerations



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SOT-23 MICROCONTROLLER

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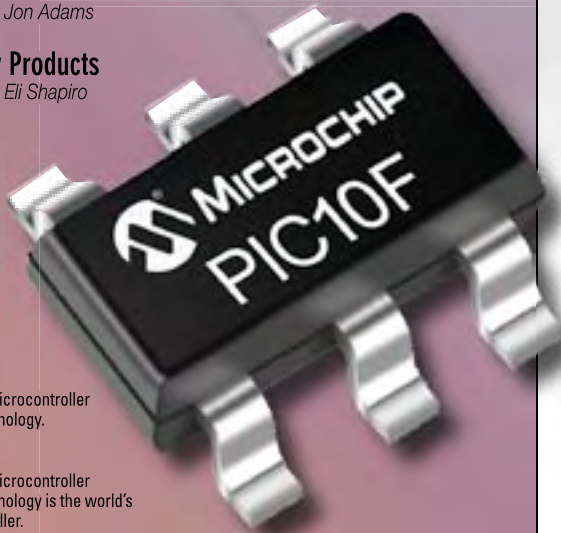
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WINTER 2004

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Product:
The PIC10F SOT-23 microcontroller
from Microchip Technology.

Cover:
The PIC10F SOT-23 microcontroller
from Microchip Technology is the world's
smallest microcontroller.

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Computing
Design
published by:

 **OpenSystems
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An OpenSystems Publication

ISSN: Print 1542-6408, Online 1542-6459

Embedded Computing Design is published quarterly by OpenSystems Publishing LLC., 30233 Jefferson Ave., St. Clair Shores, MI 48082.

Subscriptions are free, upon request in writing, to persons dealing with or considering *Embedded Computing Design*. For others inside the U.S. and Canada, subscriptions are \$24/year. For 1st class delivery outside the U.S. and Canada, subscriptions are \$50/year (advance payment in U.S. funds required).

Canada: Publication agreement number 40048627
Return address: WDS, Station A, PO Box 54, Windsor, ON N9A 615

POSTMASTER: Send address changes to

Embedded Computing Design
13253 La Montana, Suite 207 • Fountain Hills, AZ 85268



SALES OFFICE 586-415-6500

VP OF MARKETING & SALES
Patrick Hopper
phopper@opensystems-publishing.com

SENIOR ACCOUNT MANAGER
Dennis Doyle
ddoyle@opensystems-publishing.com

PRINT/ONLINE MARKETING SPECIALIST
Christine Long
clong@opensystems-publishing.com

MARKETING REPRESENTATIVE
Andrea Stabile
astabile@opensystems-publishing.com

ACCOUNT MANAGERS
Doug Cordier
dcordier@opensystems-publishing.com

Tom Varcie
tvarcie@opensystems-publishing.com

EUROPEAN REPRESENTATIVE
Stefan Baginski
sbaginski@opensystems-publishing.com
+41(0)62 758-3222

FOR REPRINTS:
Call the Sales Office

PUBLISHERS

John Black, Michael Hopper, Wayne Kristoff

ADVERTISING/BUSINESS OFFICE

30233 Jefferson Avenue
St. Clair Shores, MI 48082
Tel: 586-415-6500 • Fax: 586-415-4882

EDITORIAL/PRODUCTION OFFICE

13253 La Montana, Suite 207
Fountain Hills, Arizona 85268
Tel: 480-967-5581 • Fax: 480-837-6466

SENIOR TECHNICAL EDITOR

Mark David Barrera
mbarrera@opensystems-publishing.com

TECHNICAL EDITOR

Chad Lumsden
clumsden@opensystems-publishing.com

NEWS EDITOR

bicrutcher@opensystems-publishing.com

NEW PRODUCTS EDITOR

Eli Shapiro
newproducts@opensystems-publishing.com

ASSOCIATE EDITOR

Anne Fisher

VICE PRESIDENT OF EDITORIAL

Rosemary Kristoff
rkristoff@opensystems-publishing.com

MANAGING EDITOR

Bonnie Crutcher

CONTRIBUTING WRITERS

Jon Adams
Markus Levy
Bill Weinberg

SENIOR DESIGNER

Joann Toth

SENIOR WEB DESIGNER

Konrad Witte

WEB DESIGNER

Eric Okorie

BUSINESS MANAGER

Karen Layman

CIRCULATION/OFFICE MANAGER

Phyllis Thompson
subscriptions@opensystems-publishing.com

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ARROW

The wide range of development



Mark David Barrera

Welcome to the Winter issue of *Embedded Computing Design*. This issue's feature articles illustrate the wide range of current embedded development efforts.

New applications

■ *World's smallest microcontroller promotes non-traditional usage*, by Reston Condit of Microchip Technology, describes why Microchip created its new 6-pin microcontroller. It also includes several real-world applications that illustrate the non-traditional usage possibilities for the 6-pin SOT-23 microcontroller.

High availability

■ *PCI Express and Non-Transparent Bridging support High Availability*, by Akber Kazmi of PLX Technology, is a discussion of today's high availability challenges, and new approaches to high availability system design.

■ *High Availability application ready platform design*, by Asif Naseem of GoAhead Software, describes the development choices made by Telecom Equipment Manufacturers (TEMs) for today's high availability systems.

Mission-Critical systems

■ *Complementing high MTBF systems with Built-In-Test: The role of deployed test in mission-critical systems*, by Andy West of Radstone Technology, is a thorough description of their comprehensive approach to deployed test in mission-critical systems.

Linux clusters

■ *Software and tool considerations for Linux clusters*, by Michael Duffy of QS Technology and Duncan Roweth of Quadrics, is a discussion on the technical and managerial challenges that confront the growth of the Linux cluster market, and how system software tools can impact Linux clusters.

As mentioned in the Fall issue, we are raising the technical level of our articles in order to keep pace with the rapid change in the embedded industry. Please do not hesitate to send in an article abstract for a complex subject.

I hope you enjoy my third issue as Sr. Technical Editor of *Embedded Computing Design*. As always, I encourage your comments and suggestions concerning this and future issues.

M. D. Barrera

Mark David Barrera
Sr. Electrical Engineer
Sr. Technical Editor

mbarrera@opensystems-publishing.com

LOOKING FORWARD

By popular demand, we will publish an additional *Embedded Computing Design* issue for 2005.

We are now a bi-monthly publication, offering six issues a calendar year.

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See the editorial calendar (www.embedded-computing.com) for further details.

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| IEEE1394 Number Type _____ a _____ b | CAN Number Type _____ low sp. _____ high sp. | Audio <input type="radio"/> line in & out <input type="radio"/> mic. in <input type="radio"/> amplifier | Misc <input type="radio"/> MOST <input type="radio"/> SPI, no: _____ <input type="radio"/> I2S, no: _____ <input type="radio"/> RTC + battery <input type="radio"/> IR | I/Os No. Type _____ digital _____ analogue | Other <input type="radio"/> _____ <input type="radio"/> _____ <input type="radio"/> _____ <input type="radio"/> _____ |

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By Markus Levy



Automotive real-time benchmarks

Automotive benchmark requirements

The development of microcontroller benchmarks for the automotive industry is among the biggest challenges for the EEMBC.

For one thing, this industry is always designing for tomorrow's state-of-the-art technology. The test time for new products is so long that designs have to reach out five years or more.

Furthermore, compared to most other embedded applications, automotive

presents one of the harshest operating environments imaginable. For example, I was amazed recently to learn that one manufacturer requires an oil change every 13,000 miles! Obviously, that feature is related to the mechanical aspects of the car, but similar endurance is expected of the car's electronic components.

In addition, most automotive suppliers use proprietary methods to deal with their design challenges. This drives the requirement that new benchmarks be generic enough to satisfy a wide range of automotive suppliers. Of course, processor

vendors will still have to prove their performance to potential customers while running other proprietary benchmarks, and/or the customer's applications.

Automotive benchmark development

The EEMBC Version 1 automotive/industrial benchmarks have been available for about five years. Although many of these benchmarks are squarely aimed at the automotive industry (such as table lookup and interpolation, angle to time conversion, CAN remote data request, tooth to spark, and road speed calculation), they serve as good general-purpose workloads for microprocessors because they do not involve peripherals or system-level effects. As a representation of the true automotive environment, however, they are limited. They do not test the real-time performance of the microcontrollers or their peripherals, and this is the primary concern of automotive customers.

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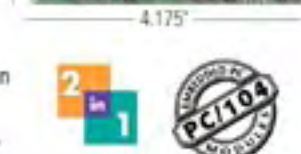
The Athena extended temperature embedded CPU combines high performance, high integration, and rugged design into a small size (4.175" x 4.475"). Athena integrates the low-power Pentium-III class VIA Eden processor (400-660MHz) with a full range of standard I/O features as well as data acquisition. The result is a small, low-cost, yet extremely versatile embedded CPU that fits in tight spaces and survives harsh environments. With 128MB on-board memory, LCD+CRT video, AC97 audio, 4 USB ports, 4 serial ports, and PC/104 expansion, Athena is an all-in-one, complete solution.

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- 128MB memory soldered on board
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- Operating temperature -40 to +85°C
- Power dissipation: 9.5 W / fanless (400 MHz); 11 W / fan (660 MHz)
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- 12-bit and 16-bit A/D
- 2-16 analog outputs
- 12-bit and 16-bit D/A
- Autocalibration
- -40 to +85°C operation

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- 24 programmable digital I/O
- -40 to +85°C operation

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2 in 1



- 2 PCI-based 10/100Mbps Ethernet ports
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- 24 programmable digital I/O
- -40 to +85°C operation

NEW!

2 in 1

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2 in 1

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- Reduced system size and weight
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The Diamond Systems Solution

The 2-in-1 concept from Diamond Systems

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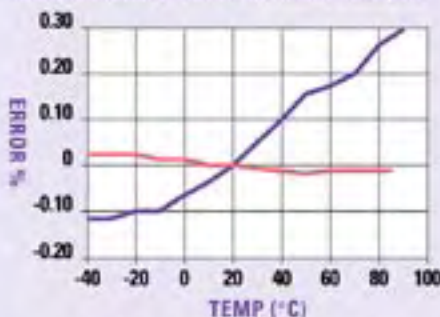
What's more, with autocalibration you can recalibrate both A/D and D/A circuits in just seconds under software control. No test equipment or handling is required. This means less downtime and lower maintenance costs.

DIAMOND SYSTEMS EMBEDDED BOARDS WITH AUTOCALIBRATION:

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- DMM-AT A/D board
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- DMM-32-AT A/D board

BENEFITS OF AUTOCALIBRATION

MEASUREMENT ERROR VS. TEMPERATURE



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THINKING PC/104? THINK DIAMOND.

As part of the evolution of the EEMBC, we are adding real-time benchmarks to test how a processor behaves in-situ to the target application. To accomplish this, the new automotive benchmarks will use special hardware-based exerciser equipment that provides a stimulus to the I/O and interrupt pins of the device, and then captures/verifies the output. As shown in Figure 1, the Device Under Test (DUT) is connected to an exerciser board with software configurable peripheral functions.

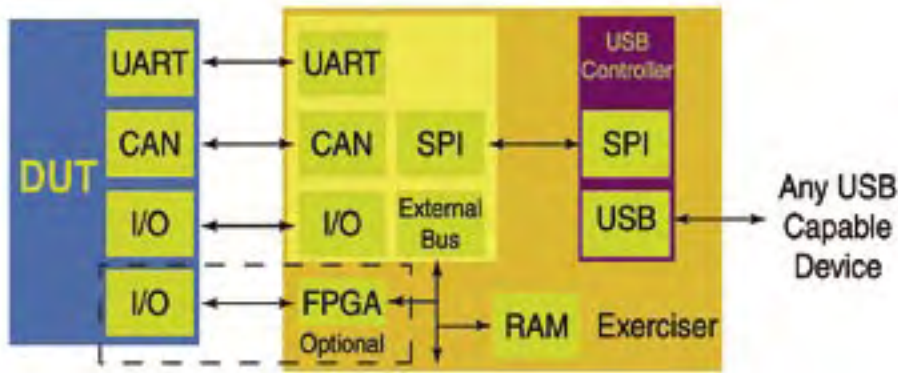


Figure 1

The purpose is to determine how a device acquires and processes data, and then report on the results. However, it is not the goal of these benchmarks to test the capabilities of each peripheral – hopefully that is guaranteed by the manufacturer.

Planned tests

The current plan for the new benchmark suite is to perform physical hardware tests for:

- Capture/compare timer
- Serial Port Interface (SPI)
- Controller Area Network (CAN)
- Pulse-Width Modulation (PWM)
- Analog-to-Digital Conversion (ADC)
- Universal Asynchronous Receiver-Transmitter (UART)

In addition, the processor’s Direct Memory Access (DMA) controller, interrupt control, and context switch capabilities are inherently tested by the combination of different tasks. The exerciser board will generate the appropriate signals to emulate each of these peripheral functions to perform the test.

This methodology actually sets a new precedent for EEMBC. Never before have we had real-time performance benchmarks whereby the microcontroller is responding to real world hardware signals.

More details on the new benchmark suite will be available in the first quarter of 2005, but until then, we invite you to get involved and help to define the next benchmark standard for the automotive industry.

Markus Levy is founder and President of EEMBC. He is also Technical Editorial Director and Analyst at ConVergence Promotions. Mr. Levy received several patents while at Intel for flash memory architecture and for flash memory drives.

EEMBC – the Embedded Microprocessor Benchmark Consortium – was formed in 1997 to develop meaningful performance benchmarks for embedded system hardware and software. Contact the EEMBC directly for membership and certification information.



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By Bonnie Crutcher

■ INDUSTRY NEWS

RapidFabric Multicast and Data Streaming Specifications approved

The RapidIO Trade Association has announced the approval and member availability of two new additions to the family of specifications known as the RapidFabric extensions. The RapidFabric specifications add features to the RapidIO architecture that address the market for inter-working and traffic-managed communications fabrics. The RapidFabric extensions seamlessly interoperate with the existing RapidIO specification, and allow OEMs to replace proprietary interconnects with an open, industry-standard fabric, reducing R & D costs while decreasing time to market in high-speed data plane applications.

“As a capability implemented in Mercury systems for more than 10 years, multicast continues to solve some of the most demanding signal and imaging problems today,” says Craig Lund, CTO for Mercury Computer Systems. “The multicast implementation in RapidIO enables us to continue to provide a competitive advantage to our customers.”

The new Data Streaming specification Phase 1 adds a logical protocol to RapidIO, which supports additional features that are required in the communications market segment.

For more information: www.RapidIO.org

SKY Computers chosen by Lockheed Martin for U.S. Navy's TEP program

SKY Computers, Inc., a subsidiary of Analogic Corporation, recently announced that Lockheed Martin Maritime Systems & Sensors (MS2) of Moorestown, N.J., is installing the SKY high-performance embedded server for the U.S. Navy Tactical Environment Processor (TEP) program.

Lockheed Martin selected the SKY SMARTpac 600 for the U.S. Navy's Tactical Environment Processor (TEP) program because the SKY product complies with open standards. This weather processing system is based on the ground-based, SKY-supported system installed at the National Weather Radar Test Bed in Norman, Oklahoma. The TEP program benefits both war fighters and meteorologists, and is intended to be an effective tool for both user groups.

For more information: www.skycomputers.com

Pericom Semiconductor delivers industry dominant performance DDR2 buffer and PLL for registered DIMMs

Pericom Semiconductor Corporation, a worldwide supplier of high-speed integrated circuits and frequency control devices, recently announced the release of its industry leading performance DDR2 Registered Buffers and PLL Clock for Registered DIMMs. Next-generation higher performance systems such as servers, routers, switches, and workstations utilize these DIMMs.

Jaci Chang, Product Marketing, stated “Pericom is pleased to announce Intel validation of its new DIMM products. Our registers and clock driver provide a complete JEDEC standard DDR2

DIMM solution. This new enhanced solution demonstrates our commitment to cutting-edge products in support of the DIMM market ...”

For more information: www.pericom.com

■ TECHNOLOGY PARTNERSHIPS

Curtiss-Wright Controls Embedded Computing and Pentland Systems announce strategic alliance

Curtiss-Wright Controls Embedded Computing (CWCEC) and Pentland Systems have announced a strategic alliance to combine their capabilities and products to supply the military and commercial aerospace markets with signal processing solutions.

For developers and integrators of such radar and other signal processing systems, the collaboration will result in the ability to deliver integrated card sets, subsystems, and software solutions that have been designed, tested, and manufactured with this interoperability and performance in mind. The result is shortened and less costly development time, and reduced total cost of ownership for end users.



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The product interoperability validation of Pentland Systems products is being performed under the Curtiss-Wright Controls Embedded Computing "EXTENSIONS" partner program.

A partner product carrying the "EXTENSIONS" program Certified Product logo, is an indication that the product has been certified as being mechanically, electrically and software interoperable with specified Curtiss-Wright Controls Embedded Computing products.

For more information: www.cwembedded.com

Arcom helps roll out GPRS-based telemetry system for Central Networks

Arcom announced a contract with Central Networks to supply industrial network gateways to enable the use of conventional DNP3 equipment over TCP/IP on a GPRS wireless network.

The system uses Arcom's DIRECTOR series industrial network gateways located at remote points on the electricity distribution network. It will facilitate the use of GPRS communications by existing devices originally designed to operate over local serial communication links. The DIRECTOR handles the protocol conversion and manages the remote connection to the client's host SCADA system using TCP/IP over the GPRS wireless network. DIRECTORS will initially be deployed at more than 500 remote locations and will dramatically reduce both the capital cost and operating costs for communications to these sites. The DIRECTOR units are viewed as an important tool to assist the end user in migrating all communications to TCP/IP over the next few years. "The rapid deployment of the DS3 and its flexible configuration were integral to the success of this project," said Roger Hey, project manager for Central Networks.

For more DIRECTOR information: www.arcom.com
For more GPRS information: www.central-networks.co.uk

Kozio's diagnostics software platform supports ADI Engineering's Pronghorn Wi-Fi Application Platform

Kozio, Inc., a developer of embedded systems software, has introduced new software to support ADI Engineering's Pronghorn 802.11 Application Platform based on the Intel IXP42x. Kozio's test software now ships with this ADI product, providing diagnostic and manufacturing test capabilities to manufacturers who build WLAN products using Pronghorn.

The ADI Pronghorn is designed to provide WLAN equipment manufacturers with a "plug-and-play" product solution to help them bring wireless solutions to market quickly.

For more information: www.kozio.com

■ CONSORTIUMS & WORKING GROUPS

EEMBC adds six new members, bringing total to 58

EEMBC, the Embedded Microprocessor Benchmark Consortium, recently announced that Applied Micro Circuits Corporation (AMCC), Juniper Networks, Marvell Semiconductor, Patriot Scientific, Qualcomm, and Rockwell Collins have joined the ranks of its members.

With these new additions, the consortium counts 58 corporate members, including 42 board of directors members who have

access to source code for all of the EEMBC benchmarks and exercise full voting rights on all issues decided by the consortium.

"As EEMBC grows, we're seeing that industry-standard processor benchmarks have applications beyond what anyone expected when this consortium was founded seven years ago," said Mark Levy, EEMBC President. "They serve the needs of companies that want a reliable means of testing their own processors; they allow systems designers to make apples-to-apples comparisons between competing processors, and they serve the business needs of companies who are asked – increasingly – to provide customers with objective performance data for their processors."

For more information: www.eembc.org

■ PEOPLE

AccelChip Inc. appoints Vin Ratford as President and Chief Executive Officer

AccelChip Inc., industry provider of automated flows from MATLAB algorithms to silicon, announced recently it has appointed EDA and Semiconductor IP veteran Vin Ratford to serve as the company's president and CEO.

Ratford has served on AccelChip's Board of Directors since 2002. He brings more than 25 years of experience to the position.

"In my work with the company, I've seen accelerating customer interest and success with the AccelChip toolset. The AccelChip DSP Synthesis tool has matured to the point where it's rapidly becoming accepted into communications and military/aerospace industries, and the AccelWare parametric libraries continue to expand," said Ratford. "The opportunity to lead the company as it moves toward full acceptance in the marketplace is a venture I just couldn't pass up. I look forward to moving AccelChip into profitability."

For more information: www.accelchip.com

Worldwide Numerical Algorithms Group announces new leadership

Dr. G. Richard Field, Chairman of The Numerical Algorithms Group (NAG), has previously announced the appointment of a new executive management team for the company following the retirement of two top executives.

- Effective August 1, 2004, Dr. Rob Meyer, the President of NAG Inc. in the United States, has been named CEO of the NAG group of companies as well as Director of NAG Ltd.
- Dr. Steve Hague, Deputy Director of NAG Ltd., has been named COO of NAG Ltd. and CTO for the NAG group of companies.
- Mr. Hiro Chiba has been appointed as Representative Director of Nihon NAG, effective July 1.

For more information: www.nag.co.uk

StarGen names Wade Appelman VP of marketing and business development

StarGen, a fabless semiconductor company specializing in advanced serial switched interconnect solutions, has announced that Wade Appelman has joined the company as the vice president of marketing and business development. A seasoned executive with strong marketing and startup experience, he has held leadership

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positions with several innovative system and semiconductor companies such as Vitesse Semiconductor and Cabletron Systems.

Appelman will be responsible for leading the marketing effort for StarGen's StarFabric product line, and will drive the establishment of the company's next-generation Advanced Switching platform as the dominant switched interconnect solution for next-generation communication, storage, server, and embedded system designs.

Anadigm appoints Nathan W. John as Vice President of Worldwide Marketing

Anadigm recently announced that Nathan W. John, a semiconductor industry veteran with more than 20 years experience in marketing, has joined the company as its vice president of worldwide marketing.

A fabless semiconductor company based in Tempe, Ariz., and Crewe, UK, Anadigm provides Field Programmable Analog Array (FPAA) integrated circuits and associated design software that greatly reduce the time, effort, and expense required to create dynamic real-world interfaces for audio, industrial, RFID, and environmental control systems.

"Nathan's experience in developing and implementing product strategies for high-growth programmable and analog components will play a key role in our drive to identify and

penetrate high-volume opportunities for Anadigm FPAA's," said William McLean, Anadigm president and CEO.

For more information: www.anadigm.com

Freescale Semiconductor delivers complete, single-chip Fast Ethernet solution

Freescale Semiconductor, Inc. has reduced both complexity and cost for system designers with the introduction of the industry's first complete, single-chip 10/100 Mbps Ethernet device. The 16-bit MC9S12NE64 microcontroller replaces the more complex multi-chip Ethernet offerings.

"Designers who choose the MC9S12NE64 can expect to reap the benefits of a single-chip Fast Ethernet (100 Mbps) solution, increasing reliability and reducing the size of the Ethernet control footprint within a system," said Daniel Hoste, vice president and general manager of Freescale's 8/16-bit Products Division. "These benefits help make Ethernet connectivity an easy option for new applications and low-cost systems where it may not have been practical in the past."

The MC9S12NE64VTU is now available in sample quantities.

For more information: www.freescale.com

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Sound and Fury at GSPx



By Bill Weinberg

I just attended the Global Signal Processing Expo (GSPx) held at the Santa Clara Convention Center from Sep 27-30. This conference targets a broad range of signal processing applications including automotive, consumer electronics, defense/aerospace, telecommunications, and wireless. The conference places a special emphasis on Software Defined Radio, Wi-Fi, and multi-media. Clearly, GSPx goes well beyond the embedded use of off-the-shelf DSP hardware. The conference is not entirely new – founder Amnon Aliphas has successfully presented signal-processing-focused events and other embedded systems conferences for the past decade.

GSPx featured over 500 papers, 4 keynote addresses, 10 half-day technical workshops, 10 panels, and numerous presentations and exhibits from dozens of companies. According to show organizer Phil Cieply, the conference drew over 1200 attendees, which is impressive when web-based information sourcing is so dominant and the tech sector is still emerging from a major slowdown.

OS and embedded software panels

Given my emphasis towards Open Source and embedded software, I attended the following two embedded system panels:

- *Linux and RTOS in Distributed Systems*, hosted by analyst Tom Williams.
- *Selecting an Embedded Operating System: A Client's Perspective*, hosted by Brian Mendel of Boeing Phantom Works.

Both panels were reasonably well-attended. Each panel member had a presentation, which was followed by an audience participation session. Unfortunately, the panel hosts should have been stronger participants in their own events, as the unrestrained panelists presented sales infomercials rather than unique technical or industry viewpoints. Moreover, the presentations were too long, and thus little time remained for audience questions or meaningful discussion.

The Linux and RTOS panel

The first panel focus was that both Linux and traditional RTOS platforms can exist in multi-tier embedded designs. Examples include communications equipment structured with distinct management and control/data planes, where Linux hosts management applications, and a combination of Linux and RTOS support blade or line-card applications.

Panelists from Wind River Systems (VxWorks RTOS) and Enea Embedded Technology (OSE RTOS) aptly positioned their own

Linux offerings in this context, by striving to retain room for their RTOS in a space increasingly dominated by Linux and other Free and Open Source Software (FOSS) components.

Metrowerks partners with traditional RTOS and embedded Linux suppliers (and inherits Linux platform tools from Lineo). They therefore took an expected neutral stand by echoing other panelists' call for tools that address both operating systems in a mixed environment.

Linux and Open Source debate

Much less amenable to useful coexistence was Dan O'Dowd of Green Hills Software (INTEGRITY RTOS). Rather than respond

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to the panel host's call for commentary on the balance between Linux and RTOSs, Mr. O'Dowd chose to use his panel slot as a forum for a public discourse against Linux and its embedded application. In my opinion, he made numerous questionable and misleading statements about Linux and Open Source.

Since most of Mr. O'Dowd's arguments build on common misconceptions about Open Source Software (OSS), they merit closer examination.

Footprint – Is Linux too big for embedded?

Mr. O'Dowd compared Linux to a Mac truck attempting to compete at Le Mans. Certainly, full-blown enterprise Linux and fully-outfitted embedded Linux configurations can produce multi-megabyte system images. However, no one ever asserted that Linux was a Formula Racer.

Linux was designed to tow heavy loads and still perform – something team Ferrari need not worry about. Also, unlike the minimal RTOS software of Mr. O'Dowd's reference, Linux provides a stable and complete platform that is ready to run an enormous array of COTS software.

By contrast, RTOS systems are built selectively from libraries, where each deployment only draws on the routines actually required by the application. If an RTOS like Green Hills INTEGRITY were configured to match the Linux basic capability set, its footprint would run to many megabytes, and actually be larger than that a comparable Linux system footprint.

Real-Time – Can Linux meet real-time deadlines?

Linux is not an RTOS. It was not designed for full pre-emptibility, or to offer the most rapid interrupt response times. Instead, it was designed for robustness and throughput.

Industry studies and real-world experience shows that 90% of all embedded applications do not have hard real-time requirements. Moreover, 87% of respondents to a VDC study of embedded Linux found that Linux fully satisfies their real-time needs. Certainly there exist numerous applications that need traditional hard real-time. And a large portion of such applications fall into the aerospace and defense arena that RTOS companies target.

But even traditional aerospace and defense applications, to say nothing of thousands of projects in consumer electronics, networking, telecommunications, instrumentation, and control are choosing embedded Linux instead of RTOS.

Standards – Is Linux standards-compliant?

In a word – yes. Linux, like the other UNIX-type operating systems, is POSIX compliant by definition. That is, it implements a large subset of one of the dozens of sub-standards that fall into the IEEE 1003 family for OS definition.

It is not fully conformant to any one of those subsets (for example, what used to be called POSIX.1 – UNIX OS definition, or POSIX.1c, threading), in that Linux does not pass all suite tests such as the Open Group or original NIST suite tests. In some cases, the Open Source community has not invested the time in creating conformant APIs and behaviors. In other cases, Linus Torvalds and others have made conscious decisions to avoid the awkward constructs and overly complex semantics that POSIX predicates.

Beyond POSIX, Linux and its application stack offer developers a veritable alphabet soup of standards compliance such as:

- BSD
- CORBA
- Java
- NFS
- OSPi/BGP/RIP
- Perl/PHP
- SMB
- SSL/SSH
- TCP/IP (IPv6)
- X11

Furthermore, many assert that Linux itself constitutes a viable standard, or at least an emerging one. Certainly more code has been created for and ported to Linux than any for proprietary OS or RTOS, including those that do pass the vaunted POSIX conformance tests.

Support – Does first-tier support exist for Linux?

Proprietary RTOS companies do provide a very direct type of support – they create their own code and then (usually) support it as part of their business model. Embedded Linux companies, however, contribute to a community code base, and also support the code developed outside their walls.

The proprietary develop/support model proves challenging to sustain in real life: companies purchase each others' IP, phase out product versions, and habitually end-of-life whole product lines, leaving customers stranded.

Even when long-lived companies offer long-term support for their products, the team that actually produced the code is typically not the team that supports it. In most companies past start-up stage, the developers that produced the code have long since departed by the time you purchase it. In addition, at any point in a product life cycle, most proprietary software companies cannot afford to dedicate significant resources to technical support and continual engineering.

Not so with Open Source Linux. Any given piece of Linux or other OSS code is a shared resource, and will therefore have dozens or even hundreds of companies that provide support for it. There are even mailing lists for help with most projects, and you can obtain support for Linux 2.6 and prior versions. And, unlike most proprietary software, you can maintain Linux yourself.

Licensing – Does GPL-licensed Linux force OEMs to open their IP?

The GPL (General Public License) for the Linux kernel source code obligates developers who redistribute binaries derived from GPL code to accompany those binaries with source (and a copy of the GPL license).

Developers, ISVs, and embedded device OEMs can and do retain control of proprietary IP in application code, libraries, middleware, and even device interface code.

Just ask BMW, Cisco, D-Link, GE, HP, IBM, Intel, Motorola, NorTel, NTT-DoCoMo, Panasonic, Philips, Samsung, Sony, Yamaha, and hundreds of other Global 1000 companies that build their devices and infrastructure with Linux.

Development – Is open source development disciplined or ad hoc?

Traditional proprietary RTOS code is developed by a small cadre of engineers under great pressure to meet product market deadlines. Because most code consumers will never actually be able to browse through the source, proprietary kernel and OS code quality can vary widely. So can the discipline that governs its creation, including design methodology, coding standards, code review practices, and quality assurance.

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By contrast, Open Source Linux and its development practices are highly transparent. For better or for worse, the whole world can inspect the code, examine the practices used to create it, and via attribution even know the pedigree of each engineer contributing to it.

Just because the Linux and OSS base is large does not mean it lacks structure and discipline. Just within the Linux kernel, there are distinct teams that maintain subsystems like memory management, the virtual file system, the scheduler, and the distinct interfaces like USB or PCI. The maintenance teams selectively accept contributions from qualified community members and make their own contributions, and then must petition the top-level kernel maintainers (for instance, Linus Torvalds) for acceptance on merit, style, and code quality.

The Open Source development process is so well disciplined that it has integrated and quality-assured contributions from thousands of developers in dozens of countries.

The embedded OS selection panel

The second panel proved almost as contentious as the first. Despite its focus on embedded OS selection for aerospace and defense applications – an area not currently well served by Linux – the panelists included representatives from embedded Linux vendors MontaVista and TimeSys, dual-OS supplier Wind River, and Linux consultant Doug Locke. It also included Mr. O'Dowd of Green Hills Software and his views against the adoption of embedded Linux.

Once again, the panel leader could have done more to drive the panel and to cut short yet another round of vendor sales presentations. Too little time remained for meaningful interaction, and the dialog that did occur steered predictably back to the questioning of the viability of embedded Linux by the traditional RTOS-consuming audience.

What disturbed me most was that the embedded Linux advocates on the panel were unprepared to meet this barrage of criticism and tough questioning. Unfortunately, most of Mr. O'Dowd's assertions and the audience's concerns about Linux went unchallenged and unanswered. The advocates were unprepared even after current analyst reports indicate that Linux is now the number one embedded OS.

There are days when I wonder if the success of embedded Linux really comes from our efforts, or occurs in spite of them. This was one of those days.

Bill Weinberg brings more than 17 years of embedded and open systems experience to his role as Open Source Architecture Specialist at the Open Source Development Labs. Bill can be contacted at bweinberg@osdl.org.

OSDL – home to Linus Torvalds, the creator of Linux – is dedicated to accelerating the growth and adoption of Linux in the enterprise. Contact the OSDL directly for membership and lab usage information.

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By Bonnie Crutcher

Rockwell Collins to use LynxOS-178 RTOS by LynuxWorks

LynuxWorks, Inc. recently announced that Rockwell Collins will use its LynxOS-178 Real-Time Operating System (RTOS) as part of the recently awarded contract from the U.S. Army Aviation Applied Technology Directorate (AATD) for the Manned/Unmanned Common Architecture Program Phase III (MCAP III).

MCAP III will develop and demonstrate an avionics architecture for Army unmanned aircraft that is common to mission processing systems currently under development for Army helicopters and Future Combat System (FCS) ground vehicles.

The Rockwell Collins MCAP III solution is based on an open-systems architecture approach. The company has chosen the LynuxWorks LynxOS-178 as the operating system. LynxOS-178 is a commercially available DO-178B level-A certifiable RTOS that meets the most stringent standards for safety-critical avionics systems. As a POSIX-conformant operating system, LynxOS-178 will assure application portability, software reuse, and interoperability between embedded military systems.

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Red Hat announces first annual summit

Red Hat, Inc., a leading provider of open source solutions to the enterprise, has announced the first annual Red Hat Summit. Summit 2005 will be held in New Orleans June 1-3 and will bring together the diverse people that make up the open source community, including community contributors, developers, customers, and partners. The Summit will blend different views and content into a program useful for attendees building and enabling open source architectures.

“The Summit is truly a user-driven event. It is an opportunity for open source users to thoroughly examine relevant choices for their infrastructures,” said Michael Tiemann, Open Source Advocate at Red Hat. “Users who have made the decision to deploy open source will be brought together and given a deeper, richer understanding of the implications of their technology decisions and how to scale those choices to the next level.”

For more information: www.redhat.com

American Arium delivers industry first full Linux support for ARM and Intel XScale processors residing on headless targets

American Arium recently announced support for ARM and Intel XScale systems running Linux. An industry first, the Arium hardware-assisted solution lets users seamlessly debug full kernel and processes/applications simultaneously on systems that have neither serial nor network ports.

“Our new Linux target debug solution is designed to improve users’ productivity on an exponential scale,” said Larry Traylor, Arium’s CEO. “In the past, there was no easy way to debug interactions between applications and the kernel because there was little or no visibility until kernel and console drivers were working. With Arium’s flagship SourcePoint debugger, developers can see everything from the launch of kernel boot code through the beginning of the initial process, even on headless targets. And they can do it in a Windows-like environment, making the debug process a lot more user friendly and easier to use.”

For more information: www.arium.com

Continuous Computing announces upSuite High Availability Middleware for Linux

Continuous Computing, the leading supplier of high availability Network Service-Ready Platform solutions for telecom equipment manufacturers, announced that its popular upSuite High Availability (HA) middleware program has been successfully ported to the Linux operating system to support easy deployment of mission-critical telecom infrastructure and enterprise networking applications. upSuite HA for Linux has been optimized for modular communications platforms using Intel Xeon and Pentium processors on AdvancedTCA, CompactPCI, and rack-mount server form factors.

A key distinguishing feature of upSuite HA is that it is extremely easy to install, maintain, and use because it is application transparent and can be easily integrated into a wide array of telecommunication

and enterprise networking applications. In addition, upSuite HA is equally applicable to the Continuous Computing AdvancedTCA product family as well as the Flex21 CompactPCI product line since the middleware was designed to work in heterogeneous hardware environments of dissimilar processors and disk storage methods.

For more information: www.ccpu.com

Diversified Technology, Inc and MontaVista Software formalize OEM agreement for Carrier Grade Linux

Diversified Technology, Inc. (DTI) and MontaVista Software, Inc. have announced a formal OEM agreement to promote the DTI Targa series of AdvancedTCA solutions pre-installed with MontaVista Linux Carrier Grade Edition (CGE). The collaboration supports both companies' commitment to modular, standards-based AdvancedTCA platforms for the telecommunications market. In addition to the DTI Targa product line, MontaVista Linux Carrier Grade Edition for the PlexSys line of PICMG 2.16 platforms will also be included in the development partnership. CGE is an advanced Linux-based development platform from market leader MontaVista Software, engineered specifically for the robust and highly available requirements of carrier grade applications.

"With DTI, we can provide our mutual equipment provider customers with a carrier-grade, scalable, integrated platform solution for networking-intensive infrastructure applications," commented Scott Jaffe, Vice President, Business Development, MontaVista Software.

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By Jon Adams

A ZigBee home networking example

A quick review

With the first ZigBee wireless technology-enabled product introductions occurring at the beginning of 2005, it is a good time to review how ZigBee networking performs its magic.

As you probably know, ZigBee networks are natively mesh-based, which means that ZigBee supports point-to-point and multiple hop connections to insure that a message can get from source to destination.

This is similar to the Internet or the telephone network, where there are hundreds of switching/routing centers spread throughout the world. Each center has multiple interconnections to other switching/routing centers, so that if a fiber route is out of service, the data can still go through almost without interruption.

Network device types

There are three types of logical network devices defined in a ZigBee network:

- The simplest device is an *End* device. The End device has no routing ability (in other words, it cannot manage someone else's traffic).
- The next level up the network is called the *Router*, which is fully mesh-capable and mains-powered (or powered from some other permanent source). Routers can establish multiple peer-to-peer links with other routing nodes, and accept connections from End devices. The Routers may also serve as a gateway to the Internet or to other networks.
- The highest functionality device is the mains-powered *Coordinator*, which has the authority to establish networks and perform whatever network management might be required. The Coordinator also has routing capability, and may serve as a gateway to the Internet or to other networks.

“... ZigBee supports point-to-point and multiple hop connections...”

There is only one Coordinator per ZigBee network, while there might be dozens of Routers, and potentially thousands of End devices. Most importantly, all devices are transceivers (they transmit and receive) since the ZigBee protocol expects most messages to receive an acknowledgement in order to verify successful reception.

End device functionality

End devices are often battery-powered. Typical End devices function as thermostats, humidistats, light switches, smoke detectors, and various sensors. These devices are often built as *peel and stick* products, where installation is intended to be simple, and product placement is either esthetic, functional, or per some

governmental requirement. These End devices do not form a mesh by themselves; instead, they are usually asleep in order to conserve their batteries.

Router and Coordinator device functionality

Since the Router and Coordinator devices are mains-powered, they are always listening for network traffic. Packets generated by End devices may pass through multiple Routers to travel from the source to a destination, which is generally a load-controlling function (such as a HVAC motor, lighting load control, damper actuator, siren). However, the destination may also be a data-collecting device like a computer or security console, or even a gateway to the Internet or other non-ZigBee network. All of these devices have a source of permanent power, so the ZigBee radio connected to these devices ends up being a Router or Coordinator.

Routers and Coordinators leave their receivers on except when transmitting, so they build up a table of neighbor nodes, which include routing nodes they can directly hear.



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ZigBee home example

The practical example shown in Figure 1 is a home with a ZigBee network that controls the lights, security system, fire system, and the heating and air conditioning.

The diagram shows a number of devices, where a red link is a Router-to-Router link, and a blue link is an End node to Router link.

Here, lighting fixture B (which might also be the Coordinator) has identified and established routes via Routers embedded in lighting fixtures A and F, mains-powered (with battery backup) smoke detector C, and table lamp D.

All the Routers are mains-powered devices (lamps, heat pump, lighting fixtures, smoke alarms) and the End devices are battery-powered (switches, thermostats, motion detectors). Sensors are bound to actuators through sometimes either the choice of the user, or because of specific binding specified by the manufacturer.

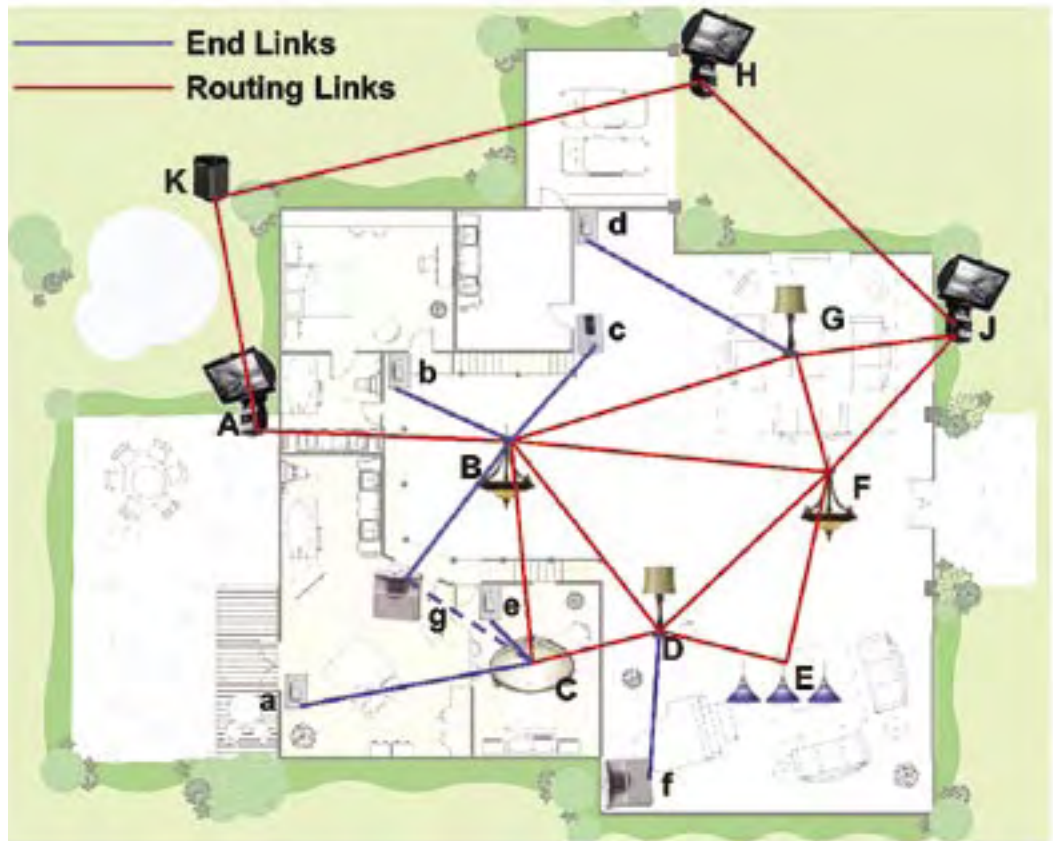


Figure 1

Home network topology

Light switch b is bound to and controls hanging lighting fixture B, and communicates with it directly (single hop). Some of the control is multi-hop: for instance, peel-and-stick thermostat/HVAC controller c communicates with the HVAC heat pump K located outside the home through a complex route, potentially due to RF obstructions or interference that might preclude a direct path. So when the home occupant wants to cool the house a bit, that command is sent from c to K through intermediaries B and A, both lamp fixtures behaving as network Routers. Note also that there is an alternate path, via B-G-J-H, which has more hops and is probably less efficient.

“All the Routers are mains-powered devices ... and the End devices are battery-powered...”

The network determines the cost of a route using various metrics and assigns the best route as the primary, and other less favorable routes as secondary. Why the secondary routes? Remember the ZigBee slogan: *Wireless control that simply works*. The message that the thermostat/controller sends out will generally take far less than 100ms to get to the HVAC heat pump, and the heat pump is expected to acknowledge that message in the same time. If the thermostat does not get the response, it will try again. If there is a network problem (for example, the link between B and A is disrupted due to interference), node B can go to the alternate route, where it sends the message via the longer path.

Another important aspect is that the network is a *multi-use system*, where lighting, HVAC, and security all can take advantage of the others' existing infrastructure. This is not mandatory, and can be defined by the manufacturer of individual devices, but allows a far more powerful and robust network to form quickly.

ZigBee advantages

ZigBee networks are able to form autonomous mesh-networked connections where routing devices establish multiple links with other routing devices. In addition, they continuously determine routing costs to allow the network to move traffic in the most efficient manner. This flexibility adds robustness and reliability to a ZigBee device, affording the user to best take advantage of *wireless control that simply works*.

Jon Adams is Chair of the ZigBee Alliance's Qualification Group, and is the Director of Radio Technology and Strategy for the Wireless and Mobile Systems Group of Freescale Semiconductor. Jon speaks and presents regularly on ZigBee, UWB, and the future of embedded wireless for machine-to-machine communications. Contact Jon at jta@freescale.com.

The ZigBee Alliance is an association of companies working together to enable reliable, cost-effective, low-power, wirelessly networked monitoring and control products based on an open global standard. Contact the alliance directly for membership and event details.

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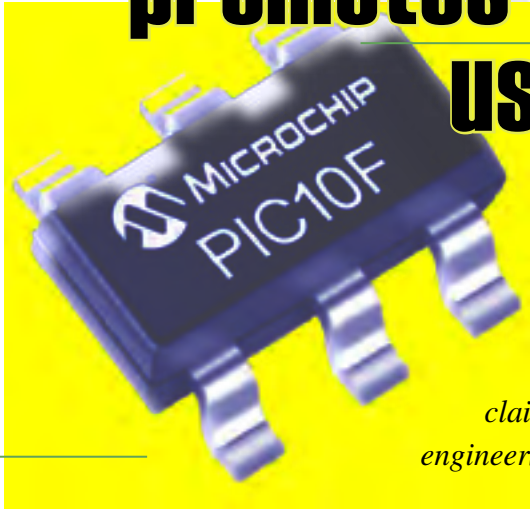


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World's smallest microcontroller promotes non-traditional usage



By Reston Condit

Microchip Technology's new PIC10F family consists of 6-pin, 8-bit Flash microcontrollers (MCUs) packaged in a SOT-23 form factor, making them the world's smallest microcontrollers. More than just a claim-to-fame, the PIC10F is poised to change the way engineers of all disciplines think about microcontrollers.

The performance, small size and equally small price tag (\$0.49 each in 10k quantities) of these microcontrollers has opened the door to new applications not traditionally served by microcontrollers. We will look at why Microchip created its 6-pin microcontroller, as well as some new applications where the 6-pin PIC10F microcontroller shines.

The line-up

The PIC10F family of 8-bit Flash microcontrollers debuted in June 2004. The family features are shown in Table 1.

The PIC10F family also features the following:

- Each MCU is equipped with a 4 MHz internal oscillator that is factory calibrated to $\pm 1\%$ and is accurate to within $\pm 2\%$ over voltage and temperature.
- The operating voltage for the PIC10F Flash microcontrollers is 2.0 to 5.5 V, allowing for flexibility and longer operating times in battery-powered applications.
- Programming the microcontroller can be done in production or while in the field via the PIC10F's In-Circuit Serial Programming™ (ICSP™) capability.

Why six pins?

So why did Microchip develop the PIC10F family of 6-pin microcontrollers? The answer is simple: Microchip believes that providing an ultra-low-cost and ultra-small-footprint microcontroller in a familiar form factor positions these microcontrollers as the next-generation electronic building block. Just as operational amplifiers have been the common building block for signal conditioning, Microchip believes the PIC10F will become a fundamental component in the embedded designer's toolbox.

Instead of browsing through millions of components in an attempt to find the right solution, a circuit designer can now reach for this versatile little SOT-23 packaged microcontroller that does exactly what he or she needs. All that is required is a few

lines of code and the PIC10F can do the job of many of other devices with much more flexibility. Instead of trying to make a square peg fit in a round hole, a designer can simply make his or her own peg.

A paradigm shift

A microcontroller is traditionally considered as the nerve center for an application. While the PIC10F can be the main microcontroller for simple applications, it really shines in applications where it replaces discrete components that condition signals or provide timing. In these applications, the 6-pin microcontroller is not the center of the design – it is on the periphery. Due to its small size and low price tag, a PIC10F can sit next to another microcontroller or ASIC, or it can replace the passive and active components that were traditionally

| Device | Program Memory | Data Memory | I/O | | Timers 8-bit | Comparator |
|-----------|----------------|--------------|-----------------|------------|--------------|------------|
| | Flash (words) | SRAM (bytes) | Input or Output | Input Only | | |
| PIC10F200 | 256 | 16 | 3 | 1 | 1 | 0 |
| PIC10F202 | 512 | 24 | 3 | 1 | 1 | 0 |
| PIC10F204 | 256 | 16 | 3 | 1 | 1 | 0 |
| PIC10F206 | 512 | 24 | 3 | 1 | 1 | 0 |

Table 1

used (such as resistors, capacitors, operational amplifiers, logic gates). The 6-pin PIC10F can generate waveforms, act as a timer or buffer, or implement many other designer desired functions.

Power-sequencing example

In this example, a PIC10F204 is used as a power-sequencing device (Figure 1). The purpose of this device is to power up different components on a printed circuit board (PCB) in a predetermined order so that everything is in-sync once the entire circuit is powered up.

In the example, a PIC10F204 powers up the main microcontroller with the GP2 power-enable line, and then powers up the FPGA with the GP0 power-enable line. The advantage to this system is that the main microcontroller is up and running before the remainder of the circuit. The pull-down or pull-up resistors that were previously needed to ensure the main microcontroller pins were in the right state upon start up are no longer needed because the main microcontroller is in full control of its faculties before any other part of the circuit is powered. The main MCU begins executing routines a short time after the FPGA is powered up.

This circuit also takes advantage of the wide operating voltage range of the PIC10F204 as it operates down to 2.0 V. Other components on the board, including the main microcontroller, may not run below 2.5 V. Note that R1, R2, and the onboard comparator create a

low-voltage-detect circuit. The R1 and R2 values were chosen so that the negative input terminal of the comparator sees 0.6 V when the supply voltage is 2.7 V. The positive terminal of the comparator is referenced to the internal bandgap voltage of the PIC10F204, which is fixed at 0.6 V. If the supply voltage falls to 2.7 V, the comparator trips. The PIC10F204 reads the comparator output voltage internally and, if it trips, the PIC10F shuts down the circuit in a specific sequence. In a variation of this example, the PIC10F204 could warn the main microcontroller of an imminent shutdown, giving the main microcontroller time to save vital information to RAM.

During power up, the PIC10F204 can perform this sequence in reverse. Again, because it operates at a lower voltage than most other microcontrollers, the PIC10F204 powers up and then monitors the supply voltage until a suitable voltage level is reached. At this point in time, the PIC10F microcontroller begins powering up the circuit.

Once the main microcontroller is up and running, the requirements for this particular design may dictate that the main microcontroller be able to reset the circuit. The line running from the main microcontroller to the GP3 input-only pin on the PIC10F204 enables this function. When the main microcontroller wants to reset the circuit, it simply toggles this reset line and the PIC10F204 takes care of the rest.

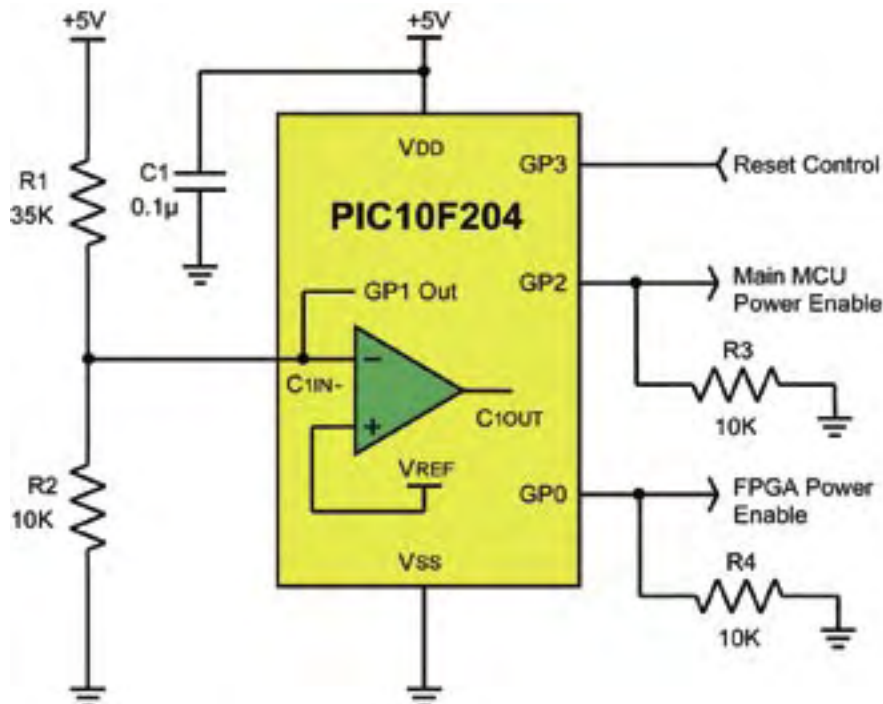


Figure 1

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One huge benefit to using the PIC10F is that, should the timing requirements or power-up sequence change, the PIC10F can be easily programmed in-circuit to accommodate these changes. A traditional, inflexible discrete solution would likely require a board redesign. With the inherent flexibility of the PIC10F, the time and expense of redesigning the PCB is avoided and time-to-market is significantly reduced.

Soft-start controller application

A PIC10F204 may be used as a soft-start controller for a switching power supply. Switching power supplies use an analog feedback system in order to generate a constant output voltage. On startup the output is zero, therefore the initial feedback error is at its maximum. In response to this, the power-switching transistors are driven at their maximum rating until the output voltage approaches the nominal level.

In this example, a PIC10F202 is used to provide a soft startup for the switching

power supply (Figure 2). The only necessary changes to a traditional switching power supply's hardware are the addition of the PIC10F202, one 0.1 uF bypass capacitor, and a 10 k pull-down resistor. As shown in Figure 2, pin GP1 is tied to the shutdown control of the switching power supply IC, or to the enable control on the power-drive section.

The PIC10F202 generates a PWM output on pin GP1 when the control input is enabled. The PWM signal is ramped from 0 to 100% over a period of time, which ensures that the power-driver section does not undergo a lot of stress. The power stage of the supply is run at its maximum rating, but not continuously. When the control input falls to zero, the microcontroller shuts down the supply, and waits to begin the startup routine over again.

The implementation of soft-start control can be used in other control systems that also benefit from this functionality. Changing the timing of the soft-start routine is as simple as modifying the firmware. Simple motor-control systems, for example, may benefit from the addition of a soft-start controller in line with the power stage. The speed of the motor can be ramped up on startup to limit the initial startup current in the power stage. The power stage for driving a motor often must be oversized to handle this initial startup current. By limiting the startup current, smaller components can be used, thereby reducing the overall cost of the system without sacrificing longevity.

Flashlight application

One of the biggest impacts of the PIC10F is in the world of mechatronics, where it can be used to enhance or replace mechanical components. Mechanical components are very susceptible to environmental hazards like dirt, grease, temperature changes, UV exposure, and corrosion. Replacing or reducing the amount of mechanical components in a given system is beneficial because these components are prone to wearing out over time. Migrating to a mechatronic solution may also provide cost savings over the life of a product, when the cost of warranty repairs is factored in.

The previously mentioned paradigm shift also applies to mechatronics. The key is to think simple. Take a mechanical three-position pushbutton switch, for example. This type of switch is found in hybrid flashlights, where it commonly toggles between powering a xenon bulb, powering three LEDs, or powering down. This mechanical switch works much like the mechanism in a retractable ballpoint pen. Every button press generates a rotary


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Some possible features include the following:

- Once a mode is selected for a certain period of time, the next button press will turn off the switch.
- The switch can learn which of the three settings the user prefers the most and make this the first option to the user when the user turns the device on.
- A strobe mode can be added that blinks the LEDs in an emergency situation.
- Dimming capability or current control can be implemented by pulse width modulating the output to the lighting elements.

The reprogrammable PIC10F202 allows the same hardware to perform a completely different function after it is reprogrammed. One intelligent PIC10F switch can perform the function of numerous mechanical switches. This saves money on retooling and provides end-product conformity.

The hybrid-flashlight example also highlights another important feature of the PIC10F microcontrollers, ultra-low sleep current. The PIC10F microcontrollers have a sleep current of just 100 nA. In the intelligent switch example, the PIC10F only needs to be awake when the switch is pushed. The microcontroller wakes up anytime it receives input on GP3, then performs its task and goes back to sleep.

A cost comparison between the mechanical and mechatronic switches illustrates that a mechatronic solution does not have to be a lot more expensive. In low quantities, a three-position push-button switch costs nearly \$1. By comparison, the intelligent switch costs just over \$1 for the microcontroller, tactile switch, PCB, and additional passive components. In large quantities the price difference becomes even less pronounced. With the added reliability, functionality, and flexibility of the intelligent switch, which one would you choose for your design?

Disposable application

The small size and cost of the PIC10F makes it an ideal candidate for use in disposable electronics. The PIC10F devices are excellent candidates for intelligent, disposable electronic applications such as medical devices. Disposable medical applications range from emergency blood-glucose monitoring kits to one-time-use pregnancy testers. In these applications, the resistivity of a testing material that reacts with a specific protein or substance in body fluids can be measured by implementing an ultra-low-cost, delta-sigma analog-to-digital converter. A circuit implementing

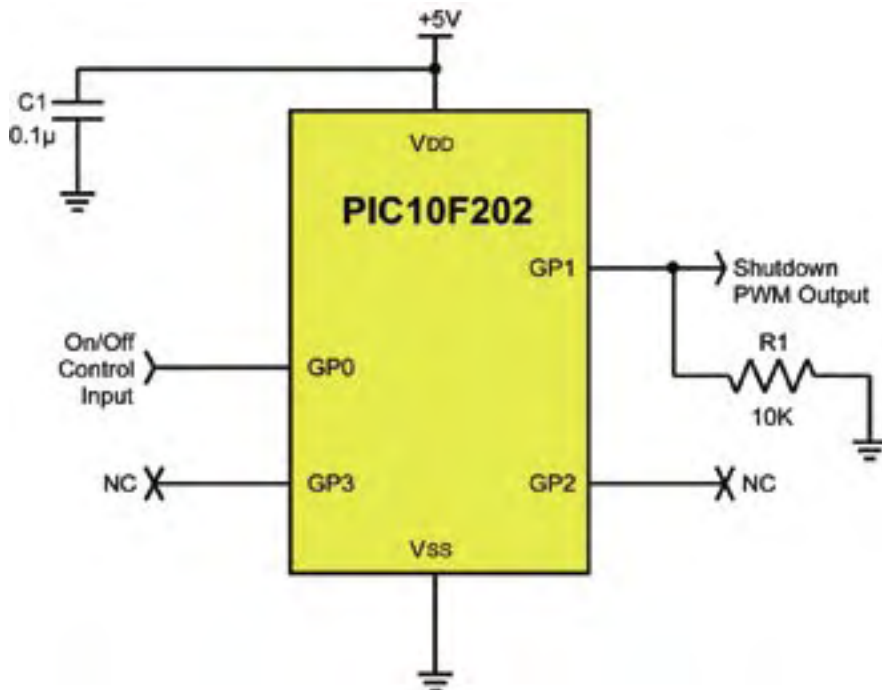


Figure 2

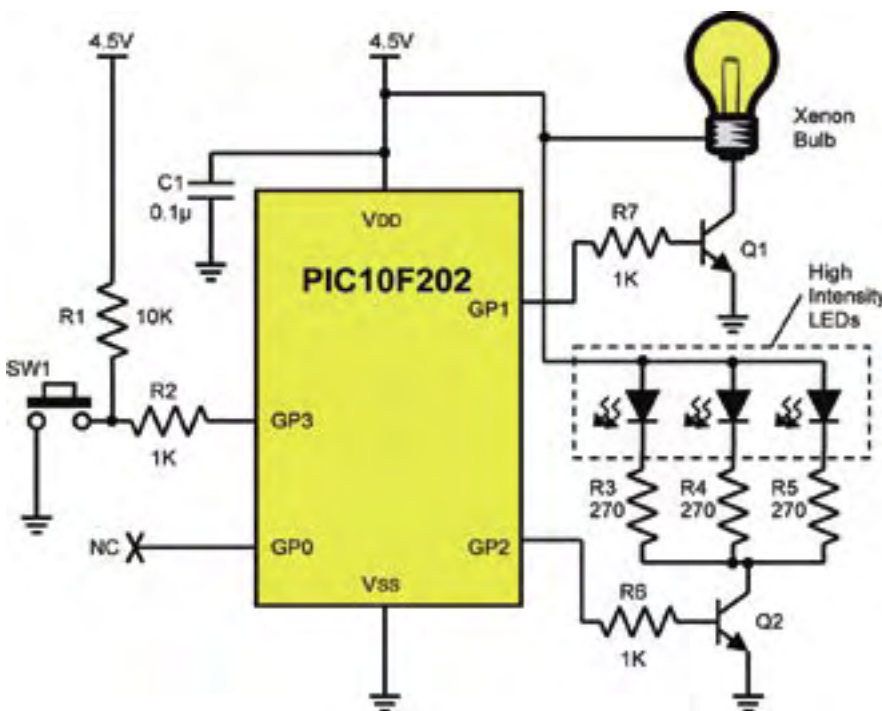


Figure 3

motion on a disk encircling the push button. As the disk turns, contact is made between the common and one of two contacts, or none at all. This solution works well, but its functionality is fixed and it is prone to failure over time.

In this example, a PIC10F202 is used in a switch application (Figure 3). This implementation uses a sealed tactile switch as an input. A firmware debounce routine

ensures that the microcontroller does not get a false reading due to contact jitter in the switch. Just as with the purely mechanical switch, the PIC10F202 can cycle through the different lighting elements until the user selects the desired element.

The manufacturer of this intelligent switch can customize the switch with different features by using the In-Circuit Serial Programming capability of the PIC10F202.



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this analog-to-digital converter is shown in Figure 4.

In this implementation, GP1 is briefly configured as a comparator input at precise time intervals, where the comparator output is read internally and then GP1 is immediately configured as an output. The state of GP1 is set to reflect the comparator output. To perform an analog-to-digital conversion, the duty cycle must be integrated over time. This is done digitally with two software counters. One counter keeps track of the number of times the comparator output reads low, and the second counts the number of samples. The ratio between these two counters is equal to the ratio of the input over V_{CC} . The resolution of the conversion is proportional to the number of samples. The greater the number of samples taken, the higher the resolution of the analog-to-digital conversion.

Identification application

Another emerging disposable electronics market is property identification devices. A unique serial number can be programmed into the Flash memory of a PIC10F and then retrieved from the device in a variety of ways. The PIC10F microcontroller can be powered remotely by charging a coil via an electrical field, which is similar to how a RFID device is powered.

Conclusion

The PIC10F family of microcontrollers is breaking new ground by offering the

intelligence and flexibility of an 8-bit Flash microcontroller in the smallest microcontroller package ever. To be sure, these 6-pin microcontrollers are ideal for mechatronic and disposable applications, as well as for applications where they replace discrete components. Sitting peripherally to the main microcontroller, the PIC10F can perform a variety of tasks that would otherwise be too expensive to consider, or would require numerous components that do not offer design flexibility. The wide number of applications for these microcontrollers remains to be seen. The possibilities seem endless. It just goes to show that sometimes really big things come in small packages. **ECD**

Reston Condit is an applications engineer at Microchip Technology Incorporated, where he has worked since 2000 in the Security, Microcontroller and Technology Division. Reston holds a Bachelor of Science degree in Electrical Engineering from the University of Arizona.



For more information, contact Reston at:

Microchip Technology Inc.

2355 W. Chandler Boulevard
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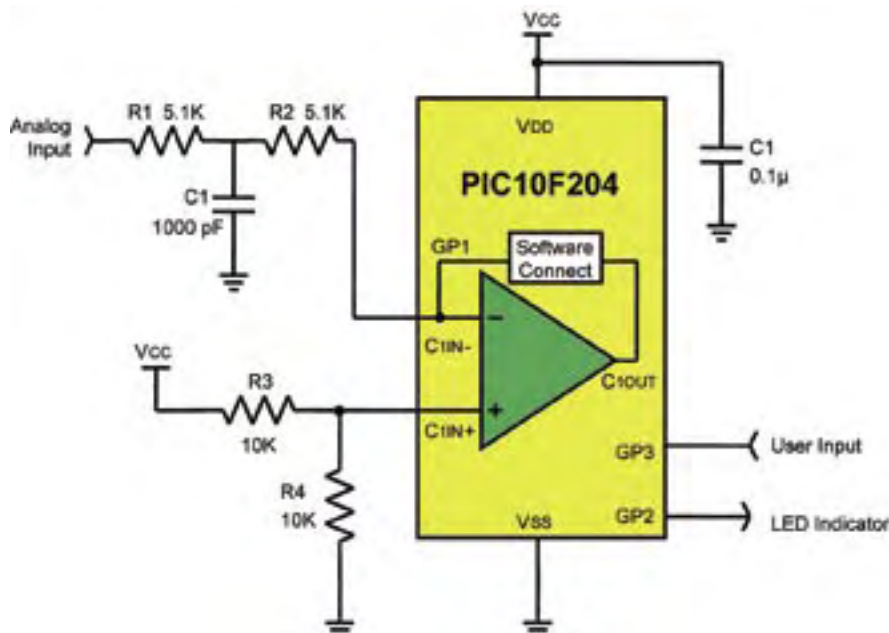


Figure 4

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PCI Express and Non-Transparent Bridging support High Availability

By Akber Kazmi

In the last ten years, Internet technology has dramatically extended the reach of businesses and consumers around the world. Business dependency on the Internet infrastructure, along with computer systems and their around-the-clock availability, has accordingly increased. Large amounts of data stored on distributed storage devices are being accessed by users spread around the globe, using many different applications while demanding 24/7 service availability.

In the early days of computing, tape backups at the end of the day were sufficient to guarantee data availability. Today's high availability challenges require new approaches. Industry has now adopted solutions that breakdown the data availability task into smaller sub-tasks.

Well defined components

In order to support high availability, all components involved in a particular service or application must be understood. At the highest level are the software elements that deal with the availability of the applications, and the data utilized by these applications.

Another set of elements consists of the hardware that provides the means to store the data, run the applications, and connect them together (such as servers, routers, hosts, switches, and gateways). The hardware that provides this infrastructure may consist of individual modules (for example I/O blade, fabric, and controller) interconnected together to form a system or cluster of systems. Furthermore, the robustness and reliability of each component within a module play a key role in defining the availability of the system.

High Availability and PCI Express

This article will discuss general concepts of High Availability (HA), and then focus on the use of PCI Express technology to support High Availability of the hardware elements used in most common applications.


It will also explore the use of Non-Transparent Bridging (NTB) as one of the key enablers of PCI Express usage in this application.

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Furthermore, it will highlight the use of Quality-Of-Service (QOS) features of the PCI Express technology that enables traffic prioritization to guarantee availability of the system resources for high-priority applications and data.

What is High Availability?

A frequent measure and term used for high availability or service availability is the expected amount of time, measured as a percent, that a service or equipment is available to serve the user/application. The 99.999 percent (5-nines) availability standard specifies 24/7 service with a maximum of five minutes of downtime in

a year. A typical desktop without 5-nines reliability may tolerate nine hours per year of unavailability, but a carrier-class switch or server would require support for 5-nines availability.

Generally, service availability depends heavily on the fault tolerance of the system, including hardware redundancy. The software components of the system use the redundant hardware to enable the service and application availability.

Redundancy

In complex systems such as routers, storage systems, and application servers,

multiple intelligent devices are employed to perform various tasks. It is important that these devices interact with each other without causing resource contentions, or access conflicts. The task of connecting these devices becomes much more challenging when they are expected to support redundancy.

As described in the *Providing Open Architecture High Availability Solutions* white paper published by the HA Forum, system redundancy can be divided into the following three categories, or classes:

- **Structural redundancy:** This involves modifying the information being exchanged or transferred, such as adding Error Checking Codes (ECC) to verify that the information transferred from one device to another was received without loss or errors.
- **Temporal redundancy:** This involves use of time or system bandwidth to achieve availability, such as using handshakes or NAK/ACK messages to confirm or acknowledge reception of error-free data.
- **Spatial redundancy:** This involves availability of more resources than needed in a normal mode of operation, such as hot spares, and spare link/connections to system resources. This may involve 1+1, 1+N, N+M redundancy, and load sharing.

In today's complex systems, support for high availability is as challenging as ever. Economic challenges do not allow for the development of custom solutions. COTS (Commercial Off-The-Shelf) solutions must be used to be cost competitive. Vendors are forming alliances and industry groups to create an ecosystem, where they can rely on solutions that are based on standard implementations with off-the-shelf availability.

PCI Express technology

PCI Express technology is an emerging interconnect standard. PCI Express is suitable for chip-to-chip, board-to-board, backplane, and box-to-box interconnect for high-performance systems through PCI Express cables. It is an evolution of the PCI standard and is fully backward-compatible with the PCI software structure.

PCI Express is based on a layered architecture, which takes advantage of developments in high-speed serial communication technology. The protocol stack provides three layers:

- **Physical layer:** Consists of an Low-Voltage Differential Signaling (LVDS) high-speed serial interface specified

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for 2.5GHz signaling with 8B/10B encoding and AC-coupled differential signaling. A set of LVDS pairs is called a *lane*, and PCI Express allows lane combinations to form bigger and wider ports, such as x1, x2 and so on up to x32. The physical interfaces support hot-plugging.

- Data link layer: Supports packet exchange between neighboring PCI Express entities with data integrity and sequence check, along with packet acknowledgments and flow control.
- Transaction layer: Translates data read/write requests from a host or an end device and optionally provides transaction layer (end-to-end) packet integrity check (CRC-32).

The PCI Express protocol stack is shown in Figure 1. In addition to a well-defined robust protocol stack, PCI Express supports QoS through the use of eight Traffic Classes (TC), eight Virtual Channels (VC), mapping of TCs on VCs, and VC arbitration schemes.

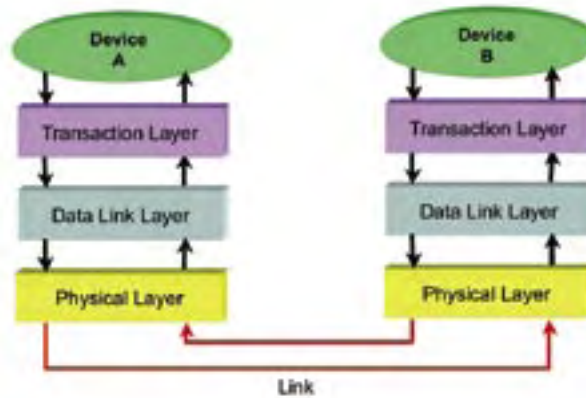


Figure 1

The PCI-SIG, the standards body responsible for the PCI Express specification, has also developed a specification to enable bridging of the PCI/PCI-X bus to the PCI Express serial interface. This would allow many existing applications that use PCI/PCI-X to smoothly migrate to PCI Express. Figure 2 represents a generic use of the PCI Express components such as a

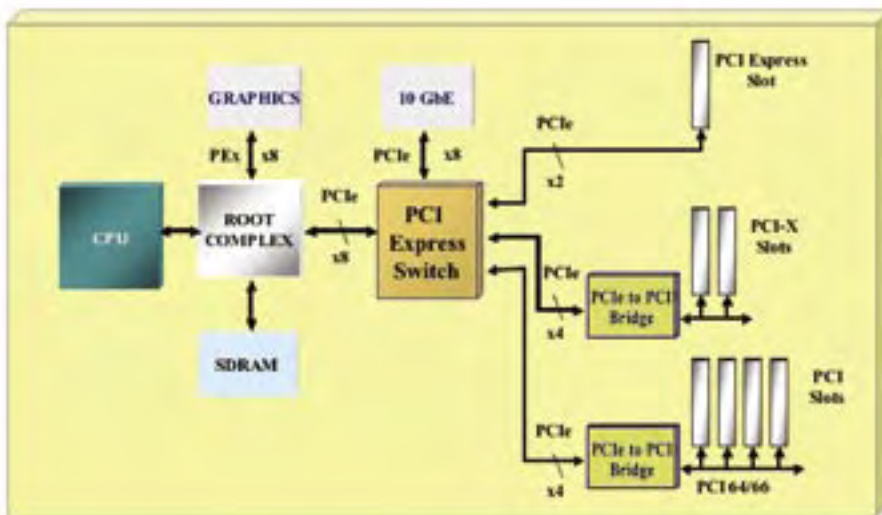


Figure 2

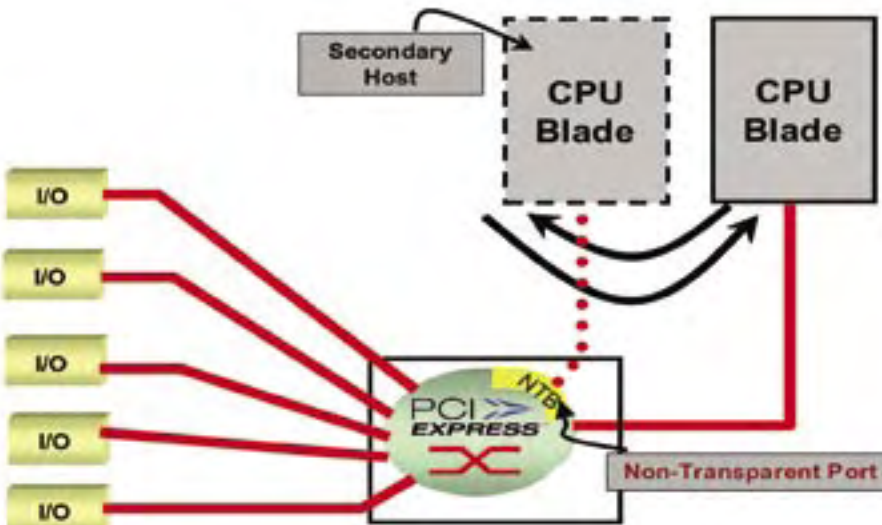


Figure 3

root complex, a switch, bridges, and a native PCI Express device.

Non-Transparent Bridging

As with PCI and PCI-X, PCI Express was developed with the objective to maintain a host-centric architecture. However, users have developed ways to support PCI Express platforms in a multi-host environment using the non-transparent bridging

function, which PCI and PCI-X have used for years.

A non-transparent bridge is functionally similar to a transparent bridge, with the exception that there is an intelligent device or processor on both sides of the bridge, each with its own independent address domain. The host on one side of the bridge will not have the visibility of the complete memory or I/O space on the other side. Each processor considers the other side of the bridge as an endpoint, and maps it into its own memory space as such. The use of NTB in a CPU redundancy (active/standby) application is shown in Figure 3.

In the NTB environment, PCI Express switches translate addresses that cross from one memory space to the other. The NTB also allows hosts on each side of the bridge to exchange information about their status through scratchpad registers, doorbell registers, and heartbeat messages. Scratchpad and doorbell registers are readable from both sides of the bridge,

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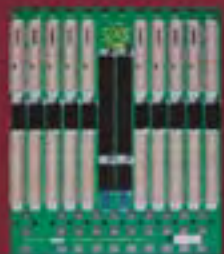
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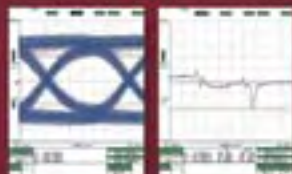
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and can be accessed as memory or I/O. Doorbell registers provide a mechanism to generate software controlled interrupts and heartbeat exchanges.

PCI Express in High Availability systems

PCI Express technology complemented by NTB provides valuable features that support high availability applications. PCI Express technology supports the three classes of system redundancy discussed earlier.

Structural redundancy

Structural redundancy involves changing the structure of data moving between entities of a system to support integrity of data exchange. In most communication protocols a checksum, or error-detection code, is appended to a packet or block of data being exchanged. PCI Express provides two levels of structural redundancy as shown in Figure 4:

- Data link layer: 32-bit LCRC (Link Cyclic Redundancy Check) between two neighboring devices.
- Transaction layer: 32-bit ECRC (End-to-end Cyclic Redundancy Check) between two devices separated by one or more entities.

Support of data scrambling and encoding of the embedded clock in the data stream adds another level of structural redundancy for links that use PCI Express as the interconnect technology.

PCI Express allows bandwidth scaling by use of multiple lanes to establish wider data paths. The specification allows wider ports to scale down in order to provide service at a reduced level in case of a failure of one or more lanes. For example, if a port is providing an x4 (2.5Gbps x4) path between two entities and one or more lanes fail, the port would automatically scale down to x2 or x1 to sustain some level of service or availability.

Temporal redundancy

Temporal redundancy involves a handshake mechanism where a receiving

entity sends acknowledgement of error-free data reception or error messages if data corruption or loss is detected. The PCI Express specification provides mechanisms for the receiving entity to generate positive/negative acknowledgements to inform the sender about the integrity of the data packets received.

Congestion avoidance is a common mechanism used in communication networks to handle overloading of the system. In addition to providing acknowledgement for packets, PCI Express components provide information to the sender about the availability of buffer space reserved for specific flows (virtual channels). This mechanism, called *credit-based flow control*, can be used to implement efficient use of buffer resources and to avoid the congestion by backpressuring the source of the data.

Another method of avoiding congestion is to dedicate system resources such as bandwidth for high-priority flows (applications). In a PCI Express system, mapping of traffic classes to virtual channels allows the host to dedicate port bandwidth for high-priority traffic. This enables efficient management of system resources, and implementation of quality of service based on the priority of traffic and associated virtual channel.

Spatial redundancy

Spatial redundancy is one of the most talked about subjects in regards to implementing high availability. In this class, one or more elements of the system are duplicated with one or more backup elements providing a similar function. This allows assigning redundant resources to a particular task, or the creation of multiple paths between two end devices, thus guarding the system against a single point of failure.

Although PCI Express does not provide a specific solution to address spatial redundancy, innovative developers and users of PCI and PCI Express technology have invented ways to overcome this challenge. Companies such as PLX have created an NTB implementation for the

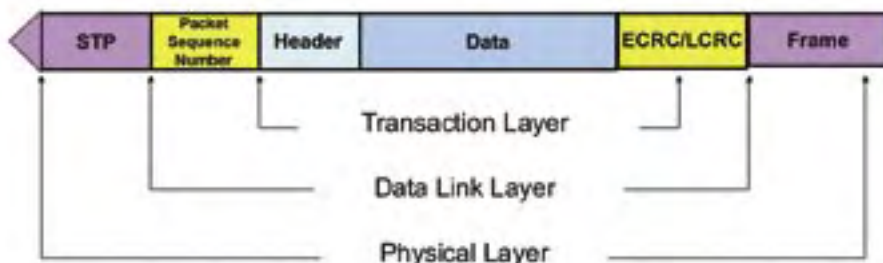


Figure 4

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PCI Express applications, which is similar to that of PCI usage models. As discussed earlier, NTB allows two processor or memory domains to be isolated from each other, and yet facilitate limited access for one processor to the other processor's domain (memory & I/Os).

The NTB function in the PCI Express switches would allow the system designers to use multiple CPUs, redundant switch-fabric modules, and intelligent I/O subsystems in a single system. The NTB feature can also be used to create a star, dual-star, or meshed switch fabric with PCI Express switching components. Of course, PCI/PCI-X-to-PCI Express bridges with the NTB function can be used to implement redundancy for the PCI-based modules. An example of NTB function use in a high availability application where a redundant host and switch fabric are required is shown in Figure 5.

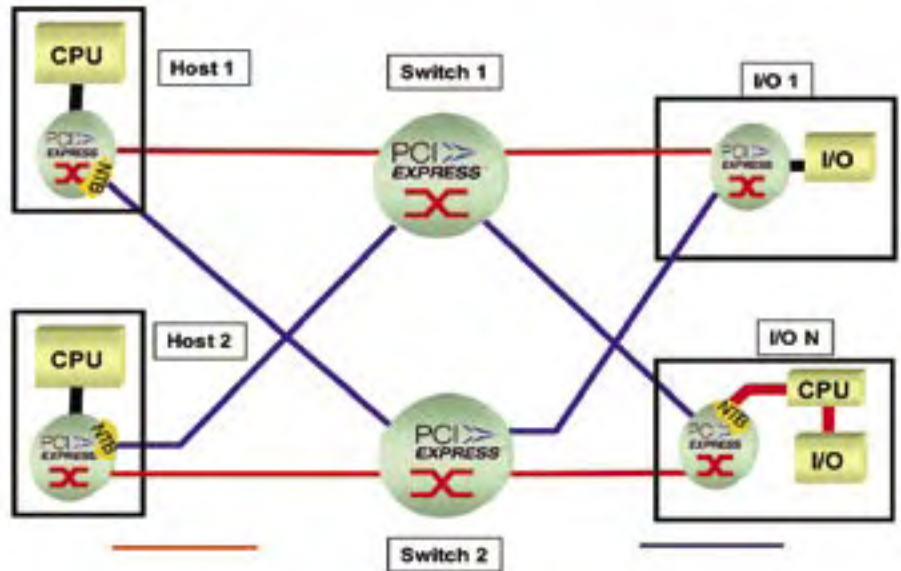


Figure 5

This example shows two active CPUs (hosts) communicating with a number of I/O modules through two active switch fabric modules operating in a dual-star configuration. Each CPU module has an active link (shown in red) to one of the switch-fabric modules and a backup (shown

in blue) link to the other switch fabric. This configuration provides redundancy for CPU modules, switch fabrics, I/O modules, and the links connecting them. The I/O modules may contain standard I/Os or embedded CPUs isolated with the aid of NTB ports on the switch. The usage model illustrated

here can be modified to support 1+N host redundancy or meshed switch fabric.

Summary

High availability is a crucial element of global 24/7 service availability for the Internet, and while there are many elements that make overall service availability possible, hardware redundancy plays a key role. PCI Express technology is the emerging solution for chip-to-chip, board-to-board, backplane, and system interconnect. Complemented by non-transparent bridging, PCI Express offers robust architecture and rich features for hardware redundancy that allow for the development of high availability systems with commercially available PCI Express switch and bridge components. **ECD**

Akber Kazmi is Senior Marketing Manager at PLX Technology, and is responsible for the PCI Express switch product line. Kazmi has more than 15 years of marketing experience, with an emphasis on the communications market. Kazmi holds an MSEE from the University of Cincinnati, and an MBA from Golden Gate University.



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High Availability application ready platform design

After the downturn of the last several years, the telecom market is bouncing back and is once again cautiously expanding converged and wireless networks. There is a new and growing demand from consumers and corporate customers for converged voice and data services. This has challenged the Telecom Equipment Manufacturers (TEMs) to provide new and innovative services at unprecedented costs and schedules.

The challenges faced by the large TEMs today are unique because their staff size is not tracking their business growth due to the massive staff reductions of the past few years. With tight budgets, aggressive schedules, and precious few resources, the TEMs must make tough development resource choices.

By Asif Naseem

Competitive pressure

The emergence of services using IP has brought unconventional players to the market, such as fast and nimble startup companies. This is intensifying the competition, and forcing TEMs and service providers to come up with new development and deployment strategies that enable them to quickly bring cost effective applications and services to the market.

Traditional platforms

Service providers generate revenue from applications and services that run on platforms generally provided by the TEMs. A high level

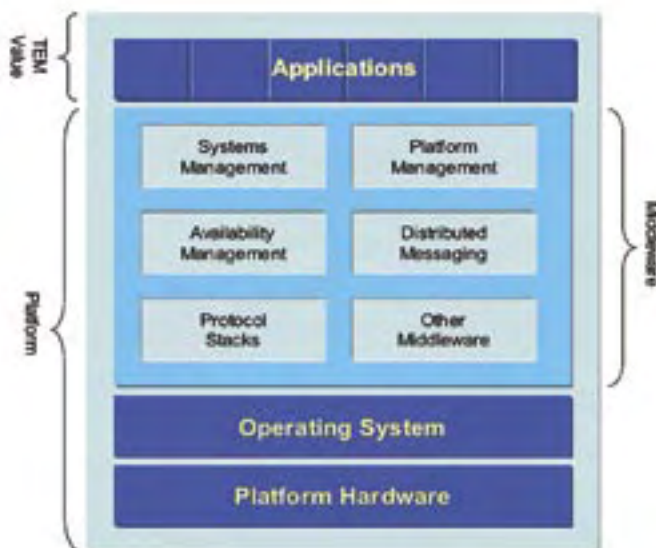


Figure 1

view of a platform consists of the following four layers shown in Figure 1:

- Applications
- Middleware
- Operating System
- Platform Hardware

The lower three layers represent a platform that must be built or acquired before the end-user applications in the top layer can be developed and deployed.

Proprietary platforms

Traditionally, large equipment manufacturers have invested enormous resources to build in-house hardware and middleware for proprietary platforms.

While such implementations address the specific requirements of a particular application or service, they require significant rework each time change is introduced in the hardware, the operating system, or the application. This makes the reuse of most of the functionality layers very costly, time consuming, and risky. Even though TEMs recognized the large costs and efforts involved, they were forced to build proprietary platforms due to the lack of Commercial Off-The-Shelf (COTS) components that were standards-based, pretested, and pre-integrated.

Proprietary platform projects have invariably faced the following challenges:

- Long development and integration cycles due to proprietary function development, and third party and legacy component integration.

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- Product commercialization cycles that are measured in years (2–3 years for a major release), when the market demands a much faster time-to-market (12–18 months).
- Missed deadlines caused by underestimated development and integration tasks.
- Competitive price pressures due to late market introduction, and high development cost.

Paradigm shift

In the last few years, market realities have led to a paradigm shift that has changed the way TEMs address these challenges. Now, the following efforts are taking place:

- Third party integration: Tight budgets, aggressive time-to-market requirements, increasing cost pressures, and fewer resources have led the TEMs to integrate third party hardware and middleware into their platforms.
- Standardization: Several new and emerging standards allow designers to build systems by combining a set of interoperable COTS building blocks from a variety of competing vendors. Numerous industry consortia are addressing the standards associated with the layers shown in Figure 1.

Application ready platform

Once a TEM has integrated third party and standardized COTS components into their platform, they are free to concentrate on revenue generating application development.

To quickly integrate, a TEM can acquire an *application ready platform* with pre-integrated hardware, middleware, and third party components. Each platform is pretested to ensure that it meets the TEM's most stringent requirements.

High availability

An application-ready platform must meet strict High Availability (HA) requirements before it is deployed in a mission or business critical application. Most mission critical applications require a system uptime of 99.999% (a downtime of less than five minutes per year) or better.

To ensure continuous operation and uninterrupted service, the application-ready platform designers must identify all potential single points of failure in the service path, and then implement methods to eliminate them. A comprehensive approach to designing a high availability application-ready platform includes:

- The upfront determination of key availability and performance requirements.
- The definition of a system architecture that supports key build vs. buy decisions, and leverages COTS elements.
- A special focus on key high availability attributes.

We now will examine the three development points.

Requirement determination

Careful upfront planning is required when you determine availability and performance requirements for the desired service, and when you allocate an appropriate budget for each required subsystem for the service.

One of the fundamental requirements of a highly available system is to minimize, if not eliminate, the time it takes to return the system to an operational state following a failure. This requires the definition of efficient availability services, which execute at a sufficient speed so a service interruption is imperceptible to the user.

For example, to support continuous service in a wireless network, failure recovery must take place in less than 50 ms. Restoring a system to an operational state following a failure is a multistage process that involves fault detection, diagnosis, isolation, recovery, repair, and reconfiguration. For our wireless network example, each recovery stage must be allocated a performance budget so that the total recovery process completes in less than 50 ms.

Modern communication systems often consist of multiple nodes connected in a cluster. This topology allows designers to include redundant nodes in the cluster that can take over operation of other nodes in the event of a failure. Collectively, these nodes work as a unit to provide a variety of communication services, and they must therefore have the capability to send and receive messages at very high speeds (such as event notifications, heartbeats, alarms, or application state information).

Such a messaging mechanism must provide efficient means of storage, retrieval, and transmission of real-time information within a node and across the cluster. For example, to support an uninterrupted wireless communication service, the messaging system must support anywhere from 10k–50k messages per second depending on the message size. These performance requirements often demand that an efficient in-memory data-store is used by the system for storage and retrieval of real-time information.

System architecture definition

In the 1990's, the computer industry transitioned from vertically integrated systems that were primarily offered by individual system vendors, to modular computing where an enterprise or an end-user can purchase COTS components from different vendors and put together an operational system with relatively little effort.

The telecom industry is beginning a similar transition and faces several challenges. Traditionally, hardware and middleware – in addition to the core communication applications – were considered as TEM market differentiators. As plentiful development resources were at-hand, most large TEMs pursued programs to implement most, if not all, of the system functionality in-house.

Recently, however, several important trends – especially on the standardization front – are causing the telecom industry to consider adopting similar system design approaches as the computer industry.

For example, PCI Computer Manufacturing Group (PICMG), a consortium of several companies including TEMs, develops and promotes carrier grade equipment standards. A more recent set of specifications, AdvancedTCA, is quickly gaining wide industry acceptance. It

primarily targets telecommunication application developers, and defines new architecture standards designed for integration ease and the migration of telecom applications across platforms.

The Open Software Development Laboratory (OSDL) is an industry body dedicated to accelerating the adoption of Linux for enterprise computing and carrier applications. The Carrier Grade Linux (CGL) working group of OSDL is defining feature roadmaps and specifications for use in telecommunications architectures.

The Service Availability Forum (SAForum) is a vendor consortium that develops and promotes standard specifications that allow for easy interoperable middleware COTS component integration.

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These specifications and standards facilitate the portability of middleware and applications across multiple platforms, and therefore reduce the startup cost and the integration effort.

The proliferation of the platform standards enables designers to rapidly build application-ready platforms that utilize various COTS building blocks as shown in Figure 2.

This allows the equipment vendors to minimize the cost and effort involved in building a platform, and allows them to focus their resources on their core competence – communication applications.

The intended system architecture must take into consideration these market trends and realities. Well designed system architecture meets service availability, cost, and schedule requirements, and the modular design of the system allows for future changes and/or replacements of modules without risking enormous cost and effort.

“The development of an application-ready platform that will provide uninterrupted service availability is an arduous task that involves complex hardware and software.”

High availability attributes

The development of an application-ready platform that will provide uninterrupted service availability is an arduous task that involves complex hardware and software.

Our experience shows that such systems evolve over multiple releases until they are able to meet the most stringent service availability requirements. Some of the most critical attributes that characterize these highly available systems are:

- the ability to thoroughly model various resources in the platform
- comprehensive high availability services
- an efficient messaging engine

The combination of these attributes with effective system management yields an application-ready platform that will ensure uninterrupted service availability.

System modeling

The system modeling capability provides a mechanism to represent physical and logical resources that make up the overall system. It also defines the relationships and dependencies among such resources in a hierarchical network of managed objects. These

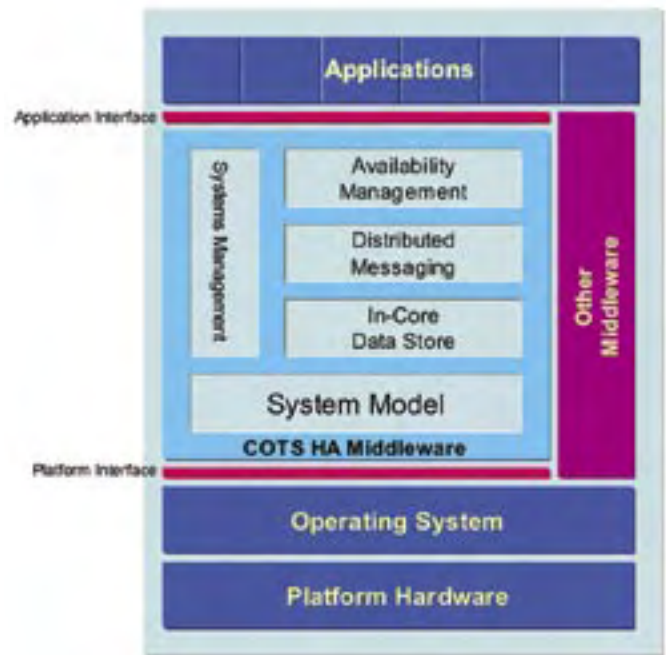


Figure 2

objects have states and attributes that represent the actual and desired state of the corresponding physical resource.

The systems model has the capability to group sets of like objects into service groups and then define respective recovery policies for each group that are executed in the event of a failure. Any change in the state of the objects that can affect service availability (such as a failed application, a hardware error, or planned downtime) causes an update to the systems model that in turn triggers the appropriate recovery action to maintain the overall service availability.

High availability services

High availability services manage resource failures without interrupting service. Such services are responsible for providing seamless switchover among redundant components, masking the end-user from any faults or resulting failures. High availability services must support a large number of nodes in a cluster, with the ability to collect, preserve, and distribute application state information for stateful, seamless failover between the nodes in the cluster. Key functions provided by high availability services include the following:

- The creation and maintenance of availability management information.
- The availability engine that applies policies to proactively manage the system for high availability, often 99.999% or better.
- The management of the various parts of the system, such as nodes in a cluster or redundant components.
- Checkpointing services to applications and other components.

Messaging engine

A messaging engine is designed to address the need for communication between the different elements within an application-ready platform. Such an engine provides an efficient mechanism for communicating a wide variety of information such as application state information, event and error notification, or fault management information. A messaging service provides an effective way for distributed components to efficiently communicate and coordinate their activities. Instead of requiring each resource to manage its various communication complexities, the messaging service does it for them.

A messaging service must be flexible, scalable, and reliable:

- Flexibility requires that the messaging service is independent of the applications it provides services to, so that the communication responsibilities can be offloaded from the applications.
- Scalability ensures that the messaging service is architected to support change and growth in the system components, and to support increased messaging activities. Applications do not need to be modified as the system and message volume changes or grows.
- The messaging service must be reliable to ensure message delivery, even in the event of failures in the primary network connection.

Last thoughts

With the emergence and adoption of new standards and the availability of COTS hardware and HA software, the developers of application-ready platforms that are intended for business critical applications (wireless communication for example) no longer have to develop proprietary functionality in-house to meet uninterrupted service requirements.

They can choose from field-tested and hardened middleware product suites that can easily be integrated on a variety of standards-based commercial hardware platforms and operating systems. This allows them to focus their energies and resources on developing core functionality that provides them with key competitive differentiation.

Companies can significantly reduce their costs, risks, and time to market through the establishment of high availability requirements, the use of COTS building blocks, and the use of a progressive systems development approach.

GoAhead Software

Over the past several years, GoAhead Software has helped both large and small TEMs build core functionality with their SelfReliant suite of products. This suite provides high availability, distributed messaging, and embedded systems management – the key components of highly available application ready platforms. These standards-based products have been field tested and hardened through worldwide commercial deployments. **ECD**

Dr. Asif Naseem is the Senior Vice President and CTO for GoAhead Software. He has more than 18 years of experience in the computer and communications industries. Dr. Naseem has an M.S. in Electrical Engineering and a Ph.D. in Computer Engineering from Michigan State University.



For more information, contact Dr. Naseem at:

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Complementing high MTBF systems with Built-In Test:

The role of deployed test in mission-critical systems

By Andy West

You wouldn't buy a car, check the oil – then never check the oil again. Similarly, a mission-critical subsystem with the highest possible MTBF should be complemented by a strategy that verifies reliable operation in deployment. No matter how high the MTBF figure, it is always a finite, statistical quantity. A failure may still occur at any particular moment.

In the embedded market, system verification is typically implemented by test firmware that exercises the hardware during power-up and operation, and reports any anomalies to the application for the appropriate corrective action. In this way, anomalies are prevented from hiding until they occur during a moment of critical system use, when they might threaten the mission. And to continue the analogy: in the same way that not all cars are created equal, not all deployed test firmwares are created equal. But first, a little history...

MIL-HDBK-217

MIL-HDBK-217 (Reliability Prediction of Electronic Equipment) was created by the Department of Defense to establish and maintain consistent and uniform methods for estimating the inherent reliability of electronic equipment and systems, and has been widely used outside of the military environment.

The 217F handbook was published in December 1991, when the very large majority of solutions were proprietary. The developer of a system therefore had complete insight into the detail of all hardware and software elements, including Built-In Test (BIT), and could craft them to coordinate. Beyond that, the hardware would typically be application-specific and not generic.

COTS challenges

The advent of Commercial Off-The-Shelf (COTS) solutions has in many ways rendered MIL-HDBK-217 inapplicable. Hardware – such as a typical Single Board

Computer (SBC) – is now generic, as is the silicon that populates these boards. Detailed information on the internal logic of such parts is mostly unavailable.

It is also true that a COTS operating system is effectively a black box where the internal device and resource usage is unknown. As such, it cannot be disturbed by the intrusive testing that is typical of BIT. Even if operating system internals were known, they would only be known at a single point in time. While COTS operating system vendors are committed to maintaining the compatibility of the Application Programming Interface (API), they are not committed to maintaining internal structures or resource usage.

An intrusive test of any individual hardware component will almost certainly cause a complete malfunction of the operating system, which relies on the total machine state of the SBC. While this is generally not an issue for a BIT that executes before the operating system runs, it has significant

implications for continuous hardware confidence testing after the point at which the operating system and application start their execution.

Our test firmware approach

The COTS market requires a different approach to the design, implementation, and operational verification of test firmware. Radstone's methodology is holistic in that it encompasses not only a hardware confidence test at power-up that is provided via BIT, but also an ongoing hardware confidence test through Background Condition Screening (BCS).

Additionally, Radstone provides comprehensive facilities in these standard products that support system acceptance testing and extra, customer-designed confidence testing.

This article reviews some of the key characteristics of Radstone's approach to BIT, but it is important to note the vital role that BCS also plays in assuring confidence.

BIT relies on unfettered and exclusive access to system resources, allowing intrusive tests to achieve the highest possible confidence. BCS runs as a background operating system task, and is designed to be non-intrusive and non-destructive. This allows confidence checks to be maintained as the background task does not disturb the operating system.

Alternative approaches to continuous testing (such as allowing callbacks to destructive BIT tests) are questionable, even if an attempt is made to save and restore the key machine state variables around the callback. COTS operating system internals are unknown, and the functioning of the operating system may be disturbed. BCS is designed to work with the operating system, and it utilizes specific hardware partitioning for test purposes. Run in conjunction, BIT and BCS provide the maximum possible ongoing guarantee of hardware integrity.

Meaningful BIT coverage

If deployed test firmware is to preserve the mission from hidden failures, there must be very high confidence in their effectiveness. The magic word in the BIT world is *coverage*, a term that is meant to indicate

the percentage of possible board failures that are detectable (or *covered*) by the test. Coverage can be estimated in a number of ways, and some of the estimations are inappropriate for a COTS environment. The key is that coverage is only meaningful if it is within the context of a valid, known, and appropriate measurement system.

For example, it was once common practice to equate coverage with the number of gates exercised by the test. This made sense when low-density TTL chips prevailed – but makes little sense today where the vast majority of gates may be used for just one or two functions (such as memory or the processor). Similarly, with today's high density components, a simplistic exercising of the component will not generally reveal whether all of its gates are functional.

This method of establishing coverage evolved to a circuit analysis method, which recognized the growing importance of the printed circuit board itself, and the fact that the significant memory subsystem had its own built-in hardware strategies to cope with failure – Error Checking and Correction (ECC). Although not without its limitations, circuit analysis was well suited to the designs of yesterday and is still a

valuable tool today when determining the efficiency of BIT code.

Another past technique used standard reliability analysis figures to help determine test firmware coverage. This also has its place and drawbacks. For example, the failure rate predictions do not always align well with actual field failures.

Heavier coverage weighting is given to BIT exercised chips with higher estimated failure rates, generally over-emphasising those with a high gate count. This can lead to skewed coverage estimates. Some specific part use is not adequately taken into consideration. For example, edge connectors in the field may have a very significant failure rate, especially as they are exposed to inadvertent abuse, but the failure rate figures in use may not account for this.

There are numerous sources of reliability prediction data in the COTS silicon world, but they are inconsistent and tend to produce results more reliant on the chosen data than on real world performance. A further limitation of standard reliability analysis is that it inadequately addresses the impact of printed circuit board and solder joint reliability.

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Our BIT coverage approach

As discussed, COTS hardware and software has challenged the traditional measurement methods. Radstone provides reliability analysis figures (generally to MIL-HDBK-217) for our products, and this is useful data when considering the overall suitability of a particular board for a mission-critical application. However, our fault insertion/stuck nodes approach goes much further to prove BIT coverage.

The advantages of fault insertion are that the evidence it delivers is operationally real and entirely objective: a known fault exists – BIT detects the fault. This method has been used historically to verify BIT

operation in the industry, but generally only as an incidental audit, and with only a very small number of inserted faults.

Number of nodes

The challenge is to make the process statistically valid by testing a large and representative sample of faults (circuit board nodes are *stuck* High or Low to create faults).

A representative sample is achieved through the random choice of a large number of nodes. The question of *how many nodes* is difficult. The question is resolved with a standard formula which reveals the correct sample size for an appropriate level of confidence (Equation 1).

$$n = \frac{N}{(Nd^2 / t^2P(100 - P)) + 1}$$

Equation 1

where:

- n = necessary sample size
- N = total node population
- d = tolerance percentage
- P = coverage level percentage
- t = confidence level percentage

The *confidence level percentage* is directly related via the area under a normal distribution curve, to the confidence that the statistical result can be applied to the whole population.

An example

For this example, the board has a relatively low population of 5,000 nodes. The example values are:

- N = 5000
- d = 2.75%
- P = 95%
- t = 90%

The result of this calculation is that 164 random nodes need to be tested (n=164). Even this relatively manageable number of test nodes can pose a significant test challenge. Consider 164 nodes spread randomly across a high-density board with several large Ball Grid Array (BGA) devices.

Failure equivalence

A stuck nodes analysis does not directly address some fault types – for example, a faulty analog component or certain internal silicon failures. However, many failures of this type are covered by *equivalence*. For example, an SBC failure at a node that is not directly observed causes an observed node to be stuck elsewhere on the SBC. This results in the detection of an equivalent failure, and coverage of the fault in the analysis. The fact that these failures are not always directly detected does not affect the overall confidence factor in the result that describes the efficiency of the BIT.

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Where equivalence does not exist, Radstone BIT includes code that is specially targeted to provide additional coverage for such failure modes.

Radstone's BIT, therefore, has a statistically valid foundation and has been developed to deliver maximum customer confidence in the reliable operation of the board it tests, and Radstone's testing does not even stop with the board.

Beyond the board

Radstone's BIT philosophy incorporates the optional ability to test edge nodes (SBC nodes that lead off-board). This feature recognizes that BIT's true value is in real world deployed systems where an SBC may be connected to:

- USB
- serial lines
- SCSI hard drives
- Ethernet LAN
- external VME or PCI bus

This presents some difficulties, in that typical edge nodes do not have the predictable loop-back path of internal nodes. Nevertheless, although the connection path in which edge nodes participate is system dependent, it is normally still possible to verify many of them via the appropriate configuration of a range of standard Radstone tests.

For example, Radstone's BIT can access pre-configured areas of VME or PCI address space, and test the data capability at each address with various cycle types. This is possible on the majority of deployed systems including those with special test partitions. Other interfaces provide different challenges, but standard responses can be elicited from a few interfaces (for instance Ethernet ping and SCSI ID replies).

Edge node coverage is also increased by tests that transmit data and expect it to be echoed back in the same or an altered form. Use of the altered form requires a minimal integration effort. If some of these tests are inappropriate to certain connections during deployment, they need not be enabled. However, within the more flexible environment of an acceptance tester, the full range of options can usually be applied, obviating the need to develop separate acceptance test software.

Conclusion

In summary, Radstone's approach to deployed test is an extremely comprehensive one, providing maximum assurance both at start-up (via BIT), and with application execution (via BCS). It

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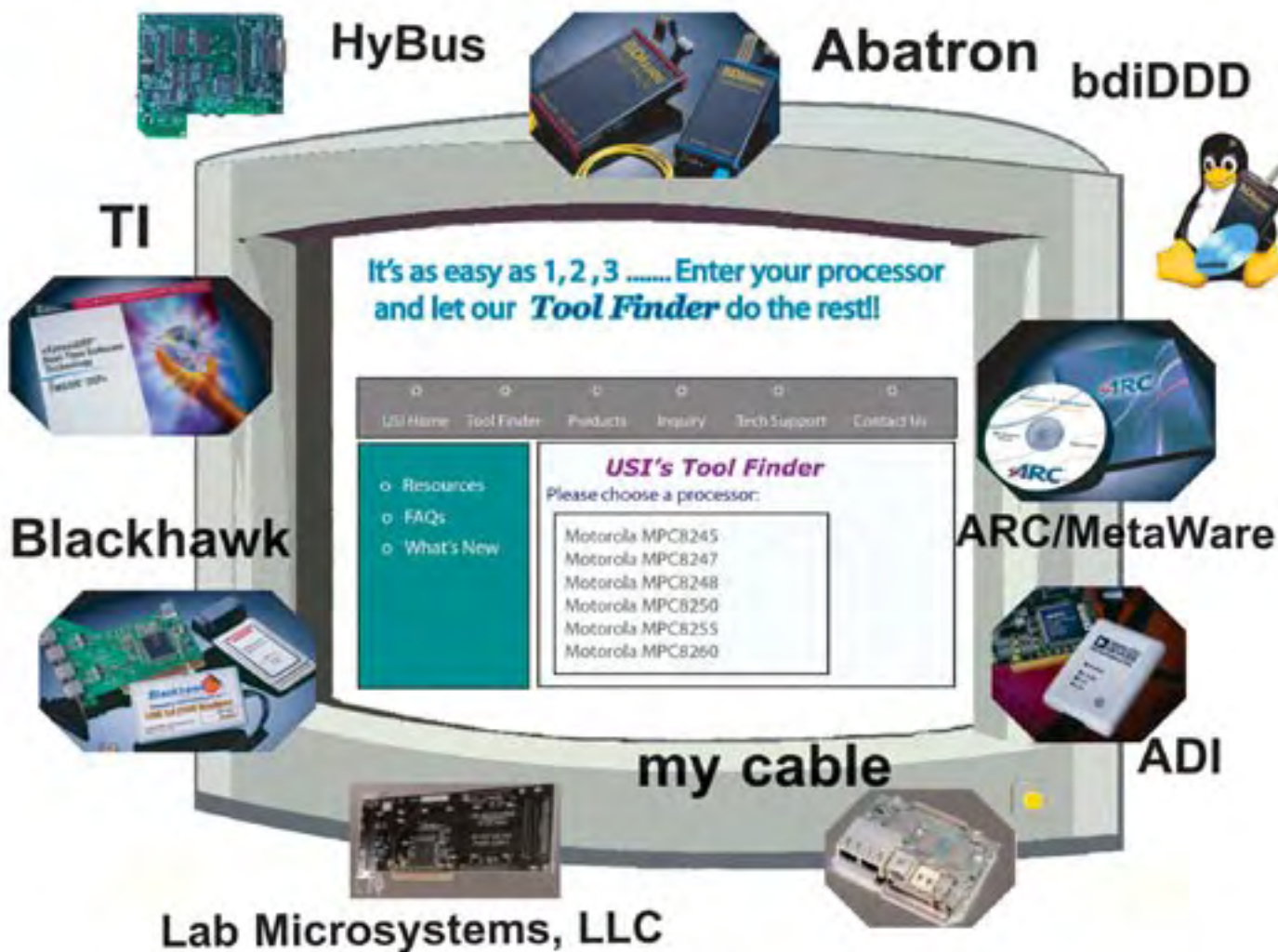


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Software and tool considerations for Linux clusters

By Michael Duffy and Duncan Roweth

Large scale commodity clusters have developed in recent years to become the dominant compute resource for High Performance Technical Computing (HPTC).

In this article, the authors draw on their experience with the design and marketing of high performance interconnect systems to discuss the technical and managerial challenges that confront the growth of the Linux Cluster market, and how system software tools can impact Linux Clusters.

Cluster acceptance for HPTC

Approximately 60 percent of the HPTC installed base is now commodity clusters that are displacing traditional vector supercomputers and large scale SMP systems (Figure 1).

Clusters for this class of computing have found wide acceptance for HPTC due to their outstanding price performance, and their enormous growth in computational capability. Clusters now dominate the list of the 500 most powerful computers in the world (www.top500.org). Of the top 500, the second and third fastest systems (Thunder and ASCI Q), are cluster-based as shown in Table 1.

The Thunder and ASCI Q computers are based on *QsNet*, the interconnect technology developed by Quadrics, a leading supplier and developer of high performance networking products and software for massively parallel systems.

Cluster acceptance for applications

Acceptance of clusters for general-purpose applications has so far been limited. This is due to the perceived complexity of:

- installing cluster-based systems
- maintaining cluster-based systems
- extracting peak performance from cluster-based systems

In the HPTC arena, customers often have to provide highly skilled internal teams to support these systems. Highly-trained IT/Linux experts tend to be in short supply and are expensive, which drives up the cost of installing and managing a cluster.

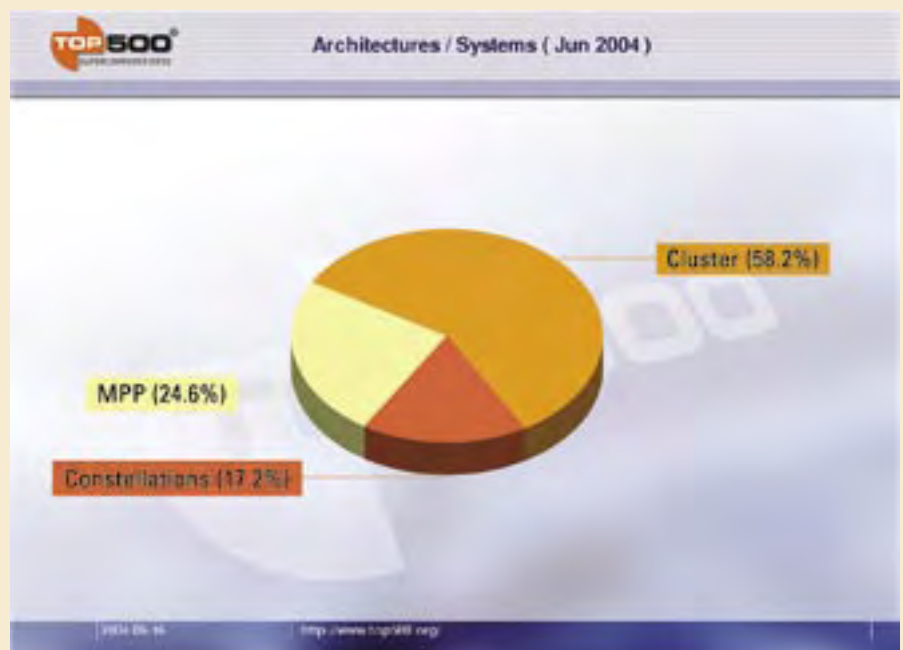


Figure 1

| Rank | Site Country/Year | Computer / Processors Manufacturer | R _{max} R _{peak} |
|------|---|---|---------------------------------------|
| 1 | <u>Earth Simulator Center</u> Japan/2002 | Earth-Simulator / 5120 NEC | 35860 40960 |
| 2 | <u>Lawrence Livermore National Laboratory</u> United States/2004 | <i>Thunder</i> Intel Itanium2 Tiger4 1.4GHz - Quadrics / 4096 California Digital Corporation | 19940 22938 |
| 3 | <u>Los Alamos National Laboratory</u> United States/2002 | ASCI Q - AlphaServer SC45, 1.25 GHz / 8192 HP | 13880 20480 |

Table 1

Smaller organizations with limited IT capabilities and budgets may hesitate to use Linux clusters because of such factors like hardware installation, configuration of Linux Kernels, driver installation, monitoring, management and repair, scripts writing, and job scheduling.

This is unfortunate because smaller organizations would often benefit from the increased computational power provided by a cluster. An embedded Linux solution would address many of these issues if the embedded tools could provide automated kernel configuration and driver build, system architecture management, hardware and software self monitoring, and selective application of intelligent software agents.

System scalability

When selecting the software tools for a commodity cluster it is essential to consider the maximum scale of system that may be required over the whole life of the program. Clustering allows the user to start small and grow the system over time. However, this advantage is lost if the software approach needs to be rethought as the system is expanded.

The challenge of scalability affects many aspects of software design. The user interface, for instance, is one area where assumptions that work for small systems quickly break down when scaled 10 or 100 fold. At the more detailed implementation level there are fixed limits on scaling, such as maximum numbers of open connections, for example, that must be understood from the outset to avoid costly re-engineering

when a system is upgraded. Insuring that performance scales as a system grows is particularly challenging, both for the application design, and system functions such as the file system.

Less obviously, scaling often highlights issues in the reliability of the basic single node hardware and software. A bug that occurs 1 out of a 1000 times on a single node, has a 63% chance of occurring when the application is run across 1000 nodes. As you scale up, the unlikely becomes the inevitable quite rapidly. The only true proof of scalability is an existence proof. Taking a large system and scaling down is a lot more certain than taking a small demonstrator and attempting to extend it.

Linux and open source tools

Commodity clusters are primarily Linux-based, so Linux-based tools naturally predominate. When it comes to tool selection, the user can choose only open source tools, or a combination of open source and proprietary tools.

The Thunder system at Lawrence Livermore National Laboratory (LLNL) was developed with the requirement that all software be open source. This system consists of over 4000 Intel Itanium 2 processors that are connected by Quadrics QsNet^{II} interconnects. It is currently the second fastest computer in the world with a measured performance of 19.94 TFLOPS.

In contrast, the MPP2 system at Pacific Northwest National Laboratory (PNNL) was developed with a combination of open source software and proprietary tools. The

software stacks for the two systems are compared in Table 2.

Software description

The basic software stack for a cluster starts from the Linux distribution. This may be either a standard proprietary distribution, or a distribution developed specifically for cluster computing.

Installation and configuration control software is provided to insure that patches and software installs can be performed consistently across the whole cluster.

An overall control program controls the allocation of resources to jobs across the cluster. This varies in complexity from a simple task farming system, to a complex multiuser partitioning and queue management system. This low-level resource scheduler will typically interface to a higher-level job queue system, possibly spanning multiple clusters.

The remaining elements of the system are the application programming environment, and where the I/O performance needs to scale with system size, a parallel file system.

Distribution choice

From the perspective of support, most users (and mainstream vendors) would prefer to use a standard Linux distribution such as Red Hat Advanced Server or SuSE. However many of the cluster tools require kernel patches which invalidate the terms of the standard support agreements. These patches typically do not change the function of the operating system, but

| | PNNL MMP2 | LLNL Thunder |
|-----------------------------------|------------------------------------|-----------------------|
| Base Linux distribution | HP/Red Hat | LLNL "Chaos" /Red Hat |
| Software install & Config Control | System Imager | YACI |
| Resource Management | RMS | SLURM |
| Batch Scheduler | LSF | LCRM |
| File system | Lustre | Lustre |
| Programming Environment | Armc + Globalarrays + Quadrics MPI | Quadrics MPI |
| Debugger | TotalView | TotalView |

Table 2

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are required to extend the kernel APIs to provide access to the system state required by specialized cluster software.

For the Thunder system, LLNL developed their own distribution, CHAOS, which integrates the set of patches required to support the Thunder software stack with the standard Red Hat distribution.

Over time it is hoped that patches that are demonstrated to be of general utility will migrate into the standard distributions. In order to support organizations standardized on commercial distributions such as Red Hat, Quadrics has developed variants of its software that run in a *patch free environment* at the cost of some restrictions in functionality.

Install process

As yet, there is not a widely adopted scalable cluster install process, although System Imager and its derivatives are widely used. Larger clusters require a multicast-based install process, to insure that install times do not increase proportionally to the number of cluster nodes. The LLNL Thunder system uses Yet Another Cluster Installer (YACI) for this purpose.

Resource manager

Once installed, the job of delivering the performance of thousands of CPUs to end user applications falls to the resource manager. Typically it will take job requests from a batch system (LSF, LCRM, or PBS for example) to allocate free CPUs and start the job. While the job is running it will manage stdio streams, forward signals, and accumulate accounting and performance statistics. On completion of the job it will clean up the nodes, thereby making them available for the next job.

The resource management system must handle a wide variety of errors, ranging from failing application processes and overfull filesystems, to unresponsive and broken nodes. Statistical inevitability guarantees that for a 1000 node system, nodes will fail every few days, and disks at least every week.

It is in this area that tools such as SLURM and RMS distinguish themselves. Simple Linux Utility for Resource Management (SLURM) is an open source system developed for Linux by Lawrence Livermore National Laboratory. Resource Management System (RMS) is a Quadrics product supported on Linux and Tru64 Unix.

When a job fails, RMS will generate a stack backtrace for the user, preserve the core files, and signal the remaining processes. The remaining processes will typically be blocked in inter-process communication. On failure of a node, the system will signal parallel jobs that span the failing node, briefly suspend scheduling of new jobs while the failed node is configured out, and then resume operation. These mechanisms underwrite the delivery of CPU time to parallel jobs in a 24/7 operation.

Most current parallel application interfaces require that the resource management system terminate a parallel job if some of its processes are lost. New implementations such as OpenMPI offer the possibility that certain classes of application can continue to run in the presence of such errors.

Resource managers typically allocate whole numbers of nodes to each parallel job for the duration. RMS supports a richer model in which applications can share the CPUs. You might, for example, run a large memory job across each node, and background tasks that consume the free CPU time. RMS supports both gang scheduling and timeslicing, ensuring that all of the processes in a parallel job are

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executed together, suspended together, and resumed together. Support from pre-emption allows a system to run low priority jobs from a background queue, suspend them when a high priority or interactive job is submitted, and resume them automatically when it completes.

Integration of Linux checkpoint restart systems such as those from Meiosys and Lawrence Berkeley National Laboratory will provide additional flexibility and resilience, allowing systems administrators to save job state in advance of maintenance periods, and migrate applications to lightly loaded nodes.

Programming environment

Message Passing Interface (MPI) dominates the programming environment for HPTC systems. The processes in a parallel program communicate via message passing (between pairs of processes) and collectives (groups of processes performing a synchronizing exchange of data).

However, while general MPI provides source code compatibility between clusters, Quadrics provides optimized MPI implementations for both generations of QsNet, and a binary compatible TCP/IP version. MPI latencies and bandwidths have traditionally been the performance metrics of high performance interconnects. However, as systems grow, hardware support for collectives (notably barrier, broadcast, and reduction) are of increasing importance.

MPI applications predominate on the LLNL systems. PNNL, in contrast, runs a mix of MPI codes that use GlobalArrays and its communication library ARMCI. ARMCI is a put/get interface that exploits the RDMA capabilities of high performance interconnects, thereby avoiding much of the inter-process synchronization associated with message passing.

Programming tools

In the area of programming tools, the baseline is the standard Linux tools – Intel and GNU compilers. These are complemented by parallel programming tools such as the Pallas Vampir performance profiling tools, and the Etnus TotalView parallel debugger tool.

File system

Lustre was initially developed for major U.S. government laboratories. It has become the file system of choice for large scale Linux clusters. LLNL, PNNL, and NCSA all run Lustre on 1000+ node production clusters. In addition, Lustre is increasingly used in mainstream products. HP recently announced HP StorageWorks Scalable

File Share, a Lustre appliance capable of being connected to both commodity and high performance Linux clusters.

Lustre stores the filesystem structure (the metadata) on a mirrored pair of MetaData Servers (MDS). The bulk data is distributed over Object Storage Servers (OSS), up to 128 in the current release. Lustre clients access the filesystem over a data network. This can be a commodity GigE network, or a high performance RDMA network such as QsNet^{II}. Single server bandwidths peak at 600 MBps in the current release. The introduction of support for multi-rail systems will see this rise to 2 GBps in the next generation of systems. Aggregate I/O rates of 11 GBps have been measured to 1000 clients. The next generation of systems will see this figure rise to 100 GBps.

Parallel file systems for proprietary UNIX systems have demonstrated today's levels of Lustre performance for some years now (for example, PFS on HP AlphaServer SC systems, and GPFS on IBM SP systems). Like Lustre, they provide resilience to disk or server failure. Lustre, however, provides two unique features, high metadata rates and an open source development strategy. This combination makes Lustre the filesystem of choice for HPTC. It is already part of HPC Linux distributions and specialist vendor distributions. Inclusion in mainstream Linux will soon follow.

Future trends

None of the companies currently integrating clusters, or building hardware or software for Linux clusters, has solved all of the discussed management problems. However, several companies offer products that indicate that the clusters of tomorrow will be easier to manage and be more productive than the clusters currently in use. As the installed base of Linux clusters grows, the users will demand improved and more cost effective tools for managing the compute resources and job scheduling.

Conclusions

The rapid development of management software for large scale Linux clusters has promoted deployment of such systems to the point where they have become the dominant architecture for HPTC systems.

The Linux operating system, combined with software from small companies and for the national labs, is allowing a wide variety of end users to exploit the benefits of commodity hardware. As the technologies developed to meet the exacting requirements of HPTC mature, and the software becomes more integrated, the systems will increasingly be used in a much wider range of applications in commercial or enterprise markets.

The authors have observed that in practice, customers are increasingly demanding the best of both worlds. What they want is an all open source solution, but in a configuration that is tested, validated, and supported by the system provider. We believe that over the next five years, the average Linux cluster size will continue to expand beyond the HPTC market into the enterprise market, that high powered CPUs such as IA64 or the equivalent will be pervasive, and the use of Linux Clusters will expand from the current emphasis on computation to working closely with storage and data centers.

As the use of Linux Clusters grows, so too will the need for stable, robust file management system features and management tools. In the future, we may see the integration of IT resources into a single network, centrally managed, that combines IP, data, compute, and video/voice communication. Integrated networks of this sort will demand improvements in cluster management tools and system software beyond the current state-of-the-art. **ECD**

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Michael J. Duffy
is President of *QS Technology*, the North American Partner/Reseller of *Quadrics* products. Duffy has over 25 years experience with high performance information technology, hardware, and software products.



QS Technology
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Duncan Roweth is head of software development at *Quadrics* in Bristol. He has been building and programming parallel systems since 1987.



Quadrics
One Bridewell Street
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By Eli Shapiro

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Website: www.dynatem.com
Model: CSATA **RSC No:** 18850
 A quad-channel Serial ATA interface card in 3U CompactPCI form factor • Four channels of Serial ATA accessible from the front panel • Maximum transfer rate of 1.5 Gbps on each channel • Intel

31244 Serial ATA controller • 64-bit/66-MHz PCI interface • PICMG 2.1 R1.0 compliant • Compliant with both SATA 1.0 and SATA II (extensions to SATA 1.0) • Drivers available for Windows NT/XP/2000 and Linux

MEMORY: FLASH

White Electronic Designs

Website: www.whiteedc.com

Model: Flash Modules **RSC No:** 18645

A line of 80-pin SIMM (JEDEC) standard Flash memory modules • Available in 1M x 32 and 2 x 1M x 32 density options • Suitable for high-speed microprocessor applications that have a no wait state requirement • 3.3V-only modules • Available in commercial (BNC) and industrial (BNI) temperature ranges • Available in a TSOP package, mounted on FR4 substrates • Access times between 70ns and 120ns

MEMORY: GENERAL PURPOSE

White Electronic Designs

Website: www.whiteedc.com

Model: WEDPN8M64V-XB2X **RSC No:** 18866

An 8M x 64 synchronous DRAM • Packaged in a 21mm x 21mm, 219 Plastic Ball Grid Array (PBGA) • Weighs 2 grams, typical • Available in commercial, industrial, and military temperature ranges • Internal pipelined operation • Frequency ranges of 100, 125, and 133-MHz • Fully synchronous with all signals registered on the positive edge of the system clock

MIL-STD-1397 (NTDS)

Sabtech Industries

Website: www.sabtech.com

Model: NTDS I/O Analyzer II **RSC No:** 18865

A COTS interface analyzer for Navy Tactical Data Systems (NTDS) • Evaluates hardware and software performance, analyzes protocol, throughput, data integrity, and timing relationships on both serial and parallel data links • Available as a rack-mounted or portable system • Connects to shipboard equipment via serial and parallel tap boxes • Captures up to five channels of I/O data for analysis • Powered by conventional 110/220VAC

POWER SUPPLY

Sola/Hevi-Duty

Website: www.sola-hevi-duty.com

Model: S2K Series **RSC No:** 18551

A line of ultra-compact, line-interactive Uninterruptible Power Supplies (UPS) with Automatic Voltage Regulation (AVR) topology and data line protection • Available in 120VAC and 230VAC models with power ratings from 300VA through 1000VA • Selectable input voltage (110V, 120V, or 127VAC) • Input voltage surge suppression • Compact dimensions • Surge-protected output receptacles • Surge-protected telephone and modem connections • Battery (internal) backup time up to eight minutes at full load • Automatic internal battery testing and status indication • Hot-swappable and end-user-replaceable internal batteries • DB-9 communications port • MultiLink power management software to facilitate shutdown of critical processes, computer equipment, or computer peripherals

PROCESSOR: PENTIUM

Carlo Gavazzi CS

Website: www.gavazzi-computing.com

Model: CSBC 1200 Series **RSC No:** 18559

Intel Pentium III or Celeron Processor with on-die 256KB or 128KB L2 Cache • Intel 82440BX AGP chipset • Up to 768MB SDRAM, ECC Level 2 • Dual PCI 10Base-T/100Base-TX Ethernet Controllers • USB, Serial, and Parallel Ports • Ultra DMA/33 IDE and Ultra2 Wide SCSI • Front and Rear I/O, Full Hot Swap Support • IPMI Rev. 1.5 Compliant

PROCESSOR: PowerPC

Varisys Ltd

Website: www.varisys.co.uk

Model: VS145 **RSC No:** 18637

A PCI-based PowerPC processor board •

MPC7457 PowerPC CPU running at 1.3 GHz • Ethernet, PMC, and host PCI interfaces • Software development supported with PowerPC Linux, a VxWorks BSP, and a GNU toolset

PRODUCTION TOOLS

Aries Electronics

Website: www.arieselec.com

Model: Test/Burn-in Socket **RSC No:** 18848

A BGA/CSP test and burn-in socket • Accommodates device packages up to 55mm x 55mm in applications up to 1 GHz • Suitable for test and burn-in of CSP, MicroBGA, DSP, LGA, SRAM, DRAM, and Flash devices with a pitch of 0.50mm or larger • Socket operating temperature ranges from -55°C to +150°C • Estimated contact life of 500,000 cycles

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RSC #65 @ www.embedded-computing.com/rsc

Data I/O

Website: www.dataio.com

Model: TF30

RSC No: 18543

A self-adjusting automated matrix tray feeder for a wide range of semiconductor component trays • Accommodates a wide variety of sizes and variations of matrix trays from Motorola, NEC, Mitsubishi, Sharp, Hitachi, Toshiba, and other manufacturers • Designed to integrate with PP and PS series automated programming systems • Allows component replenishment to the TF30 tray feeder while the host machine continues to program and process components in and out of the loaded tray

RUGGEDIZED/MIL-SPEC

Arista

Website: www.aristaipc.com

Model: ARP-2115

RSC No: 18852

A lightweight, dust-free, fanless 15" LCD industrial panel computer for rugged applications • Resistive touchscreen or strengthened glass protects the LCD panel from scratching • Aluminum panel with heavy-duty steel chassis • No moving parts • VIA low-power Eden processor at 667 MHz • System memory expandable to 512 MB • Integrates two USB 1.1 ports, one RS-232/422/485 port, two RS-232 ports, and one 10/100Base-T Ethernet port

SOFTWARE: COMPILERS

HI-TECH Software

Website: www.htsoft.com

Model: msp430

RSC No: 18655

A high-performance C compiler for the Texas Instruments MSP430 devices • ANSI C compiler • Supports 32-bit IEEE standard floating point and 32-bit long data types • Comprehensive C

library with all source code provided • Includes macro assembler, preprocessor, and one-step driver • Optimizing assembler • Multiple C optimization levels • Unlimited number of source files • Includes code wizard to generate initialization and driver code • Runs on Windows, DOS, Linux, and UNIX

SYSTEM BOARDS

Ricoh Electronics, Inc.

Website: www.ricoh.com

Model: FB5U

RSC No: 18575

An ATX motherboard for embedded applications • Intel 815E-B chipset • Supports Socket 370 Celeron (FC-PGA) or Pentium III processors with a 133-MHz FSB • Three 168-pin DIMM slots support up to 512 MB of PC100/133 memory • Optional onboard sound • Optional onboard LAN interface • Five PCI slots and one AGP slot • One floppy disk drive interface • One IDE interface supports two devices • One serial channel and one USB channel • Supports Windows 98SE/NT/2000/XP

THERMAL MANAGEMENT

Kaparel

Website: www.kaparel.com

Model: RiCool-2 Blower

RSC No: 19264

1U rack height Hot Swap PICMG 3.0 compliant, redundant design • Stainless steel housing • Provides cooling of up to 200 W per slot in AdvancedTCA Shelf • 65 dB(A) at 100 percent speed (free blowing), 60 dB(A) at 70 percent speed (free blowing) • Operating temp: -10°C to +75°C • High static pressure at zero flow of 2.8" to 3.0" (71 mm) H₂O: ideal when air filter are used (typical muffin fans have 0.3" to 0.4" H₂O) • Temperature sensor • Polarity protected • Locked rotor protection • Programmability • Nominal voltage at 48 VDC

Universal Air Filter Co.

Website: www.uaf.com

Model: Rackmount Air Filters

RSC No: 18860

A line of fully framed, cleanable rack-mount air filters designed specifically for 1U and 2U high rack-mount enclosures • Variety of media, frame, and EMI shielding options to meet specific needs • Meets UL 94 HF-1, UL 900 Class 2, CE, Telcordia NEBS GR-78-CORE, and GR-63-CORE • When used as part of a fire enclosure, they also may be configured to comply with the flame-drip requirements described in UL/CSA 60950 and EN 60950

VIDEO: DISPLAY

Densitron

Website: www.densitron.com

Model: DV30311

RSC No: 18861

A 96 x 32 pixel resolution display that is optimized for cell phone and handheld use • Single IC controller with integrated charge pump, software color adjustment, SPI interface, and temperature compensation • Measures 24.9mm x 29.2mm, with a viewing area of 22.7mm x 8.63mm • -20°C to +70°C operating temperature • 1.7V operating voltage • Available with FSTN fluid and a blue EL backlight • FPC cable with eight connections

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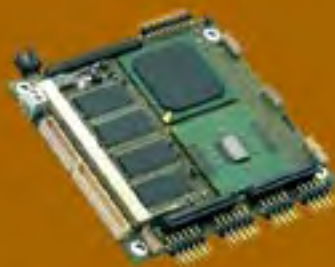
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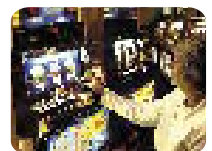
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