Embedded COMPUTING DESIGN

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COLUMNS

DEPARTMENTS

COVER
Embedded technology is changing where we live, what we wear, how we drive, and the way we receive medical care. Read more about these up-and-coming applications on page 14.

PHOTOS
Clockwise starting top left: Media Hub from Siemens VDO (www.siemensvdo.com), medical imaging equipment from Philips (www.medical.philips.com), refrigerator with built-in LCD TV from LG (www.lge.com), and grooverRider from Urban Tool (http://urbantool.com).

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FEATURES

SPECIAL: Embedded markets

SOFTWARE TECHNOLOGY: Integrated Development Environment tools

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By Tony Trawick, Mentor Graphics

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EDITOR'S FOREWORD

Perspectives on market prospects

Jerry Gipper

Trends in the embedded computing market can be analyzed in many ways. Depending on your perspective, you may maintain a different view from others. We gleaned an assortment of views on the embedded computing market while researching for this month's issue, and I would like to share some of the more interesting comments that stood out.

Phil Ames, segment manager for Intel's Embedded and Communications Group, pointed out that the industry is all about connectivity and graphics. Today, it is possible to connect devices that were never before connected. Devices are issued an IP address when they are built and connect to the Internet when they are installed.

While this development is presenting new challenges in assuring information security, it is allowing more device management. Remote management enables users to monitor, diagnose, and heal problems as they occur. Many devices have high enough processing power to accomplish much of the analytical work at the end device, improving response time and reducing Internet traffic. A typical example is a digital security camera that can recognize shapes, eliminating the need to send all the video data back to the host for processing and thus freeing the host processor from this task. These types of intelligent devices can improve workflow, so it is important to make sure embedded computing components can support integrated security and connectivity.

Phil also mentioned that human expectations are raising the bar for graphics, and that the quality of Microsoft Vista's graphics is going to raise this bar even higher. He explained that these increased expectations are leading to vastly improved point-of-sale registers and digital signage in stores. We should expect to see more dual monitors with interactive capability in kiosks and even on the desktop. The trend definitely appears to be moving toward a better human interface that is more intuitive and user friendly.

Doug Barnes, VP and GM of the Industrial Display Unit at Planar Systems, reinforced Phil's comments on graphics. "We can expect displays in areas not imagined, for instance, playground equipment that is interactive," he said. "Technology is not the limiter; application developers need to understand the capability of displays and how to use them to make the end application a better experience." Doug remarked we should expect to see many more outdoor applications using interactive touch screens as the display technology becomes better suited for outdoor use.

From my own experience, I have noted a dramatic increase in the number of hefty LED displays in the neighborhood. It has been interesting to watch how the community has responded to the impact of these displays in terms of their large size and brilliant light emission. I have noticed in the past weeks that the displays' intensity has been reduced and in some cases their operating hours have been restricted.

On the embedded computing board front, Mike Jadon, director of product marketing at Micro Memory, boldly declared that the serial fabric wars are over. "Serial RapidIO is being used for embedded backplane systems in high-end applications like defense

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and medical," he said. "Telecom is mostly GigE and 10 GigE connecting shelf-to-shelf. PCI Express (PCIe) is for the peripheral interconnects, leveraging I/O from server and PC markets on PCIe. The technical limitations are too high for PCIe to be an interconnect fabric. InfiniBand has its niche as a cluster interconnect." He asserted that many products will use a combination of these to take advantage of each fabric's strengths.

Mike also discussed the age-old trend of board suppliers moving up the food chain by offering complete integrated systems. When asked who was filling in the gap vacated by the traditional board suppliers, he stated that PC motherboards targeted at the embedded market are gaining market share and that many companies are going back to designing their own boards – back to the *make* position. Contract manufacturing services may be off-loading some of the design burden.

The fact that the embedded computing market is very fragmented is quite obvious, given the large number of companies developing technology and the seemingly unlimited number of applications for embedded computing. The volumes for any one application are usually not all that large, even for cell phones. Look at how many models there are now and how briefly any one of them stays on the market.

The real opportunity seems to be in niche markets with products that can be customized quickly to meet changing needs and provide supplier differentiation.

Jerry Gipper, Editorial Director
jgipper@opensystems-publishing.com

By Don Dingee

Watch ball!

Anyone who knows me knows I'm a baseball addict. Now that I'm well beyond my playing years, I'll watch any game – major league, minor league, college, high school, little league, T-ball, stickball, doesn't matter what level or size of field – anytime, anywhere. I've even watched games on Japanese TV while on business in Tokyo, and I speak barely a word or two of the language. I take full advantage of living in Arizona, starting with spring training in March and ending with fall league games in November, and even plan vacations around baseball games I can attend while on the road.

This time of year, as a new season begins and hope springs eternal, baseball is my number one priority – even before sleep and food most of the time. When I learned Major League Baseball (MLB) started talks earlier this year with DirecTV for exclusive rights to the MLB Extra Innings package, I became a bit nervous. Last year I was able to get MLB Extra Innings on my cable provider and keep up with teams across the league. If this deal goes through, the cable broadcasts will be eliminated. (As I write this for our deadline, the deal has not yet been approved.) But I can't justify switching to DirecTV solely for my baseball fix.

So, I've set out looking for an alternative. MLB also broadcasts over the Internet on their MLB.TV package, which is improving bandwidth again this year and becoming a viable option on a PC with a high-bandwidth connection and decent graphics horsepower. Now, if only I could stream the feed from my PC to my HDTV so I could view games in the comfort of my living room instead of just my office, I'd be set.

Streaming content is taking over the Internet, and the major networks are now streaming their shows online as well.

Stream away

Each year at the Consumer Electronics Show we watch closely for embedded technology behind the scenes. As luck would have it, I may have found a solution to my dilemma at this year's event. We scheduled a visit with a firm named Quartics (www.quartics.com) that sounded interesting. Their cofounder, Safi Qureshey, also founded AST Computer, a name you might remember from the 1980s.

We spent a few minutes talking about Quartics' technology with Charlie Raasch, the company's senior director of product planning. He sees two forces at work in the marketplace right now. First of all, a lot of streaming content is now available on the Internet, with more coming out every day. Secondly, even a powerful Intel processor gets eaten alive and consumes a huge amount of power while transcoding High-Definition (HD) recording or display formats. However, an optimized media processor designed specifically for transcoding can get the job done efficiently. Quartics has designed a family of Systems-on-Chip (SoCs) for several applications such as USB displays, wireless projectors, and the one I'm most interested in – what they call *PC2TV*.

In the Quartics PC2TV system, content is streamed from a PC or laptop over an 802.11g wireless connection to a media coprocessor box attached to the TV. The coprocessor, based on a 200 MHz MIPS core running embedded Linux, handles the heavy lifting of the HD decoding process, outputting 720p HD video from a number of streaming formats. Figure 1 shows a block diagram of the Quartics SoC.

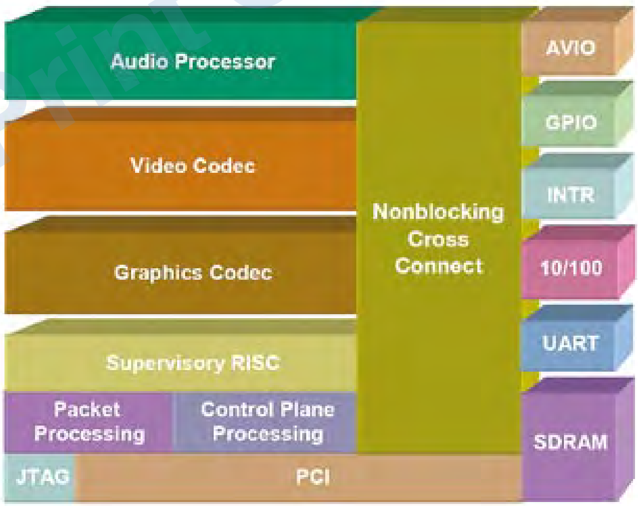

Figure 1

To the PC, the PC2TV system looks like a Wi-Fi connection with a simple peer-to-peer driver. Because it doesn't have extra software, none of the processing overhead hits the PC. Consumers don't need to worry about the streaming format since the SoC handles just about anything that can be thrown at it – MPEG-4, WMV, DivX, H.264, QuickTime, and others.

While today's systems are based on 802.11g, the technology can be adapted to any IP-based Ethernet solution – Multimedia over Coax Alliance (MoCA), Home Phoneline Networking Alliance (HPNA), or other technology. Charlie also pointed out that streaming content is showing up on non-PC devices like video iPods, which are also in future plans. They are pushing to have the capability embedded directly into HDTV units to eliminate the external box, but for now these external boxes are their entry into consumer markets.

There's stuff on besides baseball?

Obviously, this solution is for more than just baseball. Streaming content is taking over the Internet, and the major networks are now streaming their shows online as well. But it might just be the ticket for my baseball-viewing habit. I'd like to hear your thoughts and ideas on this and other ongoing developments in embedded technology – e-mail me at ddingee@opensystems-publishing.com.

embedded world highlights

By Hermann Strass

The embedded world exhibition and conference in Nuernberg, Germany kicks off a series of European electronics events each year in early or mid February. This year, 590 companies from 29 different countries exhibited their products to almost 14,000 people, 40 percent of whom were international visitors. More than 1,000 attendees visited the conference portion of the program to hear presenters from 24 different countries exchange views on the latest embedded trends and issues. An *electronic display* conference was added to this year's venue. Figure 1, courtesy of Nuernberg Messe GmbH, shows Professor Ing. Matthias Sturm delivering a speech during the opening ceremony of the event.

Figure 1

Two trends caught my attention during the trade show. The most obvious was the number of multicore processor announcements. It seemed that every company that uses microprocessors presented dual-core processor-based boards across practically their whole product range. Though many embedded applications may not have a technical requirement for this yet, all the suppliers have done the conversion. Now software experts will have to recode and test all their systems and applications to benefit from the new processors.

The second trend is how automotive electronics technologies continue to lead growth in electronics, both hardware and software. Several institutes within the Fraunhofer Gesellschaft, Europe's largest research institution, presented reliable and efficient software for cars or intelligent automotive technologies, integrated intelligence in cars, and other research projects in a practical and usable form. The electronics and automotive industries continue to find new ways to use embedded computing processing.

Awards for innovation and clever ideas

Two awards were presented at embedded world 2007. The *University Award*, presented for the first time at this year's event, was granted to three winners. This award gives students the opportunity to have their bachelor's or master's degree projects challenged by an international jury. The jury seemed surprised by the number of entries and their quality.

The following students won the University Award:

- **First place: Dipl.-Inf. Dmitrij Kissler of the University of Erlangen-Nürnberg for his thesis on "Design of a Generic Weakly Programmable Processor Array (WPPA)."** Dmitrij's master's thesis project involved a new class of microcomputer architectures called *WPPAs*. The devices combine the advantages of efficiency (in terms of area, power, and performance), application-specific circuits, and the flexibility of programmability (processing elements and interconnectivity of processing elements), which standard multicore Systems-on-Chip (SoCs) offer. WPPAs would provide codesigns with typically 1/10 to 1/100 of the chip area and 100 to 300 times better power efficiency than standard approaches with equal performance.
- **Second place: Roland Mühlenbernd from the University of Paderborn for his thesis on "FPGA Implementation of a Server-Based Scheduler for Periodic Hardware Tasks."** This runtime system uses a server-based scheduling method called *MSDL* for task execution. The runtime system and all tasks are entirely implemented in hardware.
- **Third place: The team of Philipp Jahn and Thomas Polzer from the Vienna University of Technology for their bachelor's thesis on "Graphical Development Environment for Embedded Systems."** This tool simplifies and speeds up the development process, greatly improving productivity. The user can graphically abstract from the embedded target, focus on the development process rather than on the internals of the target, and easily map the needed resources to the real world.

The traditional *Embedded Award* was presented to the following winners in three categories:

- **Hardware: SSV Embedded Systems – smart connections with Micro Linux PC.** This 32-bit embedded Linux computer system with integrated hardware and software is preinstalled on a USB memory stick, which enables the host PC to address the Linux computer as a virtual network interface or a virtual COM port. Applications can be moved around on the USB stick, requiring only a USB interface and a Web browser on the host.
- **Software: Telelogic – Rhapsody AUTOSAR.** The Rhapsody AUTOSAR software package is the first model-driven development environment based on the Unified Modeling Language and on the Systems Modeling Language.
- **Tools: aquintos GmbH – PREEvision.** PREEvision is an innovative systems engineering solution for designing and benchmarking electric/electronic architectures in automotive systems offering domain-specific graphical notations for body, chassis, power train, and multimedia electronics.

For more information, contact Hermann at hstrass@opensystems-publishing.com.

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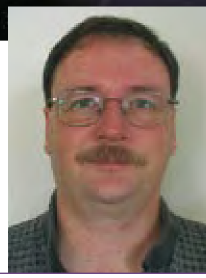
CDT 4.0: more features for embedded development



By Doug Schaefer

Editor's note: *I was honored to represent* Embedded Computing Design *on the judge's panel for the Eclipse Community Awards 2007 Best Commercial Developer Tool. Congratulations to Doug and his teammates at QNX for winning with the Momentics IDE.*
– Don Dingee

eclipse COMMUNITY AWARDS 2007
Best Commercial Developer Tool

2006 was a landmark year for the Eclipse C/C++ Development Tooling (CDT) environment, with growth in almost every area of the project. Currently, developers download the CDT more than 85,000 times a month (up from 60,000 earlier in 2006), and more than a dozen committers are working on the next CDT release. Meanwhile, numerous tool vendors now redistribute Eclipse and the CDT with their product offerings, especially in the embedded market where the CDT has become the *de facto* standard development environment.

What's in the CDT

The CDT focuses mainly on the edit, build, and debug cycle of software development. Its main objective is to improve the productivity of programmers writing code in C and C++ while leveraging the high-quality tool chains developers already use for building and debugging. Initially, the CDT project focused on developers who use the GNU tool chain, including gcc and gdb, which is by far the most popular tool set in the open source community. However, the CDT project now supports other environments as well, either directly or through CDT-based environments offered by commercial vendors.

The CDT follows the same user interface and project resource structure as other Eclipse-based development environments. The user interface comprises a collection of views and editors that appear as tabbed sections of the Eclipse window. The views show a variety of information about the project, and the editors allow developers to change files in the project. The views can be organized into pages called *perspectives*, which customize the layout of views for various purposes, such as edit and debug. Users can also adjust and save perspectives for their own specific needs. Figure 1 shows the C/C++ perspective.

Projects in Eclipse are the top-level resource users work with. Typically, a project maps to a root directory in the user's file system. Every file that resides in that directory and its subdirectories recursively become accessible to the Eclipse plug-ins. Eclipse also provides mechanisms to link other files and directories into the project structure, but does not offer a general mechanism to exclude files.

The Eclipse platform provides management for files and projects. The CDT extends this management to differentiate source files, object files, and other file types; it also provides a structured representation of file contents. Using this representation, the CDT populates both the Outline View, which shows a table of contents in the current file, and the C/C++ Project View, which shows a table of contents in available projects.

The CDT core also maintains a database of symbols across each project. This database, called an *index*, allows a number of features to provide source code analysis and navigation. For example, the user can select a function name in the source code and do a search to find all references to that function. The user can then invoke the rename refactoring feature to change the name of that function across the entire project.

The CDT editor offers many productivity features developers would expect in an advanced Integrated Development Environment (IDE). The biggest productivity enhancer is the content assist feature, which uses information from CDT's built-in parser to provide valid code completions, given the context that currently contains the cursor. The editor also provides code coloring, which differentiates between keywords and identifiers to enhance code readability, and bracket matching and automatic tabbing, which make complex code structures easier to enter.

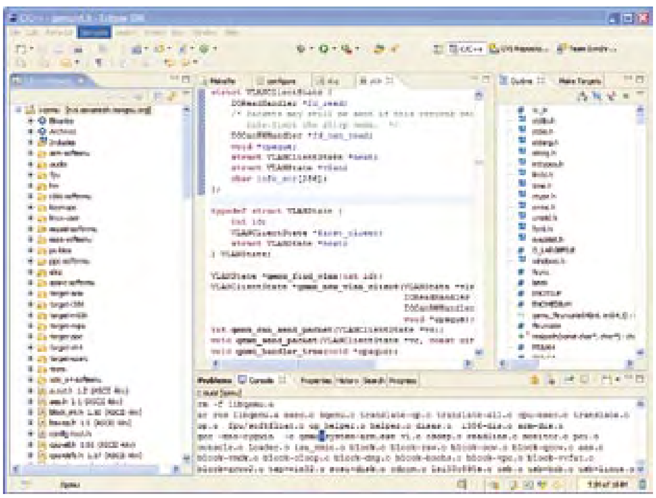


Figure 1

The CDT also contains the following two build systems:

- **Standard Build:** Reuses the user's existing build infrastructure. This feature is especially important for project teams that have invested heavily in conventional make files to ensure quality, reproducible builds.
- **Managed Build:** Allows tool vendors to provide advanced user interfaces for setting compile and link options; it also invokes builds automatically. Managed Build is useful for new projects and for users who would rather spend time writing source code than creating build files.

The CDT debug perspective provides visualization of the debug session (see Figure 2). A native debugger such as gdb handles the nuts and bolts of executing the application, setting breakpoints, and extracting variable values. Table 1 summarizes the visualizations the debug perspective offers.

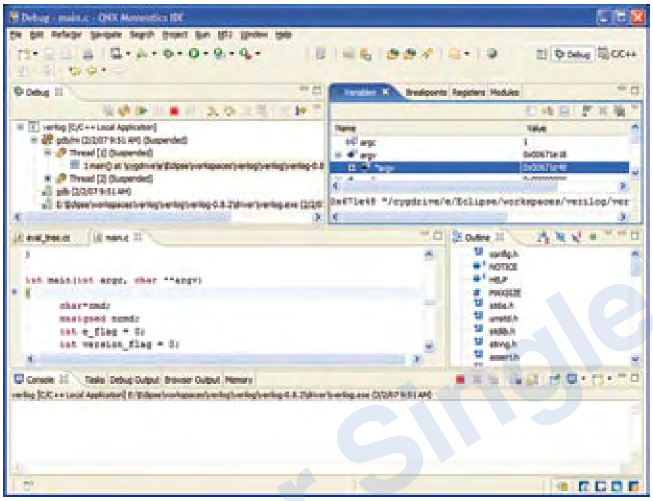


Figure 2

This View	Displays
Debug	The current debug sessions and the threads and stack frames for the applications under debug
Variables	Variable values for the current stack frame
Register	Current values of the CPU registers
Memory	Binary contents of memory
Disassembly	Assembly code for the instructions at the current execution location

Table 1

What's coming in CDT 4.0

CDT 4.0 is scheduled for release this June. With the great influx of contributors to the CDT, the new release will introduce several exciting features that improve the user experience, enhance productivity, and offer even greater scalability. Features under development include:

- **Internal Builder:** Improves build performance by removing the need to process make files. To determine which files a build must process, the Internal Builder uses Eclipse's ability to track file changes and uses interfile dependency information stored in the CDT source index. The builder can parallelize compilers to deliver faster build times on multicore machines.
- **Support for prebuilt index information:** To further boost indexing performance, the CDT indexer will allow Software Development Kit (SDK) vendors, including major operating systems vendors, to prebuild the index information for the header files provided by the SDK. The indexer can then integrate this information with the index of the user's code, eliminating the need to parse the SDK header files in the user's environment.
- **Enhanced index information:** The CDT team has enhanced the captured index information to enable new navigation and source code analysis views. The Call Hierarchy View (Figure 3) allows navigation between functions and the functions that they call or are called by. The Include Hierarchy View allows navigation between files based on inclusion relationships, and the Type Hierarchy View can navigate between C++ classes based on inheritance relationships.
- **Support for Windows SDK:** Recently, Microsoft has provided its compilers as a free download for its Windows SDK. CDT 4.0 will include build and debug support to let these tools work with CDT projects. As a result, developers will no longer need to use the GNU tools on Windows, which have been problematic because of their need for an emulation environment, such as cygwin, or because of incomplete SDK support, such as mingw. This build and debug support will also open the door for Visual Studio users to migrate their projects to the CDT in the future.
- **Framework for project generation:** Many IDEs that target specific platforms can generate skeletal projects for various project types. For example, a project for a desktop GUI application can generate enough source code to get the framework running and displaying a window on the screen. This boilerplate code gives the developer a head start when building the project. CDT 4.0 will provide the framework for such project generation.

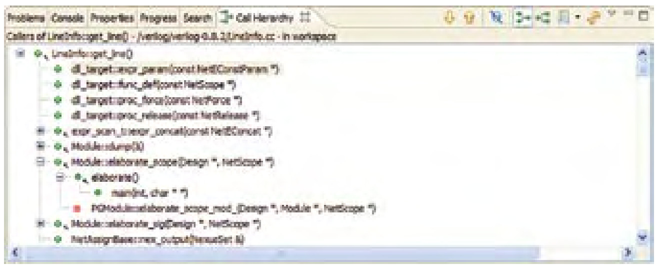


Figure 3

CDT 4.0 will be a landmark release for the CDT. Besides allowing the CDT team to firm up APIs, the release introduces new functionality that makes the CDT a compelling environment for all developers building C/C++ applications, regardless of which platform they target.

***Doug Schaefer** is the project leader for the Eclipse CDT project and a tools architect for QNX Software Systems, where he is involved in all aspects of the Eclipse-based QNX Momentics IDE. Doug has been a tools developer for most of his career and is a strong proponent of open source software development. Besides leading the CDT project, he serves on the project management committee that oversees all tools projects at Eclipse.*

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Embedded here, there, and everywhere

By Jerry Gipper and Don Dingee

Creating a list of applications that would not benefit from embedded computing would be easier than creating a list of applications that already include an embedded processor of some type. It's no secret that embedded computing is everywhere. The ability for devices to "think" and be connected is driving the demand to insert intelligence into products of all kinds. We often question the immediate benefit of doing this, but someday we will come to appreciate having a toothbrush that can think and be connected to the Internet. Soon parents and dentists will be able to know for sure whether or not kids brushed, how well they brushed, and even get updates on who's skipping brushing.

Almost everything we touch in our lives is a candidate for embedded computing of some type: the clothes we wear, food (at least the packaging), tools, homes, cars, and entertainment. As you look around your office or home, most of what you see could gain from the ability to monitor itself and communicate information somewhere to have some decision made about its status. Of course, all this could lead to tremendous information overload, which would force designers to create smaller decision-making and knowledge-based management systems, once again driving the need for more computing power. If everything around us can someday make its own decisions, then what role will we as humans undertake in the future?

We shouldn't get too far ahead of ourselves here. Let's step back and focus on the next three to five years and see what's in store. Many of the applications that we reviewed overlap as the user moves between environments. For instance, intelligent clothing comes into play as part of infotainment, home automation, and medicine. The following discussion presents some applications that will have or continue to have a major impact in the next few years.

Keeping up with the Jetsons

Home automation has been a hot topic in embedded computing for years. Everyone wants to be like the Jetsons, with Rosie taking care of the cleaning and the family's other basic needs. However, the road to home automation has been very slow. New devices such as the refrigerator with built-in LCD TV shown in Figure 1 (courtesy of LG) appear every year, but most are expensive or impractical at this stage. Integrators have carved out a niche in making systems work. Though home monitoring and security are perhaps the leading applications, there is room for improvement as we try to avoid false alarms when leaving the system turned off or in reduced-function modes.

Figure 1

The home automation industry struggles with multiple standards for communication and control. On the most basic level, communications are relayed via wiring or radio waves. Structured wiring is an option, but must be built into the home during original construction or added in at a substantial cost. Power-line carrier technology uses the home's existing electrical wiring with special adapters to interface with devices. Many RF-enabled devices like light switches, dimmers, and HVAC controls can be installed easily and included in a home's expanding automated network. Many companies offer products that can bring automation to our lives, but substantial interoperability issues must be overcome to gain wide acceptance. Several wired and wireless solutions, from X10 to ZigBee, INSTEON, and Z-Wave, are competing in the marketplace now.

Frost & Sullivan reports, "A crucial trend in this industry is the developing shift from proprietary platforms to open ones, which offers interoperability and more flexibility to end users."

The latest home automation embedded computing technologies offer enumerable benefits, including:

- Affordability
- Reliability and flexibility
- Simplicity and speed
- Interoperability
- Security

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ZigBee Alliance Chairman Bob Heile comments, "For ZigBee growth to accelerate, OEMs and others must push through their product development cycles. They must educate their customer base about the new cost savings and business opportunities created with networked devices versus stand-alone products." The same can be said for the other competing smart home technologies.

Fashion for the smart dresser

Advances in electronic components, battery power, digital signal processing techniques, and the Internet are allowing for applications within this segment that were not achievable in past years. Advanced conductive thread weaving and technology enhance the user's well being and comfort, providing health monitoring for infants and the elderly, personal area networks to connect wearable devices, and hands-free, voice-activated entertainment and communication. New biometric sensors monitor activity and provide feedback to control devices. Intelligent clothing that in the past only space programs could afford is now appearing in our stores.

"Due to advances in processing power, improved form factor, and the development of conductive textiles [that is, e-textiles], the computer has well and truly become wearable," Frost & Sullivan asserts. "Conductive fibers that can transmit both data and power, advanced processors that are able to strike a balance between performance as well as power consumption, and printable electronics are the true enabling technologies driving this advance in computing." However, high costs and concerns about return on investment are currently casting a shadow on wearable computing's future acceptability from a commercial perspective.

Some examples of intelligent clothing include:

- Clothes that plug into an MP3 player and provide touch or voice control and even moving images on the back
- Wearable computers with sensors and user interface
- Health-monitoring clothing with biosensors and capacity for communications to a medical facility, such as the LifeShirt pictured in Figure 2 (courtesy of VivoMetrics)
- Massage robes that give the wearer a soothing massage and can be regulated depending on the level of relaxation desired

In the coming years, clothing products will increasingly assume intelligent functions. Clothing will combine the functions of medium, carrier, and interface for an extremely wide range of microsystem applications. Microsystem technology is constantly producing increasingly smaller components, enabling intelligent functions to be integrated into everyday products without causing negative consequences on their usage range.

Intelligent clothing should allow people to communicate with other people and computer systems as they wish, regardless of where they are so they can access global information via the Internet and control activities remotely. This will make routine tasks easier to carry out and demonstrate new ways of working, with the emphasis on simplifying existing applications and opening up completely new application fields.

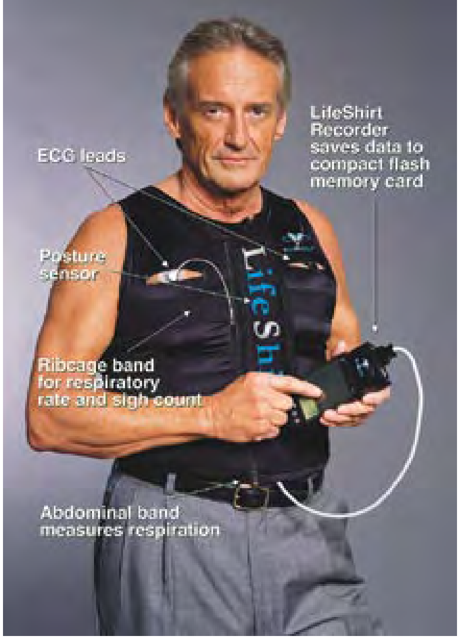


Figure 2

Researchers at MIT point out that, "One challenge for developers of smart clothing, for example, is management of the huge data volume that results when users wear clothes or devices that are literally packed with sensors. Another concern is privacy and security of medical information."

The Body Sensor Networks (BSN) organization (www.bsn-web.org) adds that some of the BSN community's key research focuses on the following recent technological developments and clinical applications:

- Novel bioelectrical, biochemical, biophysical, and mechanical sensors
- Hardware considerations: low-power RF transceiver, energy scavenging, battery technology, miniaturization, system integration, and manufacturing process and cost
- Biocompatibility and materials
- Context awareness and multisensor data fusion
- Data inferencing, knowledge discovery, and prediction
- Quality of service and trust and security issues
- Autonomic sensor networks
- Standards and lightweight communication protocols
- Integration with ambient sensing in applications such as smart dwellings and home monitoring
- Wearable and implantable sensor integration and development platforms
- Clinical applications of body sensor networks

Honk if you've got a processor

Next to the home or office, many people spend a lot of time in vehicles of one type or another. Telematics has combined with infotainment to provide similar experiences in the car. Embedded electronics are used heavily in newer vehicle models. Advancements are still needed to better connect to the Internet and integrate systems within a vehicle.

Telematics systems provide application-level services for information delivery at any time to any place in any form. Such systems are by definition distributed, and in general very complex and composed of diverse subsystems. Yet they must be reliable, cost effective, scalable, and open-ended to cope with evolving user requirements, explosive usage

Almost everything we touch in our lives is a candidate for embedded computing of some type …

growth, and continuous technology developments. Particular challenges at the service/application level include:

- The need to access and work with multimedia and real-time content
- The growing importance of supporting cooperation between people in various settings
- User mobility and roaming

The term *telematics* was originally coined to mean telecommunications and information processing convergence. It later evolved as a reference to automation in automobiles and, more broadly, using computers and telecommunications to enhance motor vehicles' functionality. GPS navigation, integrated hands-free cell phones, wireless communications, and automatic driving assistance systems all fall under the telematics umbrella as depicted in Figure 3 (courtesy of Siemens).

A sampling of key telematics initiatives includes:

Drive-by-wire

Drive-by-wire replaces hydraulic and mechanical systems in motor vehicles with electronic controls and systems. For example, joysticks and other controls can replace the steering wheel and brakes. Drive-by-wire also includes sensor-based systems that automatically try to avoid a collision when another vehicle comes too close. Various aspects of drive-by-wire are expected to be implemented in the next decade.

Figure 3

Adaptive cruise control

Adaptive cruise control is a vehicle cruise control system that automatically slows the car if it is moving too close to the car in front of it. A radar unit located behind the vehicle's grill determines the speed and distance of the object ahead. The system accelerates back to its last speed setting until the distance is computed to be safe again.

Dedicated Short Range Communications (DSRC)

DSRC is a wireless technology for vehicular traffic. Using a modified 802.11a technology for North American cars and trucks, DSRC is designed for several applications. For example, ambulances can cause traffic lights down the road to change in their favor, and traffic congestion can be transmitted to automobile navigation systems. It allows vehicles to sense they are about to crash, prompting safety systems to begin tightening seatbelts and warming up airbags before impact. In addition, a standard for wireless payment allows parking lots and fast-food drive-ins to offer the same convenience as automated highway toll systems, such as E-ZPass.

Lane departure system

A lane departure system is a vehicular safety system expected to help people who fall asleep at the wheel from drifting off the road. Cameras monitor the white and yellow lines on the road, and the system alerts the driver if the vehicle crosses the line without the turn signal being activated.

Smart car

A smart car is an automobile with advanced electronics. Microprocessors have been used in car engines since the late 1960s and have steadily increased in usage throughout the engine and drivetrain to improve stability, braking, and general

No need to turn over the wheel

One major challenge with intelligent transportation systems is drivers' resistance to relinquish vehicle control to intelligent systems. At the Consumer Electronics Show in January, demonstrations at the Vehicle Infrastructure Integration (VII) Technology Showcase sponsored by Connexis, ITS America, and the U.S. Department of Transportation emphasized traffic safety and traveler information, including wireless communications and intelligent processing installed in vehicles and roadside equipment. These demonstrations showed how intelligent systems can offer assistance without forcing the driver to give up control.

- **Traffic signal violation warning.** An intelligent intersection sends instantaneous traffic signal information to an approaching vehicle. The vehicle collects this data and uses it to determine the risk of an unsafe passage based on vehicle position and speed. When needed, the vehicle delivers advisories cueing the driver to corrective actions, thus reducing the risk of intersection collisions.
- **Public safety vehicle priority signal activation.** A public safety vehicle issues a request to the intersection for signal priority. The traffic signal state is changed if appropriate, allowing the vehicle fast, safe passage through the intersection.
- **In-vehicle signing.** Dynamic road condition data is received from roadside equipment. Audible driver advisories are presented to the driver as the vehicle approaches an active work zone, alerting the driver to a potentially dangerous situation.

TechnoCom (www.technocom-wireless.com), Raytheon (www.raytheon.com), and Econolite (www.econolite.com) collaborated on the VII technology demonstrations. TechnoCom provided its Multiband Configurable Networking Unit platform to interface the vehicle with both the roadside and software to interface with the intelligent intersection equipment. Raytheon provided vehicle and roadside system engineering, and integration services as well as application software. Econolite provided the intelligent intersection equipment (including the traffic signal controller and associated sensors and processing) used in all demonstrations.

Tallying traffic

Wavetronix (www.wavetronix.com) specializes in counting cars using advanced K-band radar and signal processing technology. Conventional counting systems use loops embedded in the roadway, but these often fail as soon as lanes are restriped or torn up during construction. The Wavetronix radar unit hangs on a pole just off the road, aims across up to 10 lanes of traffic, and autoconfigures to determine where lanes are. The radar unit can differentiate a truck from a car and even spots visually obscured vehicles using DSP technology. Radar units are spaced out at intervals along a road and connected to computers via RS-485, determining traffic volume, movement rate, and other valuable information for traffic management.

comfort. The 1990s added information-oriented enhancements such as GPS navigation, reverse sensing systems, and night vision (the ability to visualize animals and people beyond normal human range). The 2000s are adding Web and e-mail access, voice control, smart card activation instead of keys, and systems that keep the vehicle a safe distance from cars and objects in its path.

Intelligent Transportation System (ITS)

Much research is underway in making the roads we drive more intelligent and better able to monitor traffic, report changes in conditions, and control traffic flow. The ITS program improves transportation safety and mobility and enhances productivity through advanced communications technologies.

Intelligent transportation systems encompass a broad range of wireless and wireline communications-based information and electronics technologies. When integrated into the transportation system's infrastructure and in vehicles themselves, these technologies relieve congestion, improve safety, and enhance productivity.

ITS comprises 16 types of technology-based systems divided into intelligent infrastructure systems and intelligent vehicle systems:

- **Intelligent infrastructure:** arterial management, freeway management, transit management, incident management, emergency management, electronic payment, traveler information, information management, crash prevention and safety, roadway operations and maintenance, road weather management, commercial vehicle operations, and intermodal freight
- **Intelligent vehicles:** collision avoidance systems, collision notification systems, and driver assistance systems

Electronics, the best medicine

Health care has long been a pioneer for embedded electronics. Amazing new uses emerge daily. As the boomer generation ages, medical issues are becoming more prevalent and more urgent. Technology can address many of the issues involving patient monitoring, diagnosis, and treatment that are bound to overwhelm our medical infrastructure. Telehealth is an emerging subapplication that utilizes many of the latest embedded computing technologies as demonstrated in Figure 4 (courtesy of Philips).

During a panel session at this year's Consumer Electronics Show in Las Vegas, Philips Business Manager Jeff Perry remarked, "Consumerization of health-care technologies drives opportunities to serve patients in new ways and in new settings." Perry and the other panel members discussed the convergence of electronics with home health care and how electronics can enable medical attention to be part of our daily lives, connect patients with their health-care providers and families, and support independent living. The panel also mentioned key elements that must be defined to allow electronic solutions growth, including:

- Common health application protocols
- Clear and reliable physical communications standards

Figure 4

- Mobile monitoring and processing product development
- Useful devices and solutions for empowering the consumer
- Advanced and integrated sensors for improved data collection

To help address telehealth-care challenges, several technology companies recently formed the Continua Health Alliance (www.continuaalliance.org), a collaborative industry organization dedicated to bringing together standards and technology to create new health-care solutions. The Continua Health Alliance envisions personal telehealth systems that combine diverse products and technologies to enable better personal health care for people worldwide. Founding members include Avita, Body Media, Cisco, GE, IBM, Intel, Kaiser Permanente, Medtronic, Motorola, Nonin, Omron, Panasonic, Partners HealthCare, Philips, Polar Electro, RMD Networks, Samsung, Sharp, Tunstall, Welch Allyn, and Zensys.

The Continua Health Alliance hopes that creating a rich interoperable health and fitness devices ecosystem will produce the following effects:

- Empower individuals and patients to better manage their health by providing them with information regarding their fitness and health through personal medical devices and services
- Allow loved ones and professional caregivers to more accurately monitor and advise chronic disease patients and elderly individuals living independently
- Enable medical and fitness device manufacturers to rapidly develop interoperable devices and services using industry-developed connectivity standards
- Enable health-care providers to offer better quality care through personalized health solutions assembled from a rich, interoperable health-care devices and services marketplace

Barriers to increased adoption

All these applications share many common variables in their formulas to success. Wireless connectivity, security, cost, and performance play a factor in each. Early adopters have used many of these technologies, but what are some of the barriers preventing us from benefiting today from the innovation underway in these markets? What can the embedded computing industry do to advance the technology?

Performance

Before most consumers will move to a new solution, the technology must deliver more performance at a lower price than existing technologies. Why would they move if they get less? In most cases, today's technology has the performance to get the job done, but sometimes the expense is still high, either in unit cost or in installation or integration cost.

Access to market

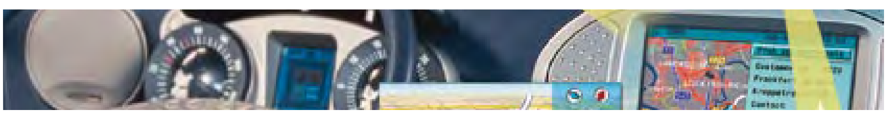
New products must have a channel to market. They must build supply chains that connect the technology to end-user markets. Oftentimes the channels exist; the iPod provides a great example of how Apple established itself as a consumer supplier and leveraged existing and supplemental channels to deliver the iPod to the masses. Most smaller companies that provide the best innovation have very limited access to the consumer markets. Integrators have proven successful in many of these niches, but to achieve mass-market success, technology must be self-installable.

Legal obstacles

Regulatory restrictions can prevent quick market pickup, especially in medical-related markets. Licensing issues can also cause a hassle, such as with wireless technologies that have certain radio frequencies restrictions or availability problems. We will run into more environmental restrictions as we grow more concerned about disposing the electronic devices we use now and those we will use in the future.

Technology resistance

Some people struggle with using technology. Poorly designed human interfaces, battery life, security, and unreliability provide some examples of things that turn off potential users. Products that are not intuitively easy to use eliminate the technology-challenged majority from the market. Battery life is critical because so many products are portable.



Batteries add to the *green* disposal issues. Many products use wireless technology, where security is often suspect. As products gather and process more personal data, security issues become more important. To be truly successful, a product has to work. The technology-challenged are not going to spend time debugging the product – they will just avoid the hassle.

Interoperability

This is a huge issue as new generations of products are introduced. Incompatibility from one generation to the next or between old and new technologies causes many users to become frustrated and confused. They hate having products that don't work as advertised or are significantly different between models. Forced obsolescence drives them crazy. So far, vendors generally haven't been rewarded for offering better interoperability.

Legacy

Many of these technologies are finding success in new geographic markets where infrastructure doesn't exist. For example, intelligent highway initiatives are taking off in China because the investment in new highway building is significant. Home automation is tied strongly to new construction. Opportunity is best where new infrastructure is being built.

Marketing

Most engineers deem *marketing* a bad word, but a well-marketed technology will always beat a great technology hardly anyone has heard of. The key to getting broader adoption is to show how cost effective, easy to use, and productive a new technology is. Early adopters will choose something just to be the first on the block to have one, but mainstream users have to see that it helps people just like them. Notice the consortia springing up in several of these marketing areas. Don't overlook marketing efforts when designing, creating, and deploying new technologies.

Rising above the challenges

This report described only a few of the new applications we are seeing. It appears that technology does not pose a major hurdle to adopting much of the innovation underway in these application segments. They all seem to have similar barriers, with interoperability, security, and technology resistance presenting the biggest obstacles. Technologists play a major role in overcoming these challenges – they must make the products work with each other in a secure manner while making the human experience easy and pleasant. Keep reading our articles for new ideas on how to best do that. ECD

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Using RDMA to increase processing performance

Applications are increasing the demand for CPU processing performance and the amount of data being transferred between subsystems. Offloading data movement to I/O hardware increases the amount of CPU resources available for these applications, boosting the system's performance.

By William Lee

Remote Direct Memory Access (RDMA) optimizes data movement between servers, accelerating the performance of applications in today's clustered supercomputers. With a few simple handshakes, two servers' network adapter cards can move data between their respective system memory spaces with little to no CPU involvement (see Figure 1). Using InfiniBand Host Channel Adapters (HCAs) with RDMA, data is placed directly into target memory. The CPU is required only for setup and completion signaling.

When compared to CPU-intensive transport technologies such as TCP/IP running on top of high-speed links (see Figure 2), RDMA can reduce CPU overhead by up to a factor of 10. Using conventional Network Interface Cards (NICs), the CPU must move data on to and off of the network preventing it from working on applications. In most common systems, data is moved twice. In embedded connections, on the other hand, where data sources and destinations are known at boot time, RDMA can lower CPU overhead to near zero. Using RDMA in I/O-intensive embedded systems can increase the value of the system by optimizing overall performance.

RDMA moves data directly from one CPU's memory to another's, but when data moves off the local bus, data integrity and transport become an issue. For this reason, RDMA requires a reliable transport to ensure data is segmented and reassembled correctly and arrives uncorrupted. On the send side, transport offload in the I/O device takes care of data segmentation and packet assembly. On the receive side, the I/O device handles all the data integrity checking, header stripping, and data reassembly. Assured delivery acknowledgements and retransmissions are also processed automatically. Subsystems using RDMA and transport offload can transfer a sustained data stream with little impact on the other applications' performance.

InfiniBand HCAs are designed to implement RDMA and transport offload. HCAs at both ends manage all the data transfer, essentially moving entire blocks of data from one subsystem's memory to another's. The receiving side can be a computer subsystem, server, or storage array. Additionally, data source and destination can be set up well before data becomes available. In certain embedded systems with predefined source and destination, this can be done when the system initializes before the applications run.

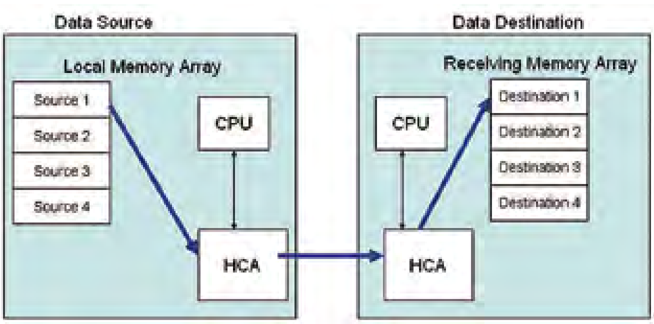

Figure 1

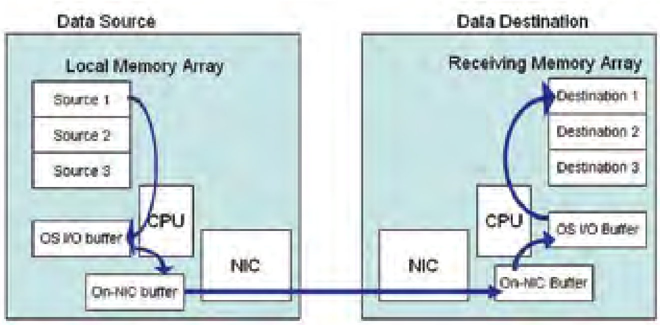

Figure 2

Data acquisition

High-bandwidth data acquisition systems generating a continuous stream of data, such as radar, satellite antennas, video cameras, or a collection of sensors aggregated onto one I/O channel, can take advantage of an InfiniBand HCA's RDMA capability. Blocks of memory can be allocated at boot time for local storage of the data being acquired. The HCA can be configured with the location of each local block of memory and the destination location for that block in the receiving subsystem.

Memory blocks are used to store data as it is acquired. When the first block is filled, the HCA is notified and transfers the data while the next block is filled. Data can be continuously acquired and transmitted in this manner. The CPU only has to notify the HCA as each block is filled, representing a significant reduction in CPU overhead compared to non-RDMA systems.

The receiving node can be a storage array, single server, or server within a cluster. Real-time rendering of video or radar images, for example, requires a significant amount of processing. Because the destination location was predefined and configured in the sending unit, CPU involvement in the data transfer is near zero; it will receive notification at the end of each data block reception for processing as needed. Using InfiniBand RDMA ensures that a continuous stream of data is available for the server and that the server has the maximum processing power required for the job.

Clustered storage array

Storage servers can be clustered with an InfiniBand fabric to create a high-performance, scalable array for Network Attached Storage (NAS) or Storage Area Network (SAN) units. Each storage server managing its own client connections appears as a monolithic block of storage when in reality it can share storage capacity with any number of its peers. IT managers can easily increase the capacity of a storage array by adding more storage servers to the embedded fabric.

Using InfiniBand RDMA ensures that a continuous stream of data is available for the server and that the server has the maximum processing power required for the job.

Relying on the storage server's CPU to manage data movement to and from its peers would severely restrict the number of clients the storage server could serve. Using RDMA between the storage servers offloads data transfers from the CPU, freeing it to serve more clients or to do more work for each client, such as running more I/O operations per second or providing more bandwidth. This improves scalability because the workload on the storage server does not increase dramatically with each added peer. Furthermore, connecting the backup system to the embedded fabric simplifies backups because data movement from each unit can be offloaded to the unit's HCA rather than involving its CPU.

Data transfers between storage servers wouldn't necessarily require predefined memory locations. With each client request, the storage server would communicate the source and destination locations with the appropriate peer. At this point the HCAs would take over, moving the data efficiently across the embedded fabric.

Real-world applications

Mellanox Technologies' InfiniHost III InfiniBand HCA devices and cards have been implemented in systems similar to those described earlier. The single-chip architecture can provide RDMA and reliable transport without requiring external memory. Integrated SERDES supports one or two ports at speeds up to 20 Gbps, and transmission distances up to 20 meters or more over copper cables and 300 meters over fiber-optic cables. These reach capabilities allow the data source to be located in a separate room from the destination if necessary. These devices and cards have full open source driver support through the OpenFabrics Alliance (openfabrics.org). ECD

William Lee *is a senior product marketing manager at Mellanox Technologies. Prior to joining Mellanox, he was a product line marketing manager at Zarlink Semiconductor and a strategic marketing manager at Marvell. He received his BSEL from the California Polytechnic State University in San Luis Obispo.*

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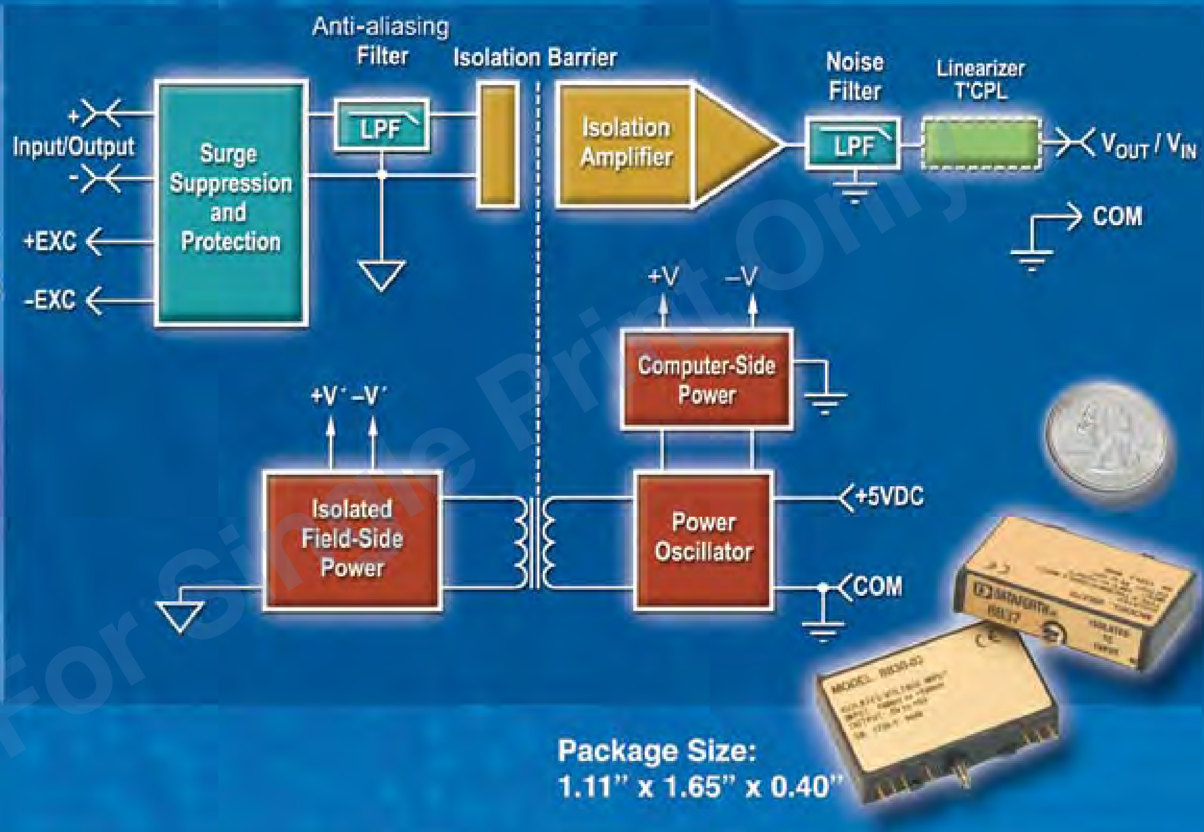

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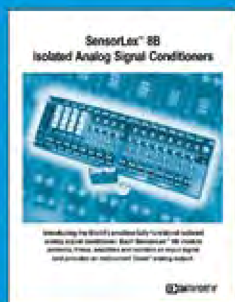

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Where are embedded computers? They're in the *long tail*

By Lawrence Ricci

Understanding ubiquitous embedded computing requires appreciation of what has been called the long tail *phenomenon. Designs targeting cross-platform applications can maximize the value of embedded devices.*

The long tail, depicted in Figure 1, refers to the fact that suppliers cannot just focus on the *mainline items* in a market flooded with multiple choices. Internet retailers like Amazon and Netflix first recognized the importance of the long tail when they discovered that a significant portion of their revenues came from rather obscure products. This finding directly contradicted the pattern at bricks-and-mortar retailers such as Barnes & Noble and Blockbuster, which generated revenues primarily from major titles. While the term *long tail* is most often used in the context of consumer products, embedded system suppliers will find much, if not most, of their business in the long tail.

This phenomenon is differentiating ubiquitous computing from the world of universal computing. The old Microsoft mission statement, "A computer on every desk and a computer in every home," aptly expressed the goal of universal computing, which was based on uniform hardware standards and a universal operating system API. In this world of universally available (but uniform) computers, a program like Lotus or WordPerfect could be introduced and quickly proliferate across millions of identical systems. However, with ubiquitous computing, the situation has changed. These embedded computers are necessarily based on diverse form factors and unique technologies literally molded into the artifacts of daily life.

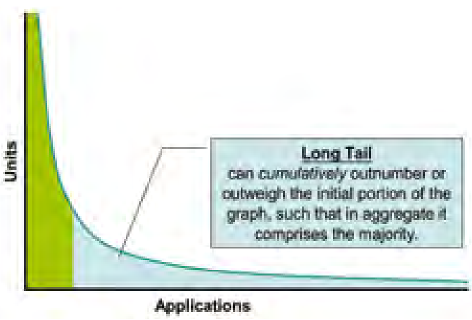


Figure 1

All types of everyday tools – golf carts, high-end sports cars, farm tractors, medical monitoring equipment, factory test equipment, gambling devices, machine tools, digital signage, cash registers, commercial scales, and exercise equipment – contain sophisticated, networked computers. These computers look completely different, and for good reason. None of these specific applications requires a tenth of the production volume necessary for a low-volume PDA, laptop, desktop, or cell phone. Everyone in the supply chain for these ubiquitous computers must understand this long tail phenomenon as the world continues to demand that embedded computers have the same or better features as universal computers (PCs, laptops, PDAs, and smartphones).

While the quantity demand for a specific form of an embedded device decreases, its value may increase. As might be expected, the value increase is often proportional to the "niche-ness" of the embedded computer's features. Indeed, the high value of the embedded system may not even be distinguished from the high value of the device in which it is embedded.

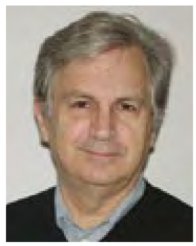
For example, a superior telematics/tele-entertainment system might be a primary differentiating feature of a $100,000 high-end automobile. The embedded system, plus better paint and a few hundred dollars' worth of leather upholstery and walnut trim, might separate the high-end vehicle from a sensibly priced mid-range sedan. This long tail vehicle is big business. A company might make only 5,000 units of a $100,000 auto, but that represents $500 million of profitable business – a measurable impact on the income statement of even an automotive giant.

Designing a system for the long tail presents a challenge; designing it cost effectively and quickly poses an even greater challenge. Complex strategies for wireless networking, security, biometrics, power management, and graphics simply cannot be developed from the ground up for each device. So, even without a fixed hardware reference like the perennial PC BIOS, much software must be transportable. The embedded system industry is currently struggling with this process of technology reuse.

The original promise of Java – *write once, run everywhere* – has never been fully realized in the embedded space. Today, most embedded Java programs are narrowly targeted on cell phone form factors and require volume commitments far higher than long tail applications. The Linux community and Microsoft, however, have made strides in serving long tail applications. Leveraging the small size and modularity of Linux, compact distributions with special embedded features (file systems and power management) are available and work well in non-PC architectures. Microsoft has modularized Windows CE for different CPUs and almost any device's form factor. Perhaps most notable are the capabilities that let an application query its hardware and software environment and then configure itself based on the available display size, orientation, color depth, communication link speeds, and so forth.

Third-party software suppliers focusing on the cross-platform, cross-application, universal needs of the ubiquitous computing environment are facilitating long tail applications. Universal needs include remote device maintenance, device administration, security, intermittently connected database operation, graphics, and multimedia rendition. These applications can power a machine tool controller or a heavy equipment computer – whichever application is needed on the long tail.

The business prospects for ubiquitous computing are bright. OEMs assembling the system can apply preexisting technology to a new form in a new application on the high-value portion of the long tail. **ECD**



Lawrence Ricci *heads business development for Applied Data Systems, coordinating technology partners and others to create new products for new and emerging markets. He has 20 years of expertise in marketing embedded systems designs for automation, military, and other applications as an employee and consultant for companies including GE Industrial Systems, ABB, and DEC. Lawrence has been designated an elite Microsoft MVP since 2000 and is interested in enhanced security for embedded systems and P2P store-foreword networks. He has a BS in Physics from Rensselaer Polytechnic Institute and an MBA in Progress from Johns Hopkins University.*

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Implementing a software product line development approach

By Richard F. Boldt

The latest advances in full life-cycle Model-Driven Development (MDD) environments address the challenges of implementing a Software Product Line (SPL) and enable engineering teams to harness the speed and profitability promised when using a mass production-centered software development approach. Richard explores this SPL concept, detailing a tool and development process.

Defining the SPL

The Software Engineering Institute (Carnegie Mellon University, 2006) defines a *Software Product Line* as "a set of software-intensive systems that share a common, managed set of features satisfying the specific needs of a particular market segment or mission and that are developed from a common set of core assets in a prescribed way." With its focus on reuse, the SPL enables domain engineers to create a set of core software assets for the product line that application engineers can later use to implement the final products. SPL implementation is, for many, an appealing concept but challenging to put into practice. Nevertheless, the promise of the SPL's productivity gains has forced the industry to take notice and adopt the approach.

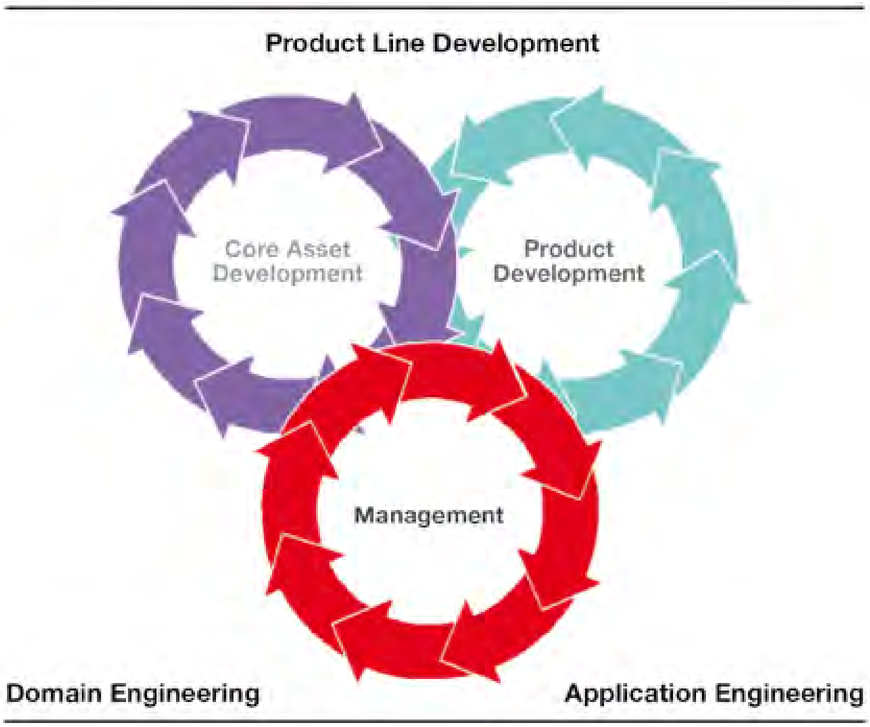

Figure 1

Before demonstrating how an *MDD* environment can complement and drive the SPL approach, designers must understand the relevant terms. As defined by the Software Engineering Institute, the SPL is simply a group of products with related capabilities specifying a common set of core software assets that can be created and then reused across multiple product variants on multiple platforms. To do this, SPL defines a process consisting of domain engineering and application engineering.

Domain engineering focuses on creating core software assets, including any variability an asset may have and how one asset may relate to another. Domain engineering always considers reuse as part of the overall design construction.

For application engineering, engineers select assets to create the specific product they are developing while addressing any variations or relations as required. The management portion of the process deals with feedback between domain engineering and application engineering, enabling continual refinements to the process and additions to the asset library. For example, when the final product requires a capability that does not exist in the asset library, the question of whether this capability should be developed and added to the asset library or just added to this product must be answered. Figure 1 shows how engineering components come together to form product line development.

Unified Modeling Language and Systems Modeling Language for MDD

Model Driven Development relies on two key standards from the Object Management Group, the *Unified Modeling Language (UML)* and *Systems Modeling Language (SysML)*. UML is a comprehensive, full life-cycle modeling language that provides developers with diagrams that allow the user to model the structure, behavior, and interaction of systems and system components.

These diagrams work as follows:

- The use case diagram shows what the system does and who uses it
- Sequence diagrams show how elements communicate over time
- Class diagrams show classes and relations between them
- Object diagrams show instances of classes and how each is linked to the others at runtime
- The structure diagram shows the internal structure of classes

Additionally, state machines and activity diagrams define behavior or algorithms. Packages, which resemble folders, organize the UML model elements.

SysML extends UML to include the concept of requirements that can be linked to any other model element, ensuring complete requirements coverage for the design.

Model-based architectures

One type of MDD environment implementation, *Model Driven Architecture (MDA)*, also extends the UML standard. The vision behind MDA is to embrace technology change and standardization as well as focus on the long-term interoperability that allows organizations to maintain their Intellectual Property (IP) in the face of technology changes. UML is key to this vision because it allows users to represent systems at a semantic rather than technological level.

To make MDA work, system semantic concepts must be isolated from technology implementation so developers can capture their IP in Platform-Independent Models (PIMs). The PIM contains formal UML specifications of the system's structure and function that abstract away the technology details. Developers can transform PIMs to use specific implementation technology by creating Platform-Specific Models (PSMs) using a translation approach, which includes adding technical details such as middleware, operating system, network, and CPU characteristics.

Decision support and requirements management

Within the SPL approach, requirements engineering drives the development of features and capabilities for a variant point. For requirements, the SPL approach necessitates that the core (main) features of every variant product should be determined. This includes making key decisions about variant features not in development but planned for the next release.

To meet the goals of component reuse, designers must be able to map commonality, variability, and the dependencies between all requirements, including test requirements. The basic principles of requirement elicitation, gathering, modeling, and traceability clearly establish product goals. With decision support weighting and analysis, critical decisions regarding features that will bring the most value to customers can be made in real time. Solid decision support and requirements management provide a foundation for accurately establishing the scope of how a product line can be produced, tested, and deployed.

Variant-based configuration and change management

The challenge facing traditional configuration management tools within the SPL approach is how to allow efficient software asset management. SPL efficiency increases the more designers can automate the change control and software configuration management process to manage product variations. Variant-based change and configuration management solutions bring value to an SPL approach by managing change dependencies between different software artifacts and allowing those changes to be propagated to interdependent downstream or upstream artifacts in the production workflow.

In addition, a variant-based change and configuration management environment allows teams to reliably deliver a product instance created from the stable collection of existing common assets, variation points, decision model, and production mechanism. By doing so, teams will successfully move toward an assembly-line approach to delivering products and applications.

Fitting it all together

In view of the definitions for the key components, how does a full life-cycle MDD environment enable the SPL approach? UML allows domain engineering to create a library of reusable software assets. MDA techniques can thus be applied to transform the reusable assets into the final products. Domain engineering uses decision support and requirements management to determine which assets will be created for reuse; application engineering then selects assets for each individual final product. Both domain and application engineering use variant-based configuration and change management to enable the management function. Figure 2 shows examples of reusable assets developed and tested in an MDD environment for SPL implementation.

In addition to being platform independent, the UML models (PIMs) are also self-documenting, which helps application engineers understand their reusable assets. When following an SPL approach, designers must focus the PIMs on reuse

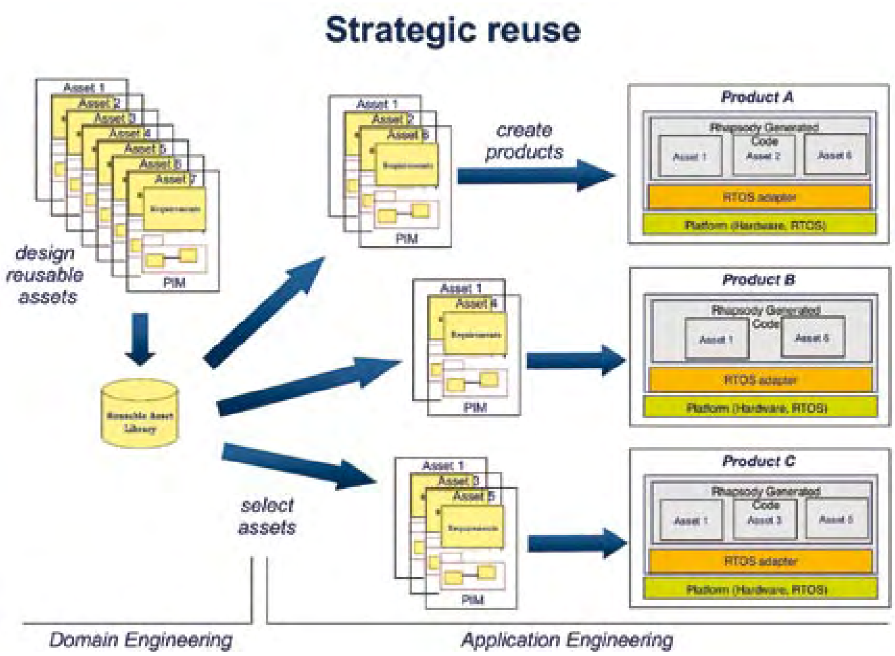

Figure 2

> To adopt an SPL approach, developers can implement a powerful, full life-cycle UML-based MDA environment that automates and simplifies the development process.

while maintaining the ability to express variation within an asset and the relations between assets. With UML 2.0, engineers can define a structured class in terms of *parts*. The parts' interfaces can be defined using ports. Parts and ports are mechanisms that make PIMs highly scalable and support component-based plug-and-play reusable architectures. Additionally, UML 2.0 can describe variability because it is naturally suited to defining relationships and provides the stereotype concept for customization.

Once application engineering has selected the specific assets for an individual product, these assets, or models, must now be translated into PSMs for product implementation. To provide additional process flexibility, automatic code generation based on core technologies such as a real-time framework – which abstracts away platform details and can be converted into different real-time operating system specific adapters – and rules-based code generation allow models to be implemented in different ways. For example, one strategy can be followed for a safety-critical application and another for a resource-constrained environment.

To adopt an SPL approach, developers can implement a powerful, full life-cycle UML-based MDA environment that automates and simplifies the development process. Bringing together the benefits of this approach – UML modeling's powerful abstraction capabilities and translation technologies from MDA, decision support and requirements management, and closely coupled task-based configuration and change management – enables engineers to create software assets for customizable reuse and deployment. By working in a seamless, full life-cycle MDD tool chain, users can drive the productivity gains necessary to make SPL development a reality. **ECD**

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The complexity crisis in embedded software

By Mark Underseth

A hidden embedded software crisis is brewing in the electronics industry. Companies are seriously struggling to deliver complex, high-quality embedded software while leveraging hundreds, if not thousands of software resources across the globe. Although advances in semiconductor technology and processes continue to produce more densely integrated silicon, software methods and technology have not kept pace with increasing software complexity. Companies recruit engineers and add resources through contractors or outsourcing but still end up shipping products late and deliver less-than-acceptable software. This problem is driving up embedded software costs and, more importantly, is crippling productivity and competitiveness.

Embedded software methods lagging

During the past few years, conversations with various companies in the electronics ecosystem – chipset suppliers, major OEMs, and wireless network operators – have revealed a common theme. Everyone is struggling with software complexity and quality from their suppliers. Chipset suppliers grapple with problematic software from third-party software vendors; OEMs complain about the software delivered from chipset partners; and wireless carriers protest against poorly tested handsets from OEMs.

This problem is occurring because the industry is trying to develop embedded software with largely the same methods and practices of 10 years ago, despite software development complexity increasing dramatically.

First, the embedded software within a device is no longer a *fixed-function* application or set of applications serving a tightly defined set of functions. Today, the embedded software shipped with a device is often a software platform upon which third parties develop and deliver additional content and applications. The methods and practices used to develop, integrate, and verify software on the earlier, simpler embedded software environment are insufficient and not scalable for complex embedded software platforms.

This means that the days of developer heroics are over. It is no longer possible for a few superstar engineers to rescue a software release. When embedded software was relatively simple and the development teams were small, a few diligent and competent engineers could carry projects to successful completion. With the size and complexity of today's embedded projects, however, hundreds of developers, integrators, and testers are involved in embedded software. Engineering organizations must manage, integrate, and productize software globally from internal developers, outsourcers, contractors, software vendors, and even open source. To scale effectively, solid management, efficient processes, and effective development practices are critical.

Though some companies today have reviewed and evolved their embedded software development methods, the exponential increase in software complexity seems to have caught the industry as a whole off guard. Numerous companies might confess to problems delivering acceptable quality products on time, but are so overwhelmed that management opts for the short-term solution and simply adds more engineers. The immediate market demands of delivering more functionality in shorter market windows often complicate process change implementation in the midst of revenue objectives. Other times, the missing catalyst is an internal visionary sponsor with the fortitude and authority to drive improvements. Embedded software technology vendors have not pioneered the problem either, so new innovative solutions and thought leadership have been lacking as well.

Observations and symptoms

Hence, even in the most process-oriented and forward-thinking companies, embedded software development practices and technology haven't evolved substantially. Even with access to countless global software resources, companies continue to struggle to produce high-quality embedded software for sophisticated devices. Some common patterns and symptoms include:

- **Disparate software testing approaches.** When software teams do not standardize developer testing in any fashion, engineers are left to create their own one-off, *ad hoc* testing approaches that no one else can reuse or automate. Internal efforts to standardize developer testing usually occur within functional teams that create and maintain their own specialized testing solutions. While the teams can be commended for taking testing seriously, their diverse approaches prevent tests from being aggregated, reused, and automated on a large scale.

- **Integration testing largely left to Product Test.** After implementing software components, some engineering organizations perform integration testing that merely consists of a "smoke" test to confirm a successful build and conduct some rudimentary manual tests before passing a release to the Product Test team. Accordingly, product testing is often the first time all embedded software components are extensively tested as an integrated whole.
- **Large volumes of defects discovered late.** Without fail, many defects are uncovered once software releases enter Product Test, engaging developers in fire-fighting debugging sessions and initiating the first of multiple resource-intensive cycles in Product Test. This forces developers to fix bugs when they're the most difficult, time-consuming, and expensive to resolve.
- **Disproportionate time and resources allocated to Product Test.** The relative time and resources devoted to product testing activities present an alarming drawback. In many companies, software coding or implementation is a relatively brief period. Integration activities can be twice as long, but product testing is even worse – it takes 5-10 times as long and usually requires large teams that may continue to grow.

Operational havoc

Companies following this pattern of software development predictably experience stressful and undesirable results. After submitting their code for integration shortly before a release milestone, developers already know they're in for some long triage and debugging sessions. Prior to the software entering Product Test, developers don't have visibility or metrics to gauge the quality of a candidate release. Managers trust developers to be diligent and thorough in testing their own software, but inevitably, the Product Test team discovers and reports a long list of defects, prompting an eleventh-hour hiatus that pulls software engineers away from other development to characterize, prioritize, and resolve bugs. Despite the greatest of efforts to salvage a release date, the software is invariably late.

At that point, attempts to predict a new product release date are just plain guesses.

When you're staring at several hundred critical defects and twice as many serious defects, it's anybody's guess when the software will be ready.

Of course, no one can manage product development effectively with such uncertainty. Over time, companies will try to compensate for the unpredictability. Software managers will assign or staff additional resources, usually test engineers, to their projects. In their development planning, project managers allocate more and more time for the integration and testing phases. Neither of these fixes is really effective nor scalable; they only minimize the symptoms.

Automate, automate, automate

Conceptually, the solution is rather simple: Automate software testing and integration extensively before software releases reach Product Test. Providing infrastructure and processes enables software developers and integrators to create and deliver reusable, automated tests that can be leveraged throughout the development cycle and in derivative projects.

For this solution to work, software verification must be unified across development teams. Instead of using disparate one-off testing solutions or harnesses, a single, common test framework should be implemented. This allows one functional team to create tests anyone can reuse, execute, and aggregate and automate for regression or integration testing.

In this *software supply-chain verification strategy* (Figure 1), everyone who develops or contributes software is a supplier. Suppliers deliver their software components to internal and/or external customers or consumers. Thus, to enable customers to verify or effectively integrate software components, all suppliers must deliver reusable, automated tests along with their code.

The supply-chain analogy is very appropriate, considering that many companies model their embedded software development after manufacturing processes. Companies would adopt a software *factory* model in which developers would be organized into *component factories* or teams responsible for delivering specific software components based on functional expertise or specialties (for example, data protocols, UI, security, Bluetooth, and multimedia). Using the supply-chain analogy, software components would be sourced through various possible suppliers, including internal component factories, outsourcing firms, third-party vendors, open source, or chipset partners.

Ultimately, software from all suppliers, including outsourcers and third-party software vendors, must be integrated and function as a cohesive whole. For example, when delivering a new SMS software component, an outsourcer would provide tests that could be reused and automated within a common test framework, greatly facilitating the acceptance and integration process. That outsourcer would become a true extension of the internal development team.

For complex embedded software development, the unified test framework is now critical common software infrastructure, similar to a configuration management system or a build environment.

Regaining control

The business implications of missing product releases or shipping shoddy software into the market are significant. Some embedded software executives are essentially managing blindfolded until software releases enter Product Test.

By unifying and automating software verification and reporting, software managers can regain control. A dashboard of real data and metrics to quantify software stability and completeness could give them up-to-the minute information to manage and allocate their resources effectively. They could control their product release dates more easily and predictably and make management decisions based on real-time data. Occasionally, managers rightfully hold back releases because they had visibility into critical defects.

Once a unified and automated software verification strategy is implemented and integrated into the development process, software managers usually see significant process improvements, including software components integrating successfully on the first try, integration and Product Test teams detecting significantly fewer defects, and software releases passing through Product Test in record few cycles. However, the result that matters most is the ability to predictably deliver high-quality products on time. As one manager put it, "We successfully delivered the product and achieved customer acceptance on time … Priceless!" ECD

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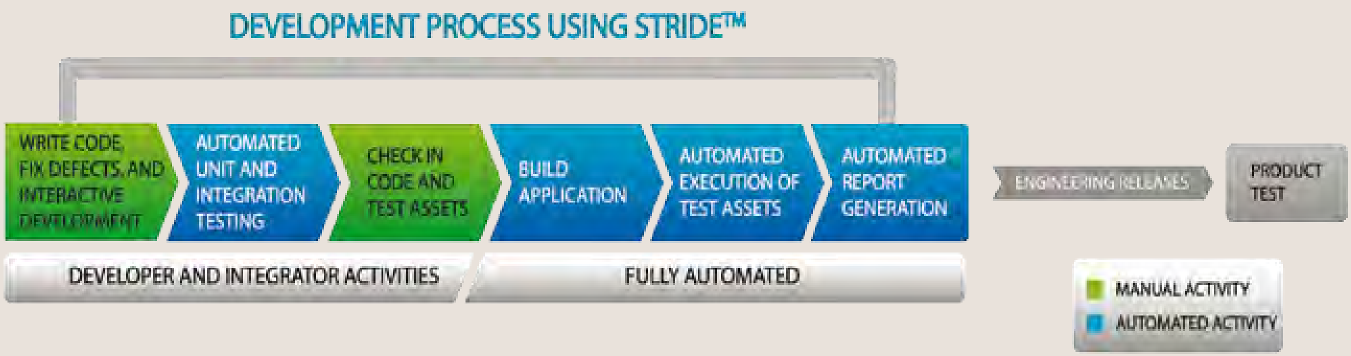

Figure 1

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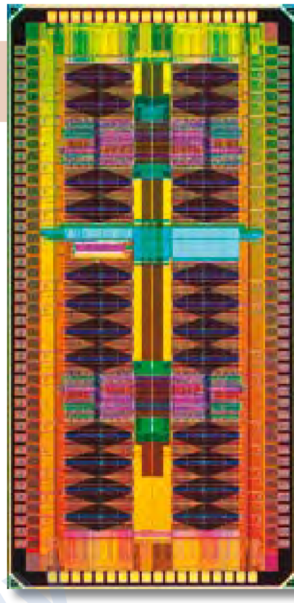
Single chip, triple the memory



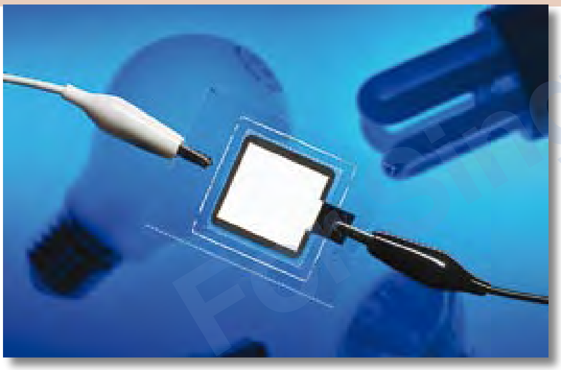
With the advent of multicore processors, memory has become an increasingly critical aspect of microprocessor performance. Microprocessor design engineers struggle with giving cores access to the most and fastest memory possible. Multicore processors will likely starve quickly using today's technology.

IBM recently announced a major breakthrough in microchip design that will more than triple the amount of memory contained on a single high-end chip. The prototype embedded Dynamic Random Access Memory (eDRAM) chip contains more than 12 million bits and high-performance logic. This new technology, designed using IBM's Silicon-On-Insulator (SOI) for high performance at low power, vastly improves microprocessor performance in multicore designs and speeds graphics movement in gaming, networking, and other image-intensive multimedia applications.

IBM's new eDRAM technology, designed in stress-enabled 65 nm SOI using deep trench, dramatically improves on-processor memory performance in about one-third the space with one-fifth the standby power of conventional static random access memory.

IBM Microelectronics • eDRAM test chip

Groundbreaking top-emitting OLEDs



As pressure mounts for more brightness and lower power, LEDs are emerging as a brilliant solution. In a fast-growing market, Organic LEDs (OLEDs) are key parts of this revolution, turning the dream of paper-thin, flexible, highly efficient displays with brilliant colors and high contrast into reality. OLEDs represent the future of ultra-flat-panel displays and a vast array of new lighting applications.

Novaled has achieved groundbreaking results in top-emitting RGB stacks' lifetime, voltage, and efficiency with its PIN OLED technology. Lifetimes are up to 16,000 hours for blue OLEDs and up to 100,000 hours at an initial brightness of 500 cd/m² for red and green. This latest performance indicates that green OLED devices are now outperforming their bottom-emission reference samples by a factor of 2.5. White top-emission devices achieved a lifetime of 18,000 hours at a driving voltage of 3 V and a starting luminance of 1,000 cd/m².

Top-emission OLED structures that emit light away from the substrate are a key feature of future OLED applications. The top-emission type increases the aperture ratio above 50 percent for displays and paves the way for more powerful, large-area active-matrix displays. When used in lighting devices, top-emission OLEDs enable manufacturers to use cheap, nontransparent, and flexible substrates.

Novaled AG • PIN OLED

PCIe's got comm covered

Originally designed for component-level applications, PCI Express (PCIe) is being stretched to provide system-level interconnections that are more demanding and often involve more connections. The latest PCIe devices from Integrated Device Technology, Inc. (IDT) manage all communications throughout a system predictably and efficiently while providing full-line rate throughput, reliability, and high quality of service. The new devices are optimized to meet the capacity, scalability, and predictable throughput requirements that bladed system providers demand. This solution, which includes the industry's first 64-lane and 16-port device, enables equipment providers to use PCIe as the primary high-performance system interconnect for demanding server, storage, communications, and embedded applications.

Three devices manage communications between roots and intelligent endpoints throughout a bladed system. Ranging from an 8-port, 32-lane configuration to 16 ports and 64 lanes, the IDT switches offer unprecedented levels of switching capacity and system scalability and provide predictable, full-line rate performance for multiple simultaneous traffic flows, regardless of system loading. The remaining 2- or 3-port devices support address translation and nontransparent bridging between PCIe domains. This family of devices offers what appears to be the lowest power consumption per port of any PCIe system switching solution available in the market today.

IDT • PCI Express devices

www.embedded-computing.com/search

Solving the fundamental problems of high-performance software development

By William Lundgren, Kerry Barnes, and James Steed

Programming languages must provide multiprocessor information to successfully move and process data in high-performance software. In this analysis, William, Kerry, and James present three algorithms, explain how to implement them efficiently on a multiprocessor target, and show how the Gedae multiprocessor programming language can automate the implementation.

The fundamental problems of high-performance software development are how to get data into fast memory and how to process it efficiently from that memory. This may seem like an oversimplification, but consider the work that goes into both moving and processing data when programming a multiprocessor system under tight real-time processing requirements. The task of getting data into fast memory includes data movement both on a single processor (for example, cache utilization) and between processors. The application must be partitioned between processors to keep the load balanced and to realize the benefit of parallelization while avoiding deadlock. The task of processing data efficiently involves using every possible processing path. Compute-intensive portions of the application must be structured so that all arithmetic logic units are fully utilized, and Direct Memory Access (DMA) processing units must be fully utilized to ensure data transfer and processing happen simultaneously.

A few tools available today address software development for multiprocessor architectures. Current compilers are based on the assumption that the hardware is a von Neumann architecture (that is, a single processor with sequential operations). Developing multiprocessor solutions with current compilers requires the developer to be aware of the architecture of the target, as shown in Figure 1a, and embed the details of the multiprocessor behavior in the code. Embedding this target-specific information in the code creates untenable software complexity.

Easing the complexity of programming a multiprocessor or multicore architecture requires a compiler to be aware of all processors in the target architecture, as shown in Figure 1b. The multiprocessor compiler collects global information about the application, such as interprocessor communication, memory use, and CPU load, and uses that information to optimize resource utilization.

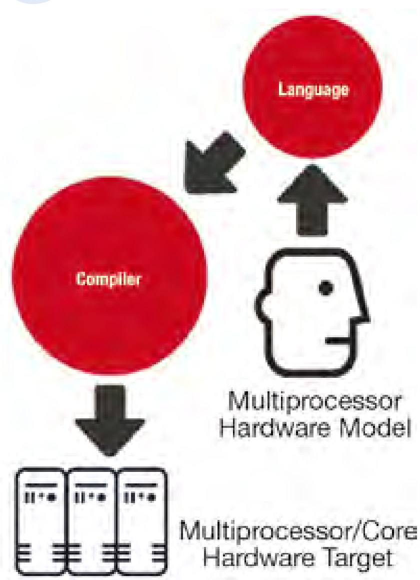


Figure 1a

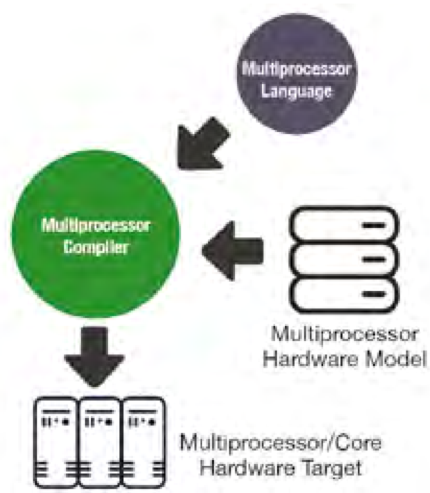


Figure 1b

To make use of a multiprocessor compiler, the programming language must provide the information required to collect this global information. The languages designed to work with von Neumann architectures unfortunately don't provide enough information. Therefore, a new language must be developed alongside the compiler to provide multiprocessor information. This programming language can be built on software libraries as long as they are kept simple with low overhead; libraries encapsulating complex behavior hide the detail required for the multiprocessor compiler to collect global information on the application.

Gedae is a multiprocessor programming language and compiler that targets multiprocessor systems, including multicore architectures such as the Cell Broadband Engine, and chip architectures, including general purpose processors, DSPs, and FPGAs. The following discussion will demonstrate how Gedae can help simplify high-performance software development.

Simple specification of data distribution

In the first example application, a distributed Euler method, multiple cores or processors are used in parallel to efficiently process the data set. The Euler method is an iterative algorithm that performs a 3 x 3 neighborhood operation on a data matrix. To perform this algorithm in parallel, the developer must choose a data distribution of the matrix that minimizes the amount of interprocessor communication. For this example, the data is distributed row-wise in blocks; that is, if there are N rows and P processors, then the first N/P rows are given to the first processor, second N/P rows are given to the second processor, and so on.

For each iteration, every processor calculates a new value for its portion of the matrix. Some of these new values must be shared with adjacent processors to perform the next iteration. With this distribution, rows from adjacent processors must be communicated at each step in the iteration, as shown in Figure 2. Zero rows are inserted as boundary conditions in the top of the 0th processor's data and the bottom of the (P-1)st processor's data. As the Euler method iterates on the data matrix, this data movement ensures each processor has the data necessary to perform the 3 x 3 neighborhood operation. The communication pattern is regular – two rows are transferred to and from each processor at each iteration.

Gedae assists with the implementation of this application by automatically inserting all communication required to process the data set in parallel. As shown in Figure 3, the developer has two tasks: express the arithmetic of the algorithm (as encapsulated in the StepOnce node) and express the data distribution (as done by families of m_selrowK and m_addrows nodes). The specification of the data distribution

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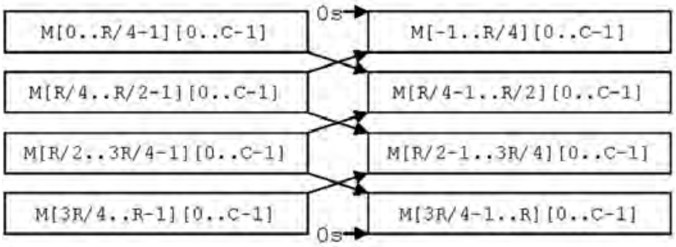


Figure 2

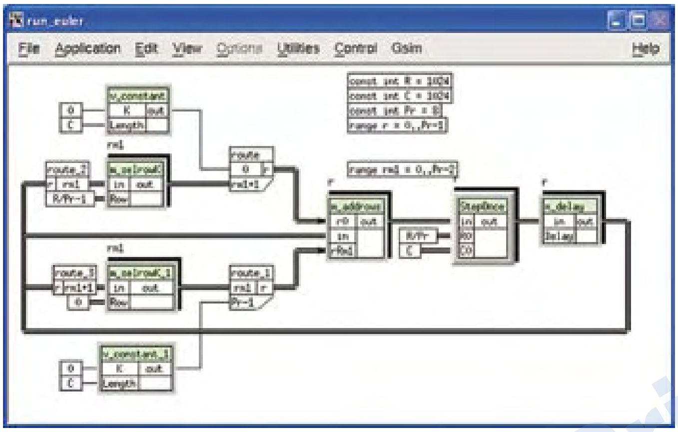


Figure 3

in this flow graph closely mirrors the data movement diagram in Figure 2. The range variables r and rm1 create an array of processing paths called a *family* when applied to the nodes in the graph, as indicated by the shadowing behind the nodes and arcs. The m_selrowK nodes select a row of data from the matrix to transfer to adjacent processors. The v_constant node provides zero rows, and m_addrows concatenates the data from other processors to the rows on the local processor.

To create the parallel implementation, the developer uses Gedae's implementation dialog to map the ith member of the family of nodes to the ith processor in the multiprocessor system. Gedae automatically inserts the necessary communication, but the developer has many degrees of freedom over what is added. In this example, the developer makes sure the communication is nonblocking and DMA transfers are utilized. To process the distributed data efficiently on each processor, Gedae builds its primitives atop a vector library called the *E library*, which provides basic arithmetic and signal processing operations. This E library is a light wrapper over hand-optimized routines created by the hardware vendor.

Dealing with lightweight processors

The second example application is a distributed sort application on a memory-limited architecture where the data set will not fit in a single processor's memory. An example of such an architecture is the Cell Broadband Engine where each of the eight synergistic processing elements has 256 KB of local storage, with a larger bulk storage shared among all PEs. Similar to the finite element analysis in the first example, the data must be decomposed and distributed across multiple processors. However, in this application, memory is also a limiting factor, not just required throughput.

Assume at the beginning of the sort that each processor has N/P data elements where N and P are the data size and number of processors. To sort the distributed array in this algorithm, each processor locally calculates a histogram, and the histograms are collected to determine how the data should be redistributed. Each iteration of the algorithm has two sections of interprocessor communication. The first section collects the histogram on a single processor. This communication contains a small amount of data, but all data must go to and from one processor. Once the histogram is collected, the data redistribution is calculated and the information is broadcast to all processors. The second section of communication is the transfer of array data between processors according to the histogram results. The communication in the data redistribution is not regular; each data element may be sent to any processor, and potentially several elements are transferred during any iteration. Each processor merges the data left from the previous iteration and the new data received from other processors, resulting in sorted local data.

To implement this application, the developer must use memory efficiently so that the generated application fits within the architecture's limited resources. Gedae statically allocates all memory usage and includes several memory-packing algorithms to shrink the size of the allocated buffers. During compilation, Gedae analyzes the memory use at each stage in the statically determined order of execution and determines when each memory buffer can be reused. Memory used in the histogram calculation can be reused in latter parts of the algorithm, such as when data is received from other processors and merged with the remaining local data. Furthermore, the flow graph language provides for the specification of *in-place* streams where inputs and outputs use the same memory buffer. For example, a single N/P in-place buffer on each processor can perform the merge operation in this example.

Gedae automatically inserts and manages all communication needed to sort the data, freeing the developer to concentrate on the algorithmic details of performing a distributed histogram and determining the data redistribution at each step. While the Euler method example has only 2*(P-1) transfers per iteration, this example adds many sends and receives to create the implementation. This inserted communication is displayed as green (send) and red (receive) bars in the Trace Table, as shown in Figure 4. The row labeled part_control in the table shows the execution of the distributed histogram calculation. This row is collapsed so that all the components are displayed in one line, and in this line the several send and receive pairs dominate the execution time of this portion of the application.

The rows labeled vui_part_vvui show each processor partitioning the data after being told by the control processor how to redistribute it, and the vvui_nconcat_vui and vui_sort rows show each processor combining and merging the new data with the old. In this example, Gedae minimizes the work the developer has to do to implement the intricate communication patterns and helps make sure the application remains memory efficient.

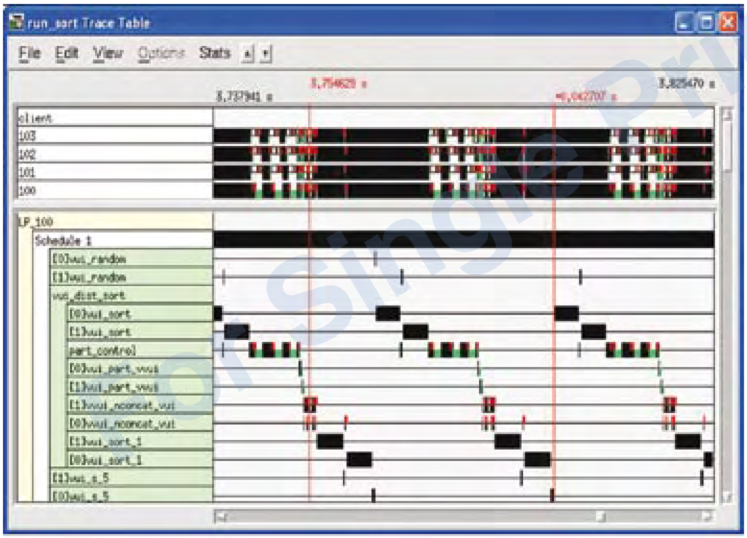


Figure 4

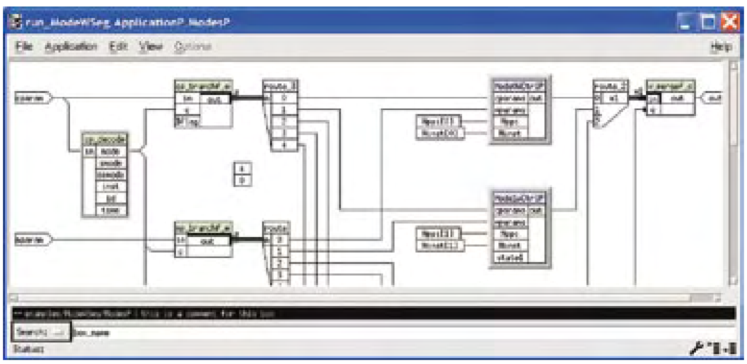


Figure 5


Figure 6

Model-driven development deployed

The third example application is a radar application, which has two different operation modes and must process data at a high data rate. To meet this high data rate, each processor must be highly utilized. Because different modes have different execution times and require a different number of processors to execute, the load must be balanced by sending data to idle processors to reach high utilization. This example application has two modes. Mode A only requires one processor and has a short duration. Mode B requires two processors, and its duration is four times as long as Mode A. A round-robin scheduling algorithm is used for managing which processors are busy and determining where to process the next mode; that is, a manager processor keeps track of which processors are busy and sends new instances of modes to the first idle processor in the queue.

Gedae helps the developer solve this problem by simplifying the operation modes' specification and bringing the scheduling algorithm to the forefront while automating its implementation and data movement. The operation modes' specification is shown in Figure 5. This flow graph is executed on each of the processors. The scheduling algorithm determines which processor to process the mode on and sends this data downstream in a packet. When the processor is idle, it waits for a packet on the source of this flow graph. When it receives a packet from the control processor, the cp_decode node decodes it, extracting the mode ID, and branches the data to the subgraph, which implements the desired mode of operation. Thus, any processor can execute either mode, with the scheduling algorithm instructing each processor when to start processing data and which algorithm to use on that data.

This round-robin scheduling algorithm aptly utilizes multiple processors. Figure 6 shows a Trace Table for this radar application. The horizontal black bars indicate the processor is busy. The long black blocks on processors 101 and 102 indicate an execution of Mode B where the duration is four times longer than that of Mode A. If Mode B is not being run, the round-robin scheduler is free to send instances of Mode A to the processors used by B, as shown in the application's trace. This example implementation is inspired by an actual deployed radar system where the software modes, mode control, and dynamic load balancing were implemented, distributed, and deployed with Gedae.

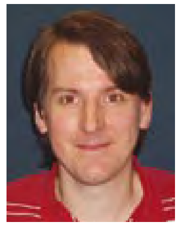
Exposing what is pertinent; automating what is mundane

Creating high-performance software requires both moving data into fast memory and processing data once it gets there. To assist with high-performance software development, the Gedae model-driven development tool automates the mundane details so the developer does not have to implement them.

Further, Gedae exposes the pertinent details so the developer can code and optimize the application more effectively. Data distribution is a natural part of the flow graph language, as shown in the Euler method example. By directly accessing the vendor's optimized vector library, the application can run efficiently. Intricate communication patterns are implemented automatically, as shown in the array sort example, and the generated implementation's communication web can be easily viewed in the Trace Table. Fully deployed software systems can also be created, such as in the radar example where a round-robin scheduling scheme distributes tasks of different duration and processing requirements on many processors. Gedae significantly simplifies high-performance software development without detriment to the delivered product's efficiency. ECD

William Lundgren *is cofounder, president, and CEO of Gedae, Inc. William started his professional career at Corning Glass Works as a product development physicist. He later worked at the U.S. Air Force Institute of Technology and the U.S. Air Force Research Laboratories developing new speech and audio processing technologies. After leaving active duty in 1985, he moved to RCA Advanced Technology Laboratories, which became Lockheed Martin, and spent 16 years leading Gedae development. William has a BS in Physics from Rensselaer Polytechnic University, BS and MS degrees in Electrical Engineering from the U.S. Air Force Institute of Technology, and is All But Dissertation for his PhD in Electrical Engineering from the University of Pennsylvania.*

Kerry Barnes *is chief scientist and a founding member of Gedae. Before joining Gedae, Kerry was a principal member of the engineering staff at Lockheed Martin, ATL where he was responsible for signal processing systems software/hardware, single-chip FFT design, direct digital frequency synthesizer design and implementation, and various software tools and applications development projects. He earned a BS in Electrical Engineering from Lehigh University and an MS in Computer and Information Science from the University of Pennsylvania.*



James Steed *is director of software development and a founding member of Gedae. Prior to Gedae, James worked at Lockheed Martin where he was responsible for developing the embeddable library of functions, including testing and creating a database and search utility. His most prominent project is the development of Gedae's new RTL language. James earned a BS in Computer Science from Cornell University and an MS in Computer Science from North Carolina State University.*

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What is Gedae?

Gedae is an integrated application development environment. It has a language for describing an architecture-independent functional specification, a multiprocessor virtual machine, and a multiprocessor compiler that transform the specification into one that runs on a virtual machine. The following topics are key to understanding Gedae:

- **Language:** The language was developed with two requirements: All functionality must be easily expressible and the language must be transformable into an efficient implementation on the virtual machine. The Gedae language consists of the Gedae Primitive Language and the Gedae Graph Language. The Primitive Language is geared toward expressiveness, while the Graph Language allows for the hierarchical development of graphs containing primitives, parameters, and other Gedae graphs. The resulting language permits direct expression of signal and data processing algorithms, distribution for providing load balancing and fault tolerance, and application control.
- **Virtual machine:** The language and machine were codesigned to achieve maximum efficiency. The virtual machine contains a runtime kernel that executes components generated by the compiler. The virtual machine also allows for vendor-specific processing optimizations, such as setting data transfer parameters. A thin layer over the vendor-provided vector-processing libraries allows primitives to execute efficiently.
- **Compiler:** As the central part of Gedae, the multiprocessor compiler builds an efficient application from code expressed in the Gedae language to run on the Gedae virtual machine. The compiler passes are automated but can be guided by the user-supplied implementation parameters to control distribution, strip mining, data transfers, scheduling priorities, queue policies, and memory management.

COMPONENT-LEVEL MODULES

Microchip Technology, Inc.

Website: www.microchip.com
Model: MCP3909 **RSC No:** 32820

The MCP3909 energy-measurement IC and reference design (Part# MCP3909RD-3PH1) enable designers to develop and bring meter designs to market quickly • Supports IEC 62053 International Energy-Metering Specification and legacy IEC 1036/61036/687 specs • Digital waveform data access through SPI interface • 16-bit dual ADC output words, 20-bit multiplier output data words • Dual functionality output pins support serial interface access and simultaneous active power-pulse output • Two 16-bit, second-order, Delta-Sigma ADCs with multibit DAC • 0.1 percent typical active energy-measurement error over 1000:1 dynamic range

COUNTER/TIMER

EuroTecH SpA

Website: www.eurotech.it
Model: Passenger Counter **RSC No:** 32804

Eurotech has released the PCN-1001 Passenger Counter based on noncontact stereoscopic vision detection technology • This new technology and advanced interpretation algorithm result in a high detection accuracy exceeding 97 percent under all lighting conditions year round • The reliable bidirectional counting results in correct and precise data that can be used for statistical or data interpretation • Date and time information can be stored together with passenger count information • Robust, lightweight, and reliable • Easy installation and setup • Stereoscopic cameras • Adjustable optical panel • Low power consumption • IP65 Environmental protection grade index • High precision counting accuracy (>97 percent) • Extended temperature range (EN50155 class T1) , -25 °C to +55 °C • ECE/ONU Reg. 10

GuideTech

Website: www.guidetech.com/flash.htm
Model: GT 658 **RSC No:** 32781

Ultra-fast, high-resolution DC – 400 MHz Time Interval Analyzer (TIA) • Ideal for most PC-based lab bench (timing) test applications • Patented TIA substantially increases measurement speed, and the measurements are displayed as a function of time • Continuous time correlation to a common reference between all measurement time stamps • Makes measurements not previously possible with traditional counters

DATA RECORDERS

TEK Microsystems, Inc.

Website: www.tekmicro.com
Model: JazzStore UWB **RSC No:** 32687

2 GSps RT Data Recording Solution • Continuous recording/playback at rates up to 2 GSps (8-bit samples) or 1.6 GSps (10-bit samples) • Sample accurate trigger modes of operation available to support record and playback at 2 GSps (10 bits) with up to 80 percent duty cycle • FAT 32-based filing system providing seamless access to recorded data from standard Linux or Windows workstation environments • Complete hardware solution within two slots of a standard VXS (VITA 41) backplane environment • Scalable storage capacity through the use of up to six dual Fibre Channel RAID systems • Up to 24 TB available storage capacity • Storage capacity allows for in excess of two hours' worth of 2 GSps samples • Recording system control through standard Windows GUI or from the customer's own software applications through API library • Support for VxWorks, Windows, and Linux operating systems

DEVELOPMENT PLATFORM

Embest Info&Tech Co., Ltd.

Website: www.armkits.com
Model: STR750 Board **RSC No:** 32792

A low-cost evaluation board based on the STR750FV2T6 processor, which is a new series of super-integrated, single-chip, 32-bit, ARM7-based MCUs from STMicroelectronics • Dimensions: 150 mm x 116 mm • Working temperature: -40 °C to +85 °C • Processor: STR750FV2T6 ARM7TDMI-S 32-bit RISC CPU running up to 60 MHz with embedded 272 KB (256 K + 16 K + 32 K) flash memory and 16 KB SRAM memory • Power input: +5.0 V/1 A • USB 2.0 interface (device)

DEVELOPMENT TOOLS

Strategic Test

Website: www.strategic-test.com
Model: TDK-4 **RSC No:** 32785

The TDK-4 is a development kit for the 806 MHz TRITON-320 processor • 6" x 4" carrier board with socket for TRITON-320 SODIMM • UCB1400 codec and touch-screen controller • CompactFlash and SD/MMC socket • 10/100 Mbps Ethernet • USB 1.1 • Three RS-232 and a JTAG interface • TRITON-320 806 MHz PXA320 SODIMM module (128 MB SDRAM and 64 MB flash memory) reloaded with Linux or WinCE • Includes comprehensive manual • Includes 12 months of technical support • Windows CE 6.0 and Linux 2.6.17

DSP RESOURCE BOARDS: FPGA

TEWS Technologies LLC

Website: www.tews.com
Model: TCP630 **RSC No:** 32519

A low-cost, user-programmable, FPGA-based CompactPCI module designed for industrial, military/aerospace, and transportation applications • Standard 3U 32-bit CompactPCI module conforming to PICMG 2.0 R3.0 with user-configurable Xilinx FPGA • Flash device in-system programmable • 32-bit PCI target interface by PLX PCI9030 • FPGA clock options: local clock oscillator/PLL programmable clock generator (200 KHz-166 MHz), six clock outputs connected to FPGA • I/O lines: 64 TTL I/O or 32 differential I/O or 32 TTL I/O and 16 differential I/O (TPMC630-12)/TTL signaling voltage (maximum current: ±24 mA) or EIA-422/-485 signaling level/direction individually programmable • I/O access: 64 I/O lines via a PIM module, parallel to up to 64 I/O lines on rear connector J2 • Operating temperature: -40 °C to +85 °C

GATEWAYS

Lantronix

Website: www.lantronix.com
Model: XPort Direct **RSC No:** 32794

The compact XPort Direct embedded device gateway module delivers network connectivity to virtually any electronic product with a serial interface on its host microcontroller • Manufacturers can now affordably offer network connectivity as a standard feature, greatly enhancing product value and enabling a host of applications such as remote monitoring, networked control, data acquisition, and Internet content streaming • Affordable network connectivity gateway for any device with a serial interface on its microcontroller • Integrated module with RJ-45 featuring dedicated networking SoC • Complete TCP/IP protocol stack and Windows deployment software • Up to 230 Kbps data rate • Compact low profile (<12 mm) • 2 x 12 pin, 2 mm headers • Two GPIO pins • RS-232/485 ready

GPS/PRECISION TIME CODE

Aeroflex

Website: www.aeroflex.com
Model: 6103 AIME A-GPS **RSC No:** 32696

Aeroflex introduces Assisted GPS (A-GPS) support on the 6103 AIME for device R&D and on the 6103 AIME/CT for conformance testing • A-GPS and GSM/(E)GPRS MS air interface protocol development and conformance test system • Comprehensive suite of all 33 3GPP TS 51.010 section 70 A-GPS test cases • Full integrated logging facility of all Layer 3 RRLP messaging • Integrated high-performance 12-channel GPS satellite simulator • Available as an upgrade to the widely used 6103 AIME and AIME/CT systems • Automation provides a quick and effective method for long, repetitive GPS test runs • Easy decoding of RRLP messaging makes identifying protocol issues quick and easy • No need for frequent field testing in networks where you have no control over network behavior • Accelerate product development for emerging location-based services markets in North America, Europe, and Asia

MASS STORAGE: SOLID-STATE DISK

VMETRO

Website: www.vmetro.com
Model: VMDRIVE Solid State **RSC No:** 32694

Designed to meet demanding military and aerospace applications, the VMDRIVE deploys 40 or 80 GB solid-state storage in rugged, conduction-cooled or commercial, air-cooled environments • 40 or 80 GB storage for 6U VME or CompactPCI form factors • Dual 2 Gbps Fibre Channel interfaces • Commercial air-cooled or rugged conduction-cooled build options • Combines two or more units for rugged SAN

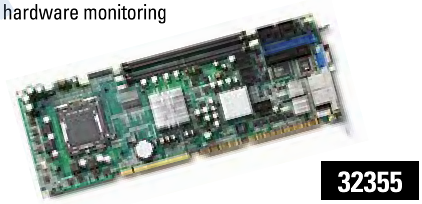
32694

PROCESSOR: PENTIUM 4

ADLINK Technology, Inc.

Website: www.adlinktech.com
Model: NuPRO-851 **RSC No:** 32355

Full-size Intel Pentium 4 (LGA775) processor SBC with DDR2, VGA, dual GbE, SATA, and USB 2.0 • High computing capability, supports 800 MHz FSB with Hyper-Threading Intel Pentium 4 (LGA775) processor • High communication bandwidth, supports two PCI Express x1 GbE ports • Supports SATA for high-speed storage devices • Support USB 2.0 and generic features, including VGA, COM, keyboard, mouse, and hardware monitoring



32355

SERVERS

Motorola Inc., Embedded Communications Computing

Website: www.motorola.com/computing
Model: Centellis 3406 Server **RSC No:** 32577

Fully integrated and verified AdvancedTCA communications server platform • 14-slot, 12.5U, 19" shelf allows designers to fit three in a standard telco rack with room for ancillary equipment • Redundant shelf management, fan trays, and power-entry modules • Redundant PICMG 3.0 and 3.1 base/fabric switching blades • Redundant processor complexes for HA middleware or user applications • Verified shelf-level thermals and PICMG standard compliance • Combined system control and switching blades maximize billable application payload • Variety of payload blades available • Integrated operating environment, including Carrier Grade Linux • RoHS complaint (five of six), architected to 5-nines reliability and availability • Designed for NEBS and ETSI compliance • Applications include wireless infrastructure, packetized voice, wireline data, and cable network head-end equipment • Dual star configuration support for base and fabric interfaces • Includes choice of one or two ATCA-F101 system controller and switching blades

NEW PRODUCTS

SOFTWARE: DEVELOPMENT TOOL

Altia Inc.

Website: www.altia.com
Model: DeepScreen 5.0 **RSC No:** 32775

Automatically generates deployable, complete graphics source code for user interfaces drawn in Altia Design • Generate tight, 100 percent deployable source code • Built-in support for common graphics libraries (WindML, Photon, X11, OpenGL, Win32, and others) • Small footprint custom graphics libraries for targets that don't already have a GL (even down to 8-bit micros) • Users can draw their graphics in Altia Design, and DeepScreen generates the code to draw the GUI • Light, robust API for connecting generated graphics code to application code • Switch between target RTOSs with the push of a button • Complete, certifiable source code • Suitable for tanks, cars, and medical devices

32775

SOFTWARE: OPERATING SYSTEM

Green Hills Software, Inc.

Website: www.ghs.com
Model: INTEGRITY 10 **RSC No:** 32510

The 10th anniversary edition of the INTEGRITY RTOS • Features new security, performance, and usability features • Suitable for a wide range of industries including consumer, networking, medical, automotive, industrial, and avionics • Supports Symmetric Multi-Processing (SMP) wherein the operating system will automatically load balance applications across multiple cores on SMP-capable processors such as the Freescale Power Architecture-based 8641D • Supports NonUniform Memory Architecture (NUMA) systems in which applications are intelligently allocated and distributed across multiple cores that have their own fast local memory • Includes a new debug agent that enables debugging of application programs with minimal real-time overhead and improved performance • Debug agent provides a significant performance boost for on-target event logging used by the MULTI EventAnalyzer • EventAnalyzer provides a graphical view of system behavior, including context switches, interrupts, system calls, and interprocess communication, and is used by developers for performance tuning and to find difficult bugs such as deadlocks and race conditions • Integrated with version 5 of the MULTI IDE and includes a new project manager • Features new kernel awareness debugging features that provide increased visibility into kernel object state during application development • New security features including a memory resource lending capability for the secure and efficient distribution and revocation of resources, and a new "pure virtual" device driver model that enhances INTEGRITY's unique driver architecture to further maximize system reliability while minimizing security and safety certification costs

SYSTEM BOARDS

Innovative Integration

Website: www.innovative-dsp.com
Model: P25M DSP/FPGA PCI **RSC No:** 32697

New P25M PCI card with Texas Instruments TMS320C6713 flexible DSP plus a reconfigurable FPGA accelerates system development • Features a 300 MHz C6713 DSP (floating point) user-configurable Spartan-3 FPGA • Four 25 MSps – 16-bit A/D • Four 50 MSps – 16-bit D/A • PCI 64-bit/66 MHz precision low-jitter sample clock • Extensive software support in source form • P25M board can be configured or modified to fit specific requirements and provides an optimal mix of performance, cost, and features • Custom logic development supported for FPGA DSP/BIOS peripheral drivers • Applications: PCI-based real-time control, stimulus-response measurements, high-end data capture and playback, industrial high-speed controls, and OEM instruments

SYSTEM MONITORING

One Stop Systems, Inc.

Website: www.onestopsystems.com
Model: OSS-SYSMON2 **RSC No:** 32790

A system monitor and control board designed to track and display operational parameters • Easily located inside system enclosure • Monitors and communicates vital system parameters to remote PC • System alarms sent to host via a 100BASE-T Ethernet connection

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TELEPHONY: GENERAL

Telesoft Technologies

Website: www.telesoft-technologies.com
Model: MPAC Conference **RSC No:** 32776

Telesoft has added conferencing support (voice conference) as an option for its CompactPCI telephony blades • This feature can be added to the MPAC 2416 and MPAC 5600 card, providing a dense and flexible conference card resource for developers to embed within voice systems • The MPAC 5600 card supports up to 384 individual conferences, with a maximum limit of 16 parties per conference • Specific applications may demand a smaller number of conferences with a greater number of parties, and this can be configured and supported on a bespoke basis based on the customer's demand • The conferencing application supports a total of 1,536 inputs to the conferencing facility (such as speakers) and 1,536 outputs from the conferencing facility (such as listeners) • The conferencing software will mix the three loudest speakers and then send those to the output

TEST SYSTEMS

Aeroflex

Website: www.aeroflex.com
Model: WCDMA ACE **RSC No:** 32817

3G protocol analysis test system • Powerful network emulator for integration, regression, and preconformance testing of WCDMA terminals • Full protocol decode and debugging tools • 3GPP Release 99, Rel-5 HSDPA, and Rel-6 HSUPA capable • Supports early development of protocol test scenarios • Compact, one-box solution with integrated PC • Emulation of up to three cells to enable handover testing • Built-in fading simulator option • Powerful, state-of-the-art test development environment allows testing on partial or complete terminal designs • Proven GUI features with a track record of boosting engineering productivity

TURNKEY SYSTEM

Advantech Corporation

Website: www.advantech.com
Model: TREK-756 **RSC No:** 32800

The TREK-756 has a heating mechanism inside a tough, dustproof, waterproof, and fanless aluminum chassis for dependable operation when moving between extreme environments at -30 °C to 50 °C (-22 °F to 113 °F) • Bigger and brighter screens • Built on the RoHS design of the TREK-755 • Sometimes hot, sometimes cold, but reliable • The TREK-756 is designed for tolerance of extreme environments and enhanced reliability • Fits into any infrastructure • In addition to working in a wide range of temperature and lighting scenarios, TREK 756 can accept standard 24 Vdc vehicle power inputs; 802.11a/b/g, GPS, GPRS, and GSM wireless modules; Linux, Windows XP, CE .NET 4.2, and XP Embedded operating systems; and VESA arms or RAM mount kits

WIN Enterprises Inc.

Website: www.win-ent.com
Model: PL-01030 **RSC No:** 32528

Fanless Micro PC with AMD LX800 processor • Low power requirements: 12 W, 5 V at 2.4 A • Compact: 218 mm (H) x 132 mm (D) x 51 mm (W); 8.6" (H) x 5.2" (D) x 2" (W) • Fanless operation • Onboard AMD Geode LX800 500 MHz processor • Two 10/100 LAN Ethernet interfaces • Four USB 2.0 ports

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Video frames caught on USB

USB is living up to its name as the *Universal Serial Bus.* Nearly every compute platform has a USB interface available for connecting additional functionality to the platform. The latest USB frame grabber from Sensoray, Model 2255, successfully fills industry's need for a multichannel, low-latency, USB video-capture device. Boasting an impressive total capture rate of 60 frames per second (fps), the 2255 allows for simultaneous video capture of up to four composite NTSC or PAL video sources at 15 fps or two channels at a full 30 fps. Monochrome or scaled-down modes enable full frame-rate capture across all channels simultaneously.

The 2255 supports a variety of output formats that eliminate the need for format conversions in a wide range of applications. Supported formats include: RGB packed, YCrCb packed, YCrCb planar, and Y8.

Powered through the USB 2.0 connection on a PC, the 2255 does not need an external power supply. The supplied software development kit contains the drivers for Linux and Windows, the API, and a demo program that illustrates how to use the API. The driver supports multiple units, allowing for easy system expansion and integration.

Sensoray • Model 2255

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