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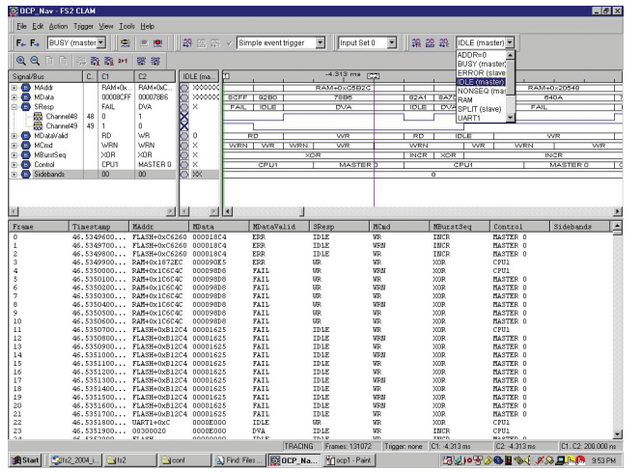
FS2 Bus Navigator™

The FS2 Bus Navigator™ is used for monitoring signal activity and for debugging complex bus/system interactions in System-on-Chip (SoC) designs. It allows the user to capture bus activity in real time and display critical information for analysis on a host PC for faster debugging and verification of the design.

The system consists of an On-Chip Instrumentation (OCI®) synthesizable logic block, a JTAG hardware probe, and PC-based software for controlling probing and analysis. The OCI transparently captures bus activity, buffers it using on-chip RAM, and transfers the collected data off-chip via a JTAG port to the external JTAG probe. The host PC controls the trace collection process and provides captured bus history to the user with an easy-to-use graphical interface.

The OCI block is synthesized into the SoC design. The OCI block monitors all the bus signals sampled with the processor clock. Signals include address data combined from the read and write data buses, and all critical control and status signals. Additional signals can be hooked up to any nodes in the SoC, such as interrupt requests, peripheral status, and CPU control signals. The additional signals can also be used to recognize specific on-chip activity outside the bus and transmitted to the probe for triggering purposes.



FEATURES:

- Captures bus activity in real time
- Available for custom buses, AMBA, OCP, and Sonics SiliconBackplane buses
- Captures bus signals and additional user-defined inputs attached to other nodes in the SoC
- Bus clock mode trace stores signals on every clock
- Bus transfer mode aligns bus transfers and response phases for single event triggering using combinations of address, data, and control
- Filtering of wait and idle state cycles in bus transfer mode
- Trace storage qualifiers; single cycle, start or stop trace on any trigger, counter, and state sequencer condition
- Configurable for user-defined number of Masters
- Trace buffer stores bus cycles or bus transfers based on RAM memory size
- Up to 16 user-defined triggers recognize combinations of 1, 0, X, signal values
- Sequential event monitoring using cascading trigger states
- User-definable time stamp records duration of each trace frame from the start of trace, displayable as absolute or delta times
- Optional VCD format export for integration with simulation environments

For more information, contact: info@fs2.com **RSC# 24317 @ www.embedded-computing.com/rsc**