

Lattice Semiconductor

5555 NE Moore Ct. • Hillsboro, OR 97124
Tel: 503-268-8000 • Fax: 503-268-8347
www.latticesemi.com



LatticeECP2 FPGAs

The LatticeECP2 (Economy Plus 2nd generation) family redefines the low-cost FPGA category. By integrating features and capabilities previously only available on higher cost, high-performance FPGAs, this family dramatically expands the range of applications that can take advantage of low-cost FPGA products.

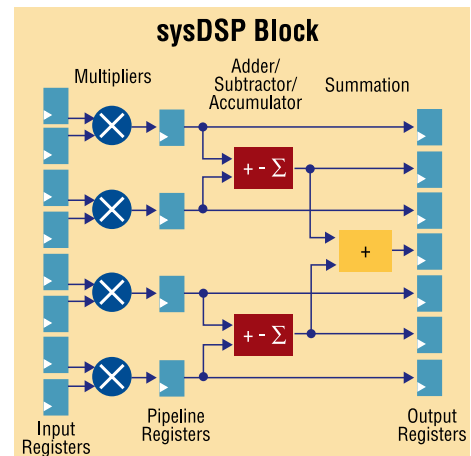
Features that the LatticeECP2 family brings to the low-cost FPGA category include high-performance DSP blocks, up to 70K LUT capacity, support for DDR1/2 memory interfaces at 400 MBps and up to 840 MBps generic LVDS performance. The LatticeECP2 also provides enhanced FPGA configuration options with features such as dual boot, bitstream encryption, and TransFR I/O capability.

LatticeECP2 FPGA devices include between three and 22 sysDSP blocks. sysDSP blocks support four functional elements in three data path widths: 9, 18, and 36. The resources in each sysDSP block can be configured to support the following four elements: MULT, MAC, MULTADD, and MULTADDSUM.

The number of elements available in each block depends upon the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP. Each sysDSP block can be clocked at 325 MHz yielding a total DSP capability of up to 28,600 Million Multiply Accumulates per second (MMACs)!

ispLeverCORE Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used DSP functions, including: FIR Compiler, FFT Compiler, NCO, Reed Solomon Encoder/Decoder, Viterbi Decoder, Convolutional Encoder, and more. Go to www.latticesemi.com/products/intellectualproperty for a complete listing of IP.



FEATURES:

- Low-cost FPGA optimized for mainstream applications
- Up to 22 high-performance sysDSP blocks per device
- sysDSP blocks are optimized for processing intensive applications and allow designers to quickly implement DSP functions
- sysDSP blocks provide configurable multiplier widths: one 36 x 36, four 18 x 18, eight 9 x 9
- sysDSP blocks provide programmable addition, subtraction, and accumulate modes
- sysDSP blocks offer programmable pipelining – input, intermediate, and output
- One LatticeECP2 device can provide up to 28,600 Million Multiply Accumulates per second (MMACs)
- LatticeECP2 FPGAs support an extensive IP portfolio
- Support for Matlab/Simulink software