Synplicity, Inc.
600 West California Avenue • Sunnyvale, CA 94086
Tel: 408-215-6000 • Fax: 408-222-0263
www.synplicity.com

Synplicity®
Simply Better Results

Synplify DSP

Advanced FPGAs are the perfect vehicle for high performance DSP applications. Hundreds of millions operations per second can be achieved, and dedicated DSP blocks and multipliers facilitate efficient and parallel implementation of DSP functions. However the traditional implementation path of hand-coding the RTL often is error-prone and time consuming, with numerous iterations between the algorithm architect and the hardware designer. With Synplify DSP you can model and simulate your algorithms quickly, and automatically create optimized RTL implementations for a wide range of target devices.

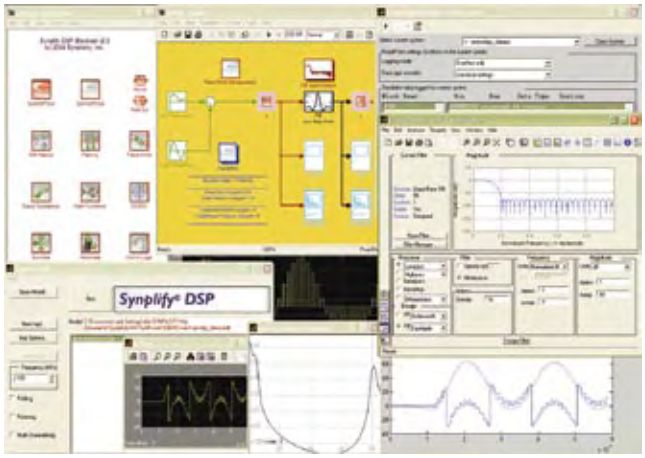
Automated RTL implementation – The Synplify DSP product automatically generates RTL and a verification test bench from a Simulink system-level specification. No hand-coding of any RTL is required.

The Synplify DSP blockset – Synplify DSP provides a set of functional blocks commonly used in DSP design including filtering (FIR, IIR), transforms, math functions, CORDIC, signal operations, memories, and control logic. These functions are technology-independent and tightly integrated into The MathWorks environment, allowing the algorithm designer to utilize Simulink features such as discrete-time simulation, multi-rate management, fixed point quantization, scope debugging, and more.

FPGA hardware independence – Synplify DSP allows algorithm behavior to be captured in Simulink without preselecting the specific FPGA device for implementation. The Synplify DSP toolbox automatically implements an optimized architecture in RTL based upon your timing and area requirements.

Multi-channel system from single-channel specification – Synplify DSP enables quick what-if analysis on channel capacity by automatically generating a pipelined system from a single channel specification.

Area-speed tradeoffs – Math intensive DSP algorithms easily consume large numbers of expensive hardware functions such as multipliers. The Synplify DSP tool analyzes the design to automatically find opportunities for sharing these resources, saving design iterations and significant area.



FEATURES:

- Rapidly create high-level, technology independent DSP models with fully integrated Synplicity fixed-point DSP library
- High quality RTL code and testbench automatically synthesized from Simulink model
- DSP synthesis – DSP architecture optimizations such as system-level re-timing for performance and folding for area utilization
- Extensive floating-point to fixed-point conversion and analysis
- Vector support – concise expression of parallel and multi-channel operations
- Powerful system-wide optimizations for performance, area, and multi-channelization tradeoffs
- Technology independence allows targeting any FPGA architecture from the same Simulink model
- M-control – use a subset of M-language to describe complex state machine and control logic
- Multi-channelization – automatically produces a resource optimized multi-channel implementation from a single channel specification
- Integrated quantization and multi-rate analysis – accelerate design and verification of fixed-point multi-rate DSP algorithms
- Automatic datatype propagation propagates type and adjusts word width to avoid overflow saving manual calculation and implementation
- Synplify DSP blockset – hardware abstraction focuses on algorithm behavior, separates implementation details and enables full portability

For more information, contact: info@synplicity.com

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