

Synplicity, Inc.

600 West California Avenue • Sunnyvale, CA 94086

Tel: 408-215-6000 • Fax: 408-222-0263

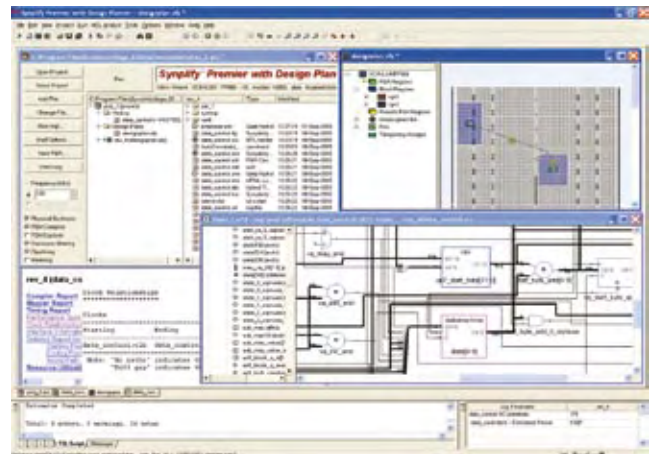
www.synplicity.com**Synplify Premier**

Synplicity's Synplify Premier software is the ultimate FPGA synthesis and debug solution. It builds upon Synplicity's industry-leading synthesis technology, and adds new graph-based physical synthesis for timing closure and simulator-like visibility into operating FPGA devices for fast source-level debug.

Graph-based physical synthesis – Synplicity invented graph-based physical synthesis to improve timing closure by means of a single-pass physical synthesis flow for 90 nm FPGAs. In FPGAs, unlike ASICs, proximity of placed logic does not imply better timing. The essence of the graph-based approach is that pre-existing wires, switches, and placement sites used for routing an FPGA can be represented as a detailed routing resource graph. The notion of distance then changes to a measure of delay and availability of wires. The Synplify Premier tool's graph-based physical synthesis technology merges optimization, placement, and routing to generate a fully placed and physically optimized netlist, providing rapid timing closure and a 5 percent to 20 percent timing improvement.

Best quality of results – The Synplify Premier product is a true timing-driven synthesis product, which means it delivers the timing performance you need in your design by automatically moving registers within combinatorial logic in order to balance timing delay and improve circuit performance up to an additional 20 percent Quality of Results (QoR).

Simulator-like visibility into a live FPGA – The Synplify Premier software provides a rapid method of finding functional errors in FPGA designs by providing simulator-like visibility into operating FPGA hardware. Synplicity's integrated debugging software, based upon technology from the Identify product, allows designers to annotate signals and conditions they want to monitor directly in their RTL code.

**FEATURES:**

- Graph-based physical synthesis – fast timing closure and a push-button performance boost of up to 20 percent
- True timing-driven synthesis – after meeting timing constraints, automatically optimizes your design for area/cost
- Automatic handling of DSP functions – infers DSP functions from RTL and maps into vendor's DSP hardware (i.e. MACs)
- Lightning-fast compile times – synthesizes even the largest design in a fraction of the time of other tools
- HDL analyst RTL analysis and debugging tool – instantly generates RTL block diagrams from your RTL code; helps identify critical paths
- Interactive timing analysis – enables point-to-point timing analysis without re-synthesis
- Automatic RAM inferencing – bypass tedious hand instantiation of RAM and makes your design technology independent
- FSM explorer – automatically finds and selects the best FSM coding style for the meeting your timing and area constraints
- Automatic retiming – moves registers automatically within combinatorial logic to balance delay and improve performance
- Integrated RTL instrumentation and debug – instrument and debug your design directly in your RTL source code
- Probe point creation – allows any signal to be tied to an external pin for testing without HDL code changes