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Synplicity®
Simply Better Results

Synplify Pro

The Synplify Pro product achieves industry-leading QoR by incorporating several advanced optimization techniques including Synplicity's proprietary Behavior Extracting Synthesis Technology (BEST). By extracting behavior such as Finite State Machines (FSM), multipliers, and memories from RTL code and starting synthesis at this level, the Synplify Pro product optimizes your design globally for improved performance and at the same time can run faster and handle larger designs than alternative synthesis tools. Another important technique for improved performance is retiming. By selecting a switch, you can tell the tool to automatically move registers inside combinatorial logic in order to balance timing delay and improve circuit performance by as much as 20 percent. Retiming may be used on a global level or selectively.

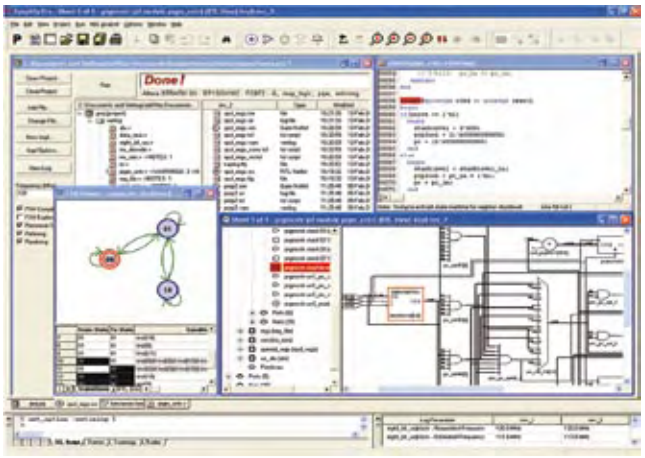
The HDL Analyst RTL graphical analysis and debugging tool provides instant graphical views of both high-level block diagrams and gate-level schematics linking back to the RTL source code, making debug and code optimization fast and easy. Critical paths of your design are quickly highlighted and linked back to your RTL source.

The FSM Explorer automatically finds state machines in your design, then evaluates alternative encoding styles and selects the one giving the best solution for the specified timing constraints. FSMs are displayed as bubble diagrams, providing an easy-to-read graphical representation of your results.

Synplicity's MultiPoint synthesis technology provides a unique and superior approach to incremental design. User-defined compile points and intelligent, difference-based synthesis technology provides a high level of design stability for incremental changes without the performance penalty of other incremental design styles.

The Synplify Pro solution offers a formal verification mode where optimizations are recorded and passed on to tools such as Cadence's Conformal product for this purpose.

The Synplify Pro tool interfaces to popular HDL simulators and is tightly integrated with place and route tools from Actel, Altera, Lattice, QuickLogic, and Xilinx.



FEATURES:

- Technology independence – target all popular FPGAs from one RTL and constraint source
- Proprietary BEST algorithms – globally optimized designs in a fraction of the time required by traditional synthesis tools
- True timing-driven synthesis – after meeting timing constraints automatically optimizes for area/cost
- Comprehensive language support – supports Verilog, VHDL, System Verilog, and mixed-language designs
- Automatic RAM inferencing – bypass tedious hand instantiation of RAM
- Lightning-fast compile times – synthesizes even the largest design in minutes
- Automatic retiming – moves registers automatically within combinatorial logic to balance delay and improve performance
- Pipelined multipliers and ROMs – automatic register balancing of pipelined multipliers and ROMs for faster circuit performance
- FSM Explorer – automatically finds and selects the best coding style option for the fastest performance
- Graphical state machine viewer – fast debugging and documentation for all state machines in your design
- HDL analyst RTL analysis and debugging tool – instantly generates an RTL block diagram from HDL code; helps identify critical paths
- MultiPoint synthesis – provides a superior methodology for incremental design

For more information, contact: info@synplicity.com

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