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## Altera DSP Builder

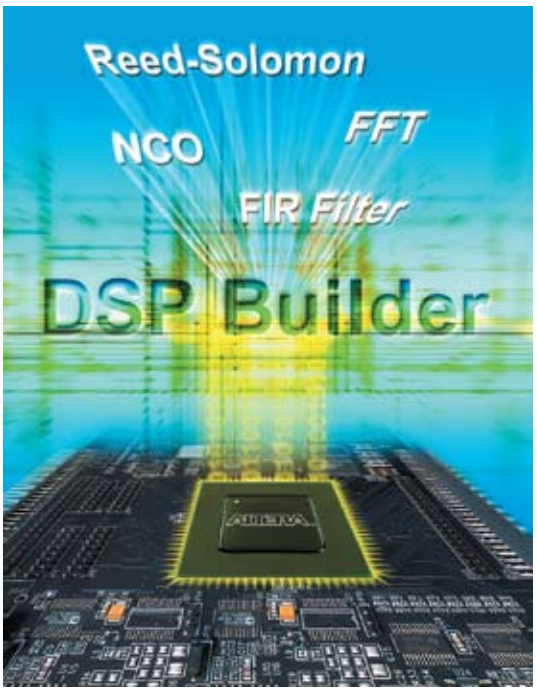
Digital Signal Processing (DSP) system design in Altera® FPGAs requires both high-level algorithm development and HDL development tools. Altera's DSP Builder integrates these tools by taking the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB/Simulink system-level design tools and combining them with VHDL synthesis, simulation, and Altera's Quartus® II development tool. Using DSP Builder, you can target your design to any Altera FPGA – including the latest device architectures such as the 40 nm Stratix® IV family – and effortlessly retarget it if your needs change.

Altera's DSP Builder technology shortens DSP design cycles by helping you create the hardware representation of a DSP design in an algorithm-friendly development environment. With this tool, you can quickly go from system definition and simulation using industry-standard MATLAB/Simulink tools to system implementation. The DSP Builder Signal Compiler block reads Simulink Model Files (.mdl) that are built using DSP Builder and MegaCore® blocks and generates VHDL files and Tcl scripts for synthesis, hardware implementation, and simulation.

DSP Builder features the Advanced Blockset capability supporting timing-driven Simulink synthesis, which is critical for designing multi-channel signal processing data paths in applications such as RF processing in wireless applications and SDR for military applications. This technology lets you achieve high-performance design implementations running at near-peak FPGA performance in a matter of minutes compared to the hours, if not days, required to hand-optimize HDL code.

The underlying high-level synthesis technology optimizes the untimed Simulink description into low-level, pipelined hardware targeted to your chosen FPGA and clock rate. The hardware is written out as plaintext VHDL, along with scripts that integrate with the Quartus II software and the ModelSim simulator. These features allow you to generate a high-quality implementation of your design without requiring intimate knowledge of the device architecture.

The DSP Builder tool is available at www.altera.com/dsp. The tool comes with reference designs for WiMAX and WCDMA digital up/down converter designs as well as designs for multi-channel complex filters.




## FEATURES

- Industry's premier DSP design tool based on The MathWorks MATLAB/Simulink design flow
- Creates a seamless bridge between the MATLAB/Simulink environment and the Altera Quartus II software
- Only design tool that generates timing-optimized HDL from a high-level Simulink description of the system
- Automates the tedious part of DSP design: control plane logic and pipeline stage generation
- Optimized for multi-channel DSP data paths
- Effortless device retargeting, for example, from Stratix series FPGAs to Cyclone® series FPGAs, including the latest 40 nm Stratix IV family
- Comes with a suite of reference designs for digital up/down conversion and multi-channel filters

For more information, go to: www.altera.com/dsp

**RSC# 38771 @ www.dsp-fpga.com/rsc**