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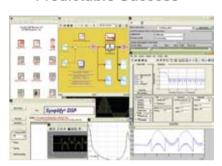

Predictable Success

Synplify DSP

The Synplify DSP solution offers DSP algorithm designers and hardware engineers the most efficient way to get their algorithms into silicon.

System and algorithm designers can quickly capture complex algorithmic behavior using the Synplify DSP library, which includes powerful modeling features such as vector arithmetic, fixed-point precision up to 128 bits, and a rich set of IP cores. Additionally, you can target FPGA or ASIC hardware from a single Simulink model.

The Synplify DSP synthesis engine allows designers to automatically implement and explore area/speed-optimized RTL implementations from a single model. This eliminates the burden of hand-coding functions and architectural optimizations, achieves significantly faster design capture, speeds time to market, and enables rapid design exploration that results in improved quality and lower cost.

FEATURES

› Unique Synplify DSP synthesis engine – Automatically creates optimized algorithm RTL architectures from your DSP model

› Powerful DSP synthesis optimizations – Exploration of speed/area/device technology trade-offs without changing your DSP model

› Comprehensive DSP library – With full multi-rate support and advanced fixed-point quantization analysis

› M-Control feature – Enables use of M-language for concise expression of complex state machine and control logic functionality

› Vector support – Enables concise expression of parallel and multi-channel algorithms common in wireless and video applications

› Extensible IP – Easily create your own reusable, optimizable custom DSP functions using Synplicity's core IP library (blockset)

For more information, contact: info@synplicity.com   **RSC# 38788 @ www.dsp-fpga.com/rsc**