



By Chris A. Ciufu

## The “A’s” have it



Last month, a coincidence of media events and new product releases aligned (or maybe “conspired”) on my desk in such a way that they all came from companies starting with the letter “A”: Altera, Aonix, AMD. I didn’t plan it this way, folks. But I might as well take advantage of this woo-woo *Twilight Zone* moment. Here’s what’s new, and why you should care.

### Altera steps up mil tempo

In the world of big FPGAs, there’s Altera and there’s Xilinx. Using public information, I estimate that about 25 percent of Xilinx’s \$1.8 billion revenue is due to the military market, while only about 10 percent of Altera’s \$1.29 billion revenue comes from defense. But Altera is looking to change all that in a big way by focusing on SWaP, SDR, VPX, mil temp, and AQEC.

In a recent interview with company bigwigs, I got the G2 on this alphabet soup. Size, Weight, and Power (SWaP) are important in many applications these days, but even more so in Software-Defined Radios (SDRs) that are often either deployed as handhelds, or rely on limited power sources in avionics bays or wheeled vehicles. The company’s new Programmable Power Technology in Stratix III devices only activates essential transistors, leaving unused gates in low power standby. Altera says this saves up to 90 percent of active power in SDR waveforms such as Soldier Radio Waveform (SRW). Also, the company surprisingly has VITA’s new 3U VPX form factor on its charts as a key platform for military SWaP applications.

Altera also maintains a secure ITAR design facility, and was one of the *very first participants* in the DoD’s AQEC IC design flow. Now sponsored by GEIA, AQEC (GEIA-STD-0002-1A) is a voluntary IC spec, and companies promise to provide design data to aid mil contractors in making uprating and lifecycle decisions. Finally, and perhaps most importantly, the company designs all of its devices for industrial temp [-40 °C to +100 °C (Tj)], and some Stratix and HardCopy devices extend to the MIL-STD-883 range of -55 °C to +125 °C (Tj). Altera seems very keen on growing military beyond that 10 percent in FY07 (ending December 2007).

### Aonix offers Ada for safety critical

You’re as surprised as I am that Ada is still out there kicking around. Or, maybe you’re not surprised if you’re working on legacy defense systems. Ada’s strong typing and rigid syntax make it ideal for military applications where code ambiguity – things like priority inversions or oddly defined variables – can’t be tolerated lest lives be lost.

During September’s Embedded Systems Conference, Aonix announced a version of their ObjectAda RAVEN that works with Wind River’s VxWorks ARINC 653 for PowerPC processors.

Although the previous sentence is a mouthful, what this means is important for several reasons. First is that users now have a way to run legacy Ada code on top of VxWorks, marrying the old with the new. Secondly, by using the ARINC-653 API, VxWorks 653 creates partitioned environments above the kernel into which multiple distinct and segregated environments can run.

This partitioned model is the core of ARINC-653 safety-critical systems. The idea is that a failure in one module, such as an Ada DO-178B application, would have no effect on the other partitions and hence the overall system’s integrity is maintained. Additionally, the Aonix ObjectAda RAVEN has an ACATS 2.5 Ada 95 compiler and tools that help create or recompile Ada code in a partition; it also relies on the APEX communications API for easy communication with the VxWorks 653 executive API. According to Aonix, this Ada + VxWorks + ARINC-653 combo is unique in the industry. Well, except for something from AdaCore that doesn’t have the APEX API. (Notice the preponderance of “A’s” again. Coincidence? I think not.)

### AMD adds multicore “triple threat”

Just as we went to press, AMD one-upped Intel by introducing the triple-core desktop Phenom x86 processor. Expected to ship in Q1 2008, the device sports three cores on the same die – a feat not to be confused with multicore CPUs having multiple dies in one package. Although it’s rumored that the triple-core Phenom might be a quad-core Phenom with one core “disabled,” this doesn’t detract from AMD’s achievement. (In fact, the original 8031 MCU was just a mask-programmed 8051 with the ROM disabled, and today’s flash memories contain mask-enabled memory arrays.)

AMD’s Balanced Smart Cache speeds access to memory and the shared L3 cache aids in multithreaded applications such as HD video, games, and as-yet-unannounced software applications. Bill Mitchell, corporate VP of the Windows Ecosystem at Microsoft, said “Microsoft is excited to see AMD creating new technologies.” Well, sure. The device sports HyperTransport 3.0 with up to 16 GBps I/O transfer bandwidth, and each core can run at a separate frequency via Cool ‘n’ Quiet 2.0 technology. SYSmark 2007 and 3DMark06 benchmarks are due out soon, as is the quad-core version of the Phenom. We’ll keep an eye on this multicore race between titans.

Chris A. Ciufu  
Group Editorial Director  
cciufu@opensystems-publishing.com