Open standards architectures from standardization bodies such as PICMG, VITA, and others are working to add “more” into embedded and deployed systems: “more” horsepower, I/O, and interoperability. Of the recent standards from VITA, VXS, VPX (VITA 46), VPX-REDI, and Advanced Telecom Computing Architecture (AdvancedTCA) from PICMG, all are poised to offer major benefits to broad market segments. And each includes accommodations for fabrics including Ethernet, PCI Express, and RapidIO, but only RapidIO has achieved penetration across all embedded markets.

Commercial Off-The-Shelf (COTS) vendors probably can’t help having “PC envy.” While the desktop PC ecosystem is essentially dominated by a single architecture, vendors in the embedded community support a rich array of diverse architectures and form factors, leaving OEMs and prime contractors to make sense of this cacophony of choice. The broad embedded markets of military, storage, medical, industrial, and communications each exert different requirements and pressures on the various embedded computing form factors: VME, CompactPCI, PC/104, EBX, ATX, COM, and more. While VME dominates the military space with nearly 75 percent market share and growing, the majority of dollars shipped within the broader embedded market divides fairly evenly among the VME, PCI, and CompactPCI form factors.

Technology evolution in the various PICMG and VITA platform standards is moving toward further commonality, where a set of fabrics can be used across the various form factors. This trend promises to give military primes and embedded OEMs the freedom to choose a single processor/data interconnect architecture and leverage it across multiple chassis form factors. The major chassis/line-card standards have been defined with a set of data fabric pins in a dot zero specification, such as PICMG 3.0, while a number of different fabric protocols are mapped onto these pins: PICMG 3.1 (Ethernet), PICMG 3.2 (InfiniBand), PICMG 3.4 (Advanced Switching), PICMG 3.5 (RapidIO), and so on. The same fabric protocols (RapidIO, PCI Express, Ethernet, and so on) can be defined as dot extensions to the base standard in respective VITA and PICMG chassis standards.

This becomes an interesting point of intersection among these previously orthogonal architectures. Each form factor has its own unique, differentiating strengths. To be sure, each standard will get traction in a robust subsegment of the military market. Until now, it has been challenging to contemplate supporting a single fabric architecture across different form factors.

Next-generation form factor standards

Figure 1 shows a typical dual-star architecture with processor and I/O subsystems interconnected by a system fabric. This basic block diagram is the same across fabrics and form factors. It is technically feasible to implement several different fabrics on PICMG and VITA systems, but there is more ecosystem support around certain fabrics.

Table 1 is a summary of fabric and interconnect dot standards for leading embedded chassis platforms and shows the different standards activity completed for different PICMG and VITA platforms. In the blade/line card chassis architectures, there are three emerging leaders: VXS (VITA 41) and VPX-REDI (VITA 46 and 48) in the military space and AdvancedTCA in the telecommunications space. Each of these form factors has its strengths and weaknesses. Below is a short comparison.

**VXS-VITA 41**

The VXS standard (VME Switched Serial) serves as the latest in a 20-year series of evolutionary improvements for the VME architecture. VME64x products are fabric limited to 1 GHz; the requirement to run 3.125, 6.25, and even 12.5 Gbaud fabrics requires a new high-speed multigigabit VME P0 connector. That is one of the major benefits the VXS standard provides. The big win is that VXS enables existing VME users to migrate to next-generation, high-speed serial fabric solutions without abandoning legacy modules.

This is how it works: VME64 and VXS share the standard, tried-and-true VME P1 and P2 connectors. The new high-speed P0 connector occupies the space between P1 and P2 for fabric-
enabled VXS cards. Legacy VME64 boards plug right into the VXS backplane, but without a P0 they have no access to the high-speed fabric. Designers can, however, bridge a legacy P2 fabric like RACE++ to the new P0 fabric, for example RapidIO, using an SBC that is enabled for both. However, they cannot migrate VME64x cards forward to VXS backplanes because the P0s don’t mate. That makes it more challenging for VME64x fabric users to go forward without obsoleting their installed base of modules.

Mercury recently announced its open-standard PowerStream 6100, a complete VXS system based around a dual-star Serial RapidIO backplane with families of radio frequency, mixed signal, FPGA compute, quad-7448 compute, SBC host/carrier, and more than a dozen pre-integrated I/O PMCs. The PowerStream 6100 also uses the company’s RapidIO switch and IP core, which are sold separately. This system is accompanied by a robust and highly scalable tool set. VXS is now ready for prime time.

VPX and VPX-REDI

VPX also adds high-speed fabric capability but takes another approach to the traditional trade-off between new functionality and backward compatibility. VPX upgrades all of the connectors to the new high-speed differential variety (MultiGig RT2). Designers can still run the VME protocol, but it operates over the new connectors. Legacy VME cards and new VPX cards share a card cage using a hybrid backplane. VPX provides substantially more pins for I/O; since they are the new MultiGig RT2s, they are ready for next-generation I/O devices, some of which are just starting to exceed the clock rating on the VME64 P2 and VME64x P0.

VPX defines a 3U form factor in addition to the ubiquitous 6U. The smaller form factor is ideal for space-constrained applications such as mobile platforms. The 3U form factor provides an attractive migration path for applications using 3U CompactPCI conduction-cooled boards today.

In addition to the dual-star backplane topology, VPX has enough pins to define mesh clusters. In a mesh, every board is connected to every other board using a direct point-to-point connection. Mesh architectures eliminate the need for a central switch on a dedicated fabric card. This design frees up board slots, which again can be advantageous for space-constrained applications.

VITA 48 or Ruggedized Enhanced Design Implementation (REDI) defines a set of interoperability standards for enhanced ruggedization including plug-in units and subrack interfaces for air cooling, conduction cooling, liquid flow-through, and spray cooling. There are no industry standards for liquid and spray cooling, so REDI is poised to raise interoperability to a new level in rugged applications. Until now, it was not possible to build a single card and deploy it using this wide variety of cooling strategies. REDI introduces standards that enable cooling to be much more flexibly applied to a single-board design instantiation.

Other REDI enhancements include an increase in board-to-board spacing and PCB thickness and a significantly increased power budget. REDI is technically not tied to a particular form factor and could conceivably be applied to VPX, VXS, or AdvancedTCA. When REDI and VPX are used together, the system is termed VPX-REDI. The cooling and mechanical enhancements offered by REDI are becoming increasingly important as components use more power, generate more heat, and require more complex routing.

REDI also adds support for Two-Level Maintenance (2LM), which simplifies field servicing. There have been some roadmap announcements on VPX and REDI boards, but no modules yet. However, it appears RapidIO VPX and/or VPX-REDI modules will be available from three module vendors with system-level product coming from Mercury. Stay tuned in 2006 for a lot of exciting choices coming from the VPX and VPX-REDI ecosystems.

AdvancedTCA

While VXS, VPX and REDI are generally used for sensor support and harsh environments, the AdvancedTCA form factor is gaining traction as a communications platform in military applications. AdvancedTCA is a telecom-oriented standard targeted at edge, core, transport, and data center infrastructure equipment.
The board front panels are 8U high, 30.48 mm wide, and 280 mm deep, and applications can add rear transition modules for I/O connectivity. One of AdvancedTCA’s major steps forward is the introduction of an open standard around shelf management based on the TCP/IP-over-Ethernet protocol.

The management bus is separate from the data fabric bus defined to run four-lane 3.125 Gb/s serial interfaces. The strong vendor ecosystem support of AdvancedTCA is naturally attracting attention in the military space. Like CompactPCI, AdvancedTCA has a clear role in benign environments and in military telecommunications infrastructure. AdvancedTCA has the ecosystem to support media gateways and multifunction routers, which are critical elements of a military field communications network.

Modern fabrics compared
VXS, VPX, REDI, and AdvancedTCA can technically run many different serial backplane fabrics. Table 1 shows support across the board in the standards area for RapidIO, PCI Express, and Ethernet. These three are the clear leaders in terms of committed standards activity, design-win momentum, and overall ecosystem activity. Many vendors present themselves as fabric-agnostic, which may indicate they don’t know enough to guide customers to a sensible choice. Following is a quick reference on the strengths and weaknesses of each interconnect.

Ethernet
Ethernet is widely used in telecommunications applications, but it is less popular in military applications as a backplane standard due to the processor overhead imposed by segmenting and reassembling IP packets and managing packet loss. The rule of thumb is that it takes 1 GHz CPU processing power to terminate a Gigabit Ethernet port. TCP/IP Offload Engines (TOEs) can help, but they add size, weight, and power. In military applications, Ethernet is best used for command and control traffic and low-bandwidth utilization (<60% of Gbps for GbE) data connectivity.

PCI Express
PCI Express is gaining traction in embedded computing for I/O connectivity and small processor clusters. If more than simple connectivity is required, system designers generally adopt a system fabric with more functionality. The Advanced Switching Interconnect (ASI) camp eloquently makes this case, although it is weak in follow-through. The RapidIO switch fabric is being used to bridge PCI Mezzanine Card traffic in some real-world design wins referenced below. The same capabilities will enable the RapidIO standard to serve as a good fabric for PCI Express subsystems, which are based on the same PCI architecture.

PCI Express is ubiquitous in control plane and I/O connectivity throughout embedded computing, but it is persona non grata in the telecommunications data plane. There simply is no PCI Express network or communications processor that makes line-rate data plane computing possible.

With Ethernet strong in communications only and PCI Express strong in embedded I/O only, is there any fabric gaining traction as a backplane system fabric in all markets?

RapidIO: The “strongest embedded ecosystem”
The RapidIO standard has achieved penetration across all the major embedded markets: military, communications, storage, and imaging in both control and data applications. The RapidIO switch fabric is widely implemented across the PICMG and VITA standards communities because it plays to the widest audience of constituent markets. This is because of several factors. First, it has major platform wins driven by the life-cycle demands and economics of the embedded military, storage, image processing, and telecom markets, as opposed to the PC Desktop or LAN (think nine-month silicon life cycles). Second, the RapidIO switch fabric has a broad ecosystem of silicon, software, system, IP, and tools vendors. The emergence of silicon from tier-one vendors, like Freescale and TI, has done much to shorten hallway discussions centered around the fabric wars.

Freescale Semiconductor produces a family of communications processors called PowerQUICC, which collectively have majority market share in communications computing. The PQIII 8548, which is available now, supports serial RapidIO. Every major off-the-shelf operating system vendor is supporting the RapidIO switch fabric on these Freescale processors: Wind River, Enea, QNX, and Monta Vista, and other Linux vendors. Freescale has also announced its dual-core 8641, with serial RapidIO, which will be the company’s highest-performing AltiVec processor to date.

Texas Instruments, which has dominant market share in wireless infrastructure computing, announced a high-end DSP in May to be available with serial RapidIO. An AMC with the TI DSP supporting the RapidIO standard will be available for use in AdvancedTCA systems.

As a protocol, the RapidIO switch fabric has already achieved deployment in major OEMs and defense contractors. It is being deployed in major Unmanned Aerial Vehicle (UAV) platforms (Global Hawk and E-10A) as part of Phase II of the Northrop Grumman/Raytheon MP-RTIP program. The RapidIO standard is also being incorporated into the Lockheed Martin Aegis Ballistic Missile Defense (BMD) system. Micronic Laser Systems AB is using the RapidIO standard in manufacturing inspection systems. Among the new serial fabrics, RapidIO is a solid leader in terms of production readiness and deployment in embedded and military platforms.

The preponderance of support in key solutions, coupled with significant OEM and military prime contractor interest, has drawn significant RapidIO switch support. Aside from the switch mentioned above, vendors Tundra, IDT, and Erlang have publicly disclosed RapidIO switches. Development systems for the Tundra switch are currently marketed by Silicon Turnkey Express.

The RapidIO switch fabric now has support from several IP vendors including Altera, Cadence, GDA, Jennic, LSI Logic, Praesem, Rapid Prototypes, and Xilinx. These RapidIO IP cores can be targeted at ASICs, FPGAs, and structured ASICs. As one example of many, Jennic’s IP core can be targeted at the LSI Logic RapidChip and at the NEC ASIC process.

Finally, the RapidIO standard has earned support from the critical test-equipment vendors Agilent and Tektronix, and, perhaps more notably, is uniquely supported by sophisticated GUI-based fabric management tools such as those available from Fabric Embedded Tools. RapidIO technology is impressing embedded OEMs and military primes as the lowest risk and fastest path to get scalable system products to market.
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