VITA STANDARDS UPDATE

By John Rynearson

VITA 46.20 and 46.21 suspend meetings pending OpenVPX's completion

Editor's note: By the time you read this in June, the May VSO meeting will have taken place. Be sure to check out our online E-cast archives for the latest video and audio updates on VITA standards. See http://ecast.opensystemsmedia.com.

Be sure to check out our online E-cast archives for the latest video and audio updates on VITA 41, 46, and 48. See http://ecast.opensystemsmedia.com.

VSO ANSI accreditation

Accredited as a Standards Development Organization (SDO) in June 1993 by the American National Standards Institute (ANSI), the VITA Standards Organization (VSO) meets every two months to address vital embedded bus and board industry standards issues. Information on ANSI/VITA standards is available on the VITA website at www.vita.com.

VSO study and working group activities

Standards within the VSO may be initiated by a study group and developed by a working group. A study group requires the sponsorship of only one VSO member and is used to build interest in a standard. A working group requires the sponsorship of at least three VITA members, and the proposed work must fit within the defined scope of VITA's accreditation with ANSI.

VITA 41.6, VXS 1x GbE Control Channel Layer

Objective: To define and assign 1x GbE signals for communication over signal sets currently defined as reserved for future use in VXS.0.

Status: VITA 41.6 has completed its ANSI recirculation ballot. Changes to the draft need to be reviewed before ANSI submission.

VITA 46.4, PCI Express on VPX Fabric Connector

Objective: To standardize the implementation of PCI Express fabric in VITA 46 environments and define the mapping of PCI Express links on a VPX connector.

Status: The group is discussing the need for a backplane ref_clk. Some evidence indicates that a common ref_clk is required for reliable operation.

VITA 46.9, PMC/XMC/Ethernet Signal Mapping to 3U/6U on VPX User I/O

Objective: To define how mezzanine card pins map to the VITA 46.0 plug-in modules.

Status: The working group has decided to remove the Ethernet signal mapping from this standard and move it to either 46.6 or an overall system specification.

PDF – This column and the accompanying table are available at www.vmecritical.com, then click on VITA Standards.

For more information, e-mail John at techdir@vita.com.

VITA 46.11, System Management on VPX

Objective: To develop a method to provide for system management on a VPX module.

Status: Dan Toohey, Mercury Computer Systems, Inc., has become the chairman of this activity. The working group is discussing the scope of the effort and defining both a physical and logical structure to aid in discussion.

VITA 46.14, Mixed Signal VPX

Objective: To develop a standard that supports mixed signals on a mezzanine card that will be specific to the VPX mechanical format.

Status: The group is discussing how to include mixed signal connector formats in ANSI/VITA 46.0, VPX, which currently only includes digital signals.

VITA 46.20, VPX Switch Slot Definition

Objective: To define the pin mappings of one or two switch slots within 3U and 6U VPX systems and to provide recommendations for typical backplane interconnection topologies between VPX switch slots and VPX payload slots.

Status: This group has suspended meetings pending the completion of the OpenVPX system specification.

VITA 46.21, Distributed Switching on VPX

Objective: To define a small set of standard distributed switching topologies with minimal hops that are application agnostic.

Status: This effort has been suspended pending completion of the OpenVPX system specification.

VITA 57.1, FPGA I/O Mezzanine Pin Assignments

Objective: To define a standard mezzanine connector, form factor, and pin assignment strategy optimized for connecting I/O to FPGAs.

Status: Revisions have been added to VITA 57.1, and balloters are being solicited for the revision ballot.

VITA 58, Line Replaceable Integrated Electronic Chassis

Objective: To develop a standard for electronic chassis.

Status: VITA 58 has completed its initial ANSI ballot and public review. The ballot passed and the results will be submitted for ANSI recognition, which is expected shortly.

VITA Standards Activity Chart

MARCH MEETING HIGHLIGHTS

Standard *Reaffirmed	Title	Status	*VME and CS* edition
ANSI/VITA 1.0 *2002	VME64 Standards	Released	
ANSI/VITA 1.1 *2003	VME64 Extensions	Released	Aug. 2004
ANSI/VITA 1.3 *2003	9U x 400 mm Format	Released	
ANSI/VITA 1.5	2eSST	Released	Feb. 2004
ANSI/VITA 1.6 *2005	Keying for Conduction-cooled VME	Released	
ANSI/VITA 1.7	Increased Connector Current Level	Released	
ANSI/VITA 3 *2002	Board Level Live Insertion	Released	
ANSI/VITA 4.0 *2002	IP Modules	Released	
ANSI/VITA 4.1 *2003	IP/I/O Mapping to VME64x	Released	
ANSI/VITA 5.1 *2004	RACEway Interlink	Released	
VITA 5.2	RACEway++	Withdrawn	Aug. 2004
ANSI/VITA 6.0 *2002	SCSA	Released	
ANSI/VITA 6.1 *2003	SCSA Extensions	Released	
ANSI/VITA 10 *2002	SKYchannel Packet Bus	Released	
ANSI/VITA 12 *2002	M-Modules	Released	
ANSI/VITA 13	Pin Assignments for HIC on VME	Withdrawn	
ANSI/VITA 17.0 *2004	Front Panel Data Port	Released	
ANSI/VITA 17.1	Serial Front Panel Data Port	Released	Feb. 2004
VITA 17.2	Serial Front Panel Data Port (SFPDP) Channel	Working Group	Feb. 2009
VITA 19.0	BusNet Overview	Withdrawn	
ANSI/VITA 19.1	BusNet MAC	Withdrawn	
ANSI/VITA 19.2	BusNet LLC	Withdrawn	
ANSI/VITA 20 *2005	Conduction-cooled PMC	Released	Apr. 2005
ANSI/VITA 23 *2004	VME64x Extensions for Physics	Released	
ANSI/VITA 25	VISION	Withdrawn	
ANSI/VITA 26 *2003	Myrinet-on-VME	Released	
ANSI/VITA 29	PC•MIP	Released	
ANSI/VITA 30.0 *2005	2 mm Connector Practice on Euroboard	Released	
ANSI/VITA 30.1	2 mm Conduction-cooled Euroboard	Released	
VITA 30.2	Power Connector Equipment Practice	Released	Apr. 2007
ANSI/VITA 31.1	GbE on VME64x Backplanes	Released	Feb. 2004
ANSI/VITA 32	Processor PMC	Released	Feb. 2004
VITA 34	A Scalable Electromechanical Architecture	Working Group	Apr. 2004
ANSI/VITA 35 *2005	Pin Assignments for PMC to VME	Released	
VITA 36	PMC I/O Modules	Withdrawn	Apr. 2004
ANSI/VITA 38	System Management on VME	Released	
ANSI/VITA 39	PCI-X Aux. Std. for PMCs and PrPMCs	Released	Feb. 2004
ANSI/VITA 40	Status Indicator Standard	Released	Dec. 2008
ANSI/VITA 41.0	VXS: VME Switched Serial	Released	Oct. 2006
ANSI/VITA 41.1	VXS: InfiniBand Protocol Layer	Released	Oct. 2006
ANSI/VITA 41.2	VXS: RapidIO Protocol Layer	Released	Oct. 2006
VITA 41.3	VXS: GbE	Working Group	Apr. 2006
VITA 41.4	VXS: PCI Express	Working Group	Apr. 2006
VITA 41.6	VXS: 1x GbE Control Channel Layer Standard	Working Group	June 2009
VITA 41.7	VXS: Processor Mesh Topology	Working Group	
VITA 41.8	VXS: 10 GbE Protocol Layer Standard	Working Group	June 2009
VITA 41.10	VXS: Live Insertion Requirements for VITA 41 Boards	Working Group	Apr. 2006
VITA 41.11	VXS: Rear Transition Modules	Working Group	Apr. 2006
VITA 42.0	XMC	Released	Feb. 2009
ANSI/VITA 42.1	XMC: Parallel RapidIO	Released	Oct. 2006
ANSI/VITA 42.2	XMC: Serial RapidIO	Released	Oct. 2006
ANSI/VITA 42.3	XMC: PCI Express	Released	Oct. 2006
VITA 42.4	HyperTransport	Working Group	Apr. 2005
VITA 42.6	XMC: 10 GbE Ethernet 4-Lane Protocol Layer Standard	Working Group	June 2009
VITA 42.10	XMC: General Purpose I/O	Working Group	
VITA 42.20	XMC: Dual Fabric I/O	Working Group	
VITA 43S	Hot Swap NextGen Mezzanine	Inactive	Feb. 2004
VITA 45S	Serial VME	Canceled	Apr. 2004
ANSI/VITA 46.0	VPX: Base Specification	Working Group	Feb. 2009
ANSI/VITA 46.1	VPX: VMEbus Signal Mapping	Working Group	Feb. 2008
VITA 46.3	VPX: Serial RapidIO on VPX Fabric Connector	Working Group	Oct. 2008
VITA 46.4	VPX: PCIe Mapping and Advanced Switch Signal Mapping	Working Group	June 2009
VITA 46.5	VPX: HyperTransport	Working Group	
VITA 46.6	VPX: GbE	Working Group	
VITA 46.7	VPX: 10 GbE	Working Group	
VITA 46.9	PMC/XMC/Ethernet Signal Mapping to 3U/6U on VPX User I/O	Working Group	June 2009
VITA 46.10	Rear Transition Module for VPX	Working Group	June 2009
VITA 46.11	System Management on VPX	Working Group	June 2009
VITA 46.12	Fiber Optic Interconnect	Working Group	June 2009
VITA 46.14	Mixed Signal VPX	Working Group	June 2009
VITA 46.20	VPX Switch Slot Definition	Working Group	June 2009
VITA 46.21	Distributed Switching on VPX	Working Group	June 2009
ANSI/VITA 47	Env., Design and Const., Safety, and Qual. for Plug-in Units	Released	Jun. 2006
VITA 47r1	Revisions to ANSI/VITA 47	Released	Feb. 2008
VITA 47r2	Revisions to ANSI/VITA 47	Working Group	Feb. 2009
VITA 48.0	REDI: Ruggedized Enhanced Design Implementation	Working Group	Feb. 2009
VITA 48.1	Mechanical Specs for Microcomputers Using Air Cooling	Working Group	
VITA 48.2	Mechanical Specs for Microcomputers Using Conduction Cooling	Working Group	
VITA 48.3	Mechanical Specs for Microcomputers Using Liquid Cooling	Working Group	
VITA 49.0	VITA Radio Transport (VRT)	Working Group	Feb. 2009
VITA 49.1	VITA Radio Link Layer (VRL)	Working Group	Oct. 2008
VITA 50	Best Practices for Electronic Module Cooling	Inactive	Dec. 2007
ANSI/VITA 51.0 *2008	Reliability Prediction	Released	Aug. 2008
ANSI/VITA 51.1 *2008	Reliability Prediction: MIL-HDBK-217 Daughter	Released	
VITA 51.2	Physics of Failure Reliability Predictions	Working Group	Feb. 2009
VITA 52	Lead-free Practices	Working Group	Oct. 2006
VITA 53	Commercial Technology Market Surveillance	Working Group	Feb. 2009
VITA 54	Embedded Platform Management Architecture (EPMA)	Inactive	Aug. 2005
VITA 55	Virtual Streaming Protocol	Inactive	Feb. 2009
VITA 56	Express Mezzanine Card (EMC)	Inactive	Oct. 2007
ANSI/VITA 57 *2008	FMC: FPGA Mezzanine Card Standard	Released	Dec. 2008
VITA 57.1	FPGA I/O Mezzanine Pin Assignments	Working Group	June 2009
VITA 58	Line Replaceable Integrated Electronics Chassis	Working Group	June 2009
VITA 59	RSE: Rugged System-On-Module Express	Working Group	Dec. 2008
VITA 60	Alternative Connector on VPX	Working Group	Feb. 2009
VITA 61	Alternative Connector for XMC	Working Group	Feb. 2009
VITA 62	Power Supply Modules	Working Group	June 2009
VITA 63	KVPX	Working Group	Feb. 2009
VITA 64	Optimized Footprint for VITA 60	Working Group	Feb. 2009

For corrections or suggestions, contact Chris Ciufo, *VME and Critical Systems* magazine, at cciufo@opensystemsmedia.com.